

# 128 Bit IDIC<sup>®</sup> for Radio Frequency Identification

IDIC<sup>®</sup> stands for **IDentification Integrated Circuit** and is a trademark of TEMIC.

## Description

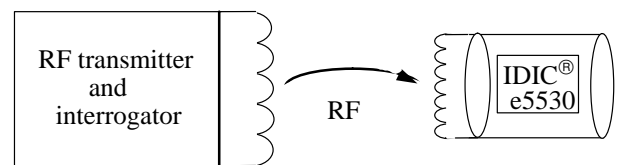
The e5530 is part of a closed coupled identification system. It receives power from an RF transmitter which is coupled inductively to the IDIC<sup>®</sup>. The frequency is typically 100 to 450 kHz. Receiving RF, the IDIC<sup>®</sup> responds with a data stream by damping the incoming RF

via an internal load. This damping-in-turn can be detected by the interrogator. The identifying data are stored in a 128 bit PROM on the e5530, realized as an array of laser-programmable fuses. The logic block diagram for the e5530 is shown in figure 2. The data are output bit-serially as a code of length 128, 96, 64 or 32 bits. The chips are factory-programmed with a unique code.

## Features

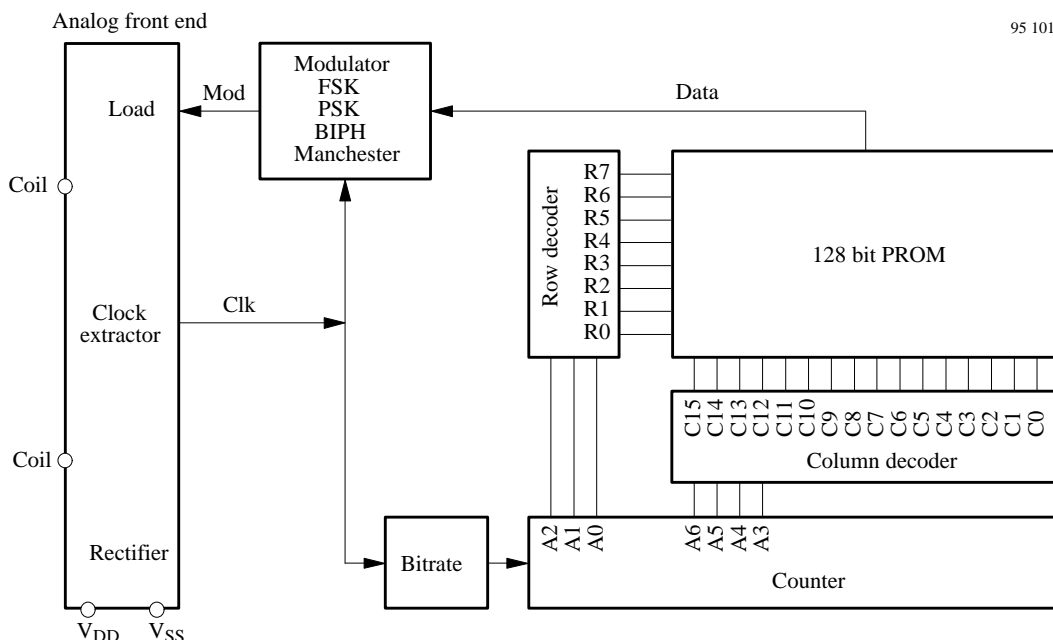
- Low power, low voltage CMOS
- Rectifier, voltage limiter, clock extraction on-chip (no battery)
- Small size
- Factory laser programmable ROM
- Operating temperature range -40 to +125°C
- **Radio Frequency (RF):** 100 to 450 kHz
- Transmission options  
Code length: 128, 96, 64, 32 bits  
Bitrate [bit/s]: RF/8, RF/16, RF/32, RF/40, RF/50, RF/64, RF/80, RF/100, RF/128, RF/256  
Modulation: FSK, PSK, BIPH, Manchester BIPH-FSK

## Application



95 10318

Figure 1.



95 10155

Figure 2. Block diagram

## Functional Description

### Read Operation

Once the IC detects the incoming RF, the IC repetively reads out the code data as long as the RF signal is applied. The transition from the last bit to bit 1 of the next sequence occurs without interruption. Data is transmitted by alternating damping of the incoming RF via a load. Different kinds of modulation and bitrates are optionally available.

### Rectifier

For internal power supply, an on-chip bridge rectifier is used which consists of two diodes and two n-channel transistors. A Zener diode, which protects the circuit against overvoltage on the coil inputs, and a smoothing capacitor for the internal supply are also provided.

### Damping Load

Incoming RF will be damped by the power consumption of the IC itself and by an internal load, which is controlled by the modulator. The loads are p-channel transistors connected between  $V_{DD}$  and the coil inputs. The layout includes metal mask options for the load circuit: single-side, double-side and alternate-side modulation.

### Modulator

One of four methods of modulation can be selected by fuses. The timing diagram is shown in figure 3.

#### FSK

Logical "1" and "0" are distinguished via different frequencies of damping. The frequency for "1" is the RF divided by 10, a "0" divides by 8.

#### PSK

A logical "1" causes (at the end of the bit period) a 180° phase shift on the carrier frequency, while a logical "0" causes no phase shift. The carrier frequency is  $RF/2$ .

#### BIPH

Logical "1" produces a signal which is the same as the bitclock and a logical "0" produces a signal of twice the bitclock period.

#### Manchester

A logical "1" causes a positive edge in the middle of a bit period, while a logical "0" causes negative edge.

A combination of BIPH- and FSK-modulation is also optionally available. The available combinations between the modulation types and the bitrates are shown in table "Transmission Options".

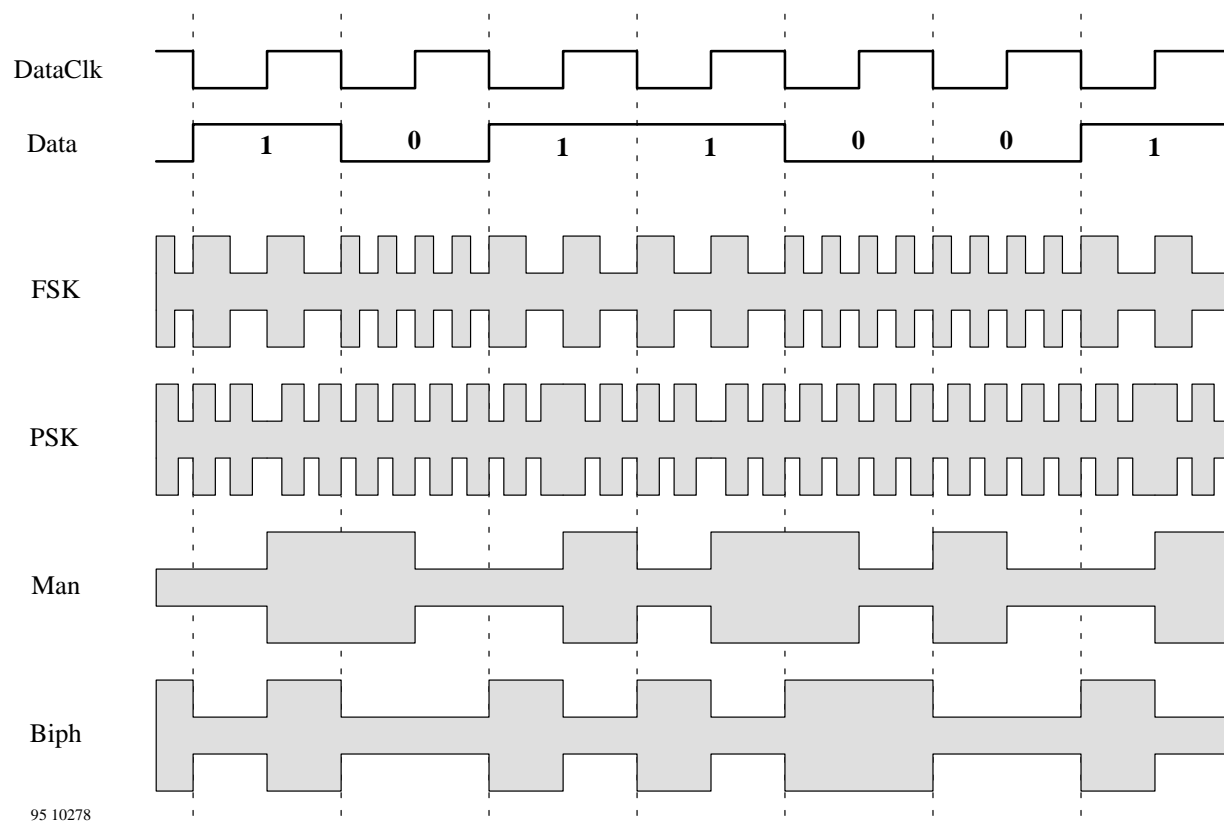


Figure 3. Timing diagram for modulation options

## Absolute Maximum Ratings

Parameters	Symbol	Value	Unit
Maximum current into Coil1 and Coil2	$I_{coil}$	10	mA
Maximum power dissipation (dice)	$P_{tot}$	100	mW*
Maximum ambient air temperature with voltage applied	$T_{amb}$	-40 to +125	°C
Storage temperature	$T_{stg}$	-65 to +150	°C

\* Free-air condition. Time of application: 1 s

Stresses above those listed under 'Absolute Maximum Ratings' may cause permanent damage to the device. Functional operation of the device at these conditions is not implied.

## Operating Characteristics

$T_{amb} = 25^{\circ}\text{C}$ , reference terminal is  $V_{DD}$ , operating voltage  $V_{DD} - V_{SS} = 3\text{ V}$  dc, unless otherwise specified

Parameters	Test Conditions / Pins	Symbol	Min.	Typ. *	Max.	Unit
Operating voltage	Condition for logic test	$V_{SS}$	-1.5		-5.0	V
Operating temperature		$T_{amb}$	-40		125	$^{\circ}\text{C}$
Input frequency (RF)		$f_{CLK}$	100		450	kHz
Operating current	$f_{CLK} = 125\text{ kHz}$ , $V_{SS} = -2\text{ V}$	$I_{CC}$		3		$\mu\text{A}$
Clamp voltage	$I = 4\text{ mA}$	$V_{CL}$	6.7		10	V

\* Typical parameters represent the statistical mean values

## Transmission Options

Modulation	Carrier Frequency (CF)	Bitrate [bit/s]
FSK	RF/8, RF/10	RF/32, RF/40, RF/50, RF/64, RF/80, RF/100, RF/128
PSK	RF/2	CF/4, 8, 16, 32
BIPH		RF/8, RF/16, RF/32, RF/64, RF/100, RF/128
Manchester		RF/8, RF/16, RF/32, RF/64, RF/100, RF/128

**We reserve the right to make changes to improve technical design and may do so without further notice.**

Parameters can vary in different applications. All operating parameters must be validated for each customer application by the customer. Should the buyer use TEMIC products for any unintended or unauthorized application, the buyer shall indemnify TEMIC against all claims, costs, damages, and expenses, arising out of, directly or indirectly, any claim of personal damage, injury or death associated with such unintended or unauthorized use.

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