DG408/409

8-Ch/Dual 4-Ch High Performance CMOS Analog Multiplexers

Features

- Low On-Resistance—$r_{DS(on)}$: 100 Ω
- Low Charge Injection—Q: 20 pC
- Fast Transition Time—t_{TRANS}: 160 ns
- Low Power—I_{SUPPLY}: 10 µA
- Single Supply Capability
- 44-V Supply Max Rating

Benefits

- Reduced Switching Errors
- Reduced Glitching
- Improved Data Throughput
- Reduced Power Consumption
- Increased Ruggedness
- Superior to DG508/509A
- Wide Supply Ranges (± 5 V to ± 20 V)

Applications

- Data Acquisition Systems
- Audio Signal Routing
- ATE Systems
- Battery Powered Systems
- High Rel Systems
- Single Supply Systems
- Medical Instrumentation

Description

The DG408 is an 8-channel single-ended analog multiplexer designed to connect one of eight inputs to a common output as determined by a 3-bit binary address (A_0, A_1, A_2). The DG409 is a dual 4-channel differential analog multiplexer designed to connect one of four differential inputs to a common dual output as determined by its 2-bit binary address (A_0, A_1). Break-before-make switching action protects against momentary crosstalk between adjacent channels.

An on channel conducts current equally well in both directions. In the off state each channel blocks voltages up to the power supply rails. An enable (EN) function allows the user to reset the multiplexer/demultiplexer to all switches off for stacking several devices. All control inputs, address (A_x) and enable (EN) are TTL compatible over the full specified operating temperature range.

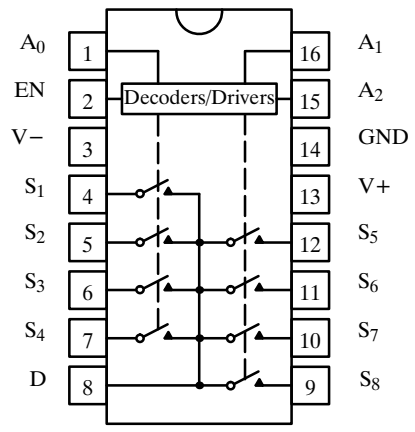
Applications for the DG408/409 include high speed data acquisition, audio signal switching and routing, ATE systems, and avionics. High performance and low power dissipation make them ideal for battery operated and remote instrumentation applications.

Designed in the 44-V silicon-gate CMOS process, the absolute maximum voltage rating is extended to 44 V. Additionally, single supply operation is also allowed. An epitaxial layer prevents latchup.

For additional information please see App Note AN201 and Technical TA201.

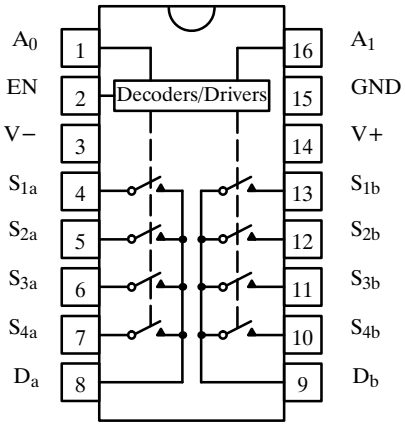
Functional Block Diagrams and Pin Configurations

DG408 Dual-In-Line and SOIC



Top View

DG409 Dual-In-Line and SOIC



Top View

Functional Block Diagrams and Pin Configurations (Cont'd)

Truth Table — DG408

A_2	A_1	A_0	EN	On Switch
X	X	X	0	None
0	0	0	1	1
0	0	1	1	2
0	1	0	1	3
0	1	1	1	4
1	0	0	1	5
1	0	1	1	6
1	1	0	1	7
1	1	1	1	8

Truth Table — DG409

A_1	A_0	EN	On Switch
X	X	0	None
0	0	1	1
0	1	1	2
1	0	1	3
1	1	1	4

Logic "0" = $V_{AL} \leq 0.8$ V
Logic "1" = $V_{AH} \geq 2.4$ V
X = Don't Care

Ordering Information — DG408

Temp Range	Package	Part Number
−40 to 85°C	16-Pin Plastic DIP	DG408DJ
	16-Pin SOIC	DG408DY
−55 to 125°C	16-Pin CerDIP	DG408AK
		DG408AK/883
		5962-920401MEA
	LCC-20*	5962-920401M2A

Ordering Information — DG409

Temp Range	Package	Part Number
−40 to 85°C	16-Pin Plastic DIP	DG409DJ
	16-Pin SOIC	DG409DY
−55 to 125°C	16-Pin CerDIP	DG409AK
		DG409AK/883
		5962-920402MEA
	LCC-20*	5962-920402M2A

*Block Diagram and Pin Configuration not shown.

Absolute Maximum Ratings

Voltage Referenced to V−
V+ . . . . . 44 V
GND . . . . . 25 V
Digital Inputs[a], V_S, V_D . . . . . (V−) −2 V to (V+) +2 V or 20 mA, whichever occurs first
Current (Any Terminal) . . . . . 30 mA
Peak Current, S or D
(Pulsed at 1 ms, 10% Duty Cycle Max) . . . . . 100 mA
Storage Temperature (AK Suffix) . . . . . −65 to 150°C
(DJ, DY Suffix) . . . . . −65 to 125°C
Power Dissipation (Package)[b]
16-Pin Plastic DIP[c] . . . . . 450 mW
16-Pin Narrow SOIC[d] . . . . . 600 mW
16-Pin CerDIP[e] . . . . . 900 mW
LCC-20[f] . . . . . 750 mW

Notes
a. Signals on S_X, D_X or IN_X exceeding V+ or V− will be clamped by internal diodes. Limit forward diode current to maximum current ratings.
b. All leads soldered or welded to PC board.
c. Derate 6 mW/°C above 75°C.
d. Derate 7.6 mW/°C above 75°C.
e. Derate 12 mW/°C above 75°C.
f. Derate 10 mW/°C above 75°C.

Specifications[a]

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 15 V, V− = −15 V V_{AL} = 0.8 V, V_{AH} = 2.4 V[f]		Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	 Max[d]	D Suffix −40 to 85°C Min[d]	 Max[d]	Unit
Analog Switch										
Analog Signal Range[e]	V_{ANALOG}			Full		−15	15	−15	15	V
Drain-Source On-Resistance	$r_{DS(on)}$	V_D = ±10 V, I_S = −10 mA		Room Full	40		100 125		100 125	Ω
$r_{DS(on)}$ Matching Between Channels[g]	$\Delta r_{DS(on)}$	V_D = ±10 V		Room			15		15	%
Source Off Leakage Current	$I_{S(off)}$	V_S = ±10 V, V_D = ∓10 V V_{EN} = 0 V		Room Full		−0.5 −50	0.5 50	−0.5 −5	0.5 5	nA
Drain Off Leakage Current	$I_{D(off)}$	V_D = ±10 V V_S = ∓10 V V_{EN} = 0 V	DG408	Room Full		−1 −100	1 100	−1 −20	1 20	
			DG409	Room Full		−1 −50	1 50	−1 −10	1 10	
Drain On Leakage Current	$I_{D(on)}$	V_S = V_D = ±10 V Sequence Each Switch On	DG408	Room Full		−1 −100	1 100	−1 −20	1 20	
			DG409	Room Full		−1 −50	1 50	−1 −10	1 10	
Digital Control										
Logic High Input Voltage	V_{INH}			Full		2.4		2.4		V
Logic Low Input Voltage	V_{INL}			Full			0.8		0.8	
Logic High Input Current	I_{AH}	V_A = 2.4 V, 15 V		Full		−10	10	−10	10	µA
Logic Low Input Current	I_{AL}	V_{EN} = 0 V, 2.4 V, V_A = 0 V		Full		−10	10	−10	10	
Logic Input Capacitance	C_{in}	f = 1 MHz		Room	8					pF
Dynamic Characteristics										
Transition Time	t_{TRANS}	See Figure 2		Full	160		250		250	ns
Break-Before-Make Interval	t_{OPEN}	See Figure 4		Room		10		10		
Enable Turn-On Time	$t_{ON(EN)}$	See Figure 3		Room Full	115		150 225		150	
Enable Turn-Off Time	$t_{OFF(EN)}$			Room	105		150		150	
Charge Injection	Q	C_L = 10 nF, V_S = 0 V		Room	20					pC
Off Isolation[h]	OIRR	V_{EN} = 0 V, R_L = 1 kΩ f = 100 kHz		Room	−75					dB
Source Off Capacitance	$C_{S(off)}$	V_{EN} = 0 V, V_S = 0 V, f = 1 MHz		Room	3					pF
Drain Off Capacitance	$C_{D(off)}$	V_{EN} = 0 V, V_D = 0 V f = 1 MHz	DG408	Room	26					
			DG409	Room	14					
Drain On Capacitance	$C_{D(on)}$		DG408	Room	37					
			DG409	Room	25					
Power Supplies										
Positive Supply Current	I+	V_{EN} = V_A = 0 V or 5 V		Full	10		75		75	µA
Negative Supply Current	I−			Full	1	−75		−75		
Positive Supply Current	I+	V_{EN} = 2.4 V, V_A = 0 V		Room Full	0.2		0.5 2		0.5 2	mA
Negative Supply Current	I−			Full		−500		−500		µA

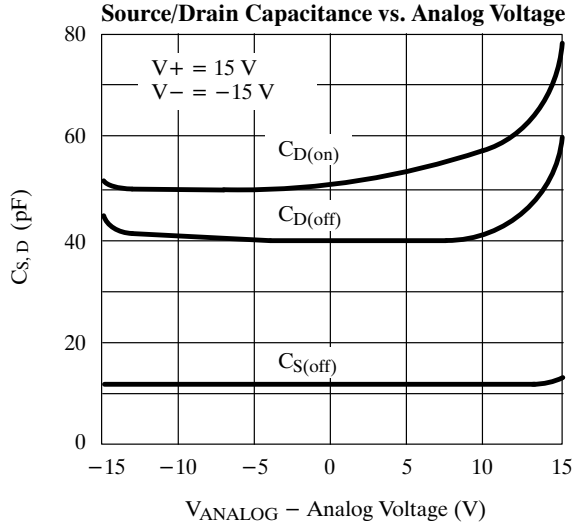
Specifications[a] for Single Supply

Parameter	Symbol	Test Conditions Unless Otherwise Specified V+ = 12 V, V− = 0 V V_{AL} = 0.8 V, V_{AH} = 2.4 V[f]	Temp[b]	Typ[c]	A Suffix −55 to 125°C Min[d]	A Suffix −55 to 125°C Max[d]	D Suffix −40 to 85°C Min[d]	D Suffix −40 to 85°C Max[d]	Unit
Analog Switch									
Drain-Source On-Resistance[e, f]	$r_{DS(on)}$	V_D = 3 V, 10 V, I_S = − 1 mA	Room	90					Ω
Dynamic Characteristics									
Switching Time of Multiplexer[e]	t_{TRANS}	V_{S1} = 8 V, V_{S8} = 0 V, V_{IN} = 2.4 V	Room	180					ns
Enable Turn On Time[e]	$t_{ON(EN)}$	V_{INH} = 2.4 V, V_{INL} = 0 V V_{S1} = 5 V	Room	180					
Enable Turn Off Time[e]	$t_{OFF(EN)}$		Room	120					
Charge Injection[e]	Q	C_L = 1 nF, V_S= 6 V, R_S = 0	Room	5					pC

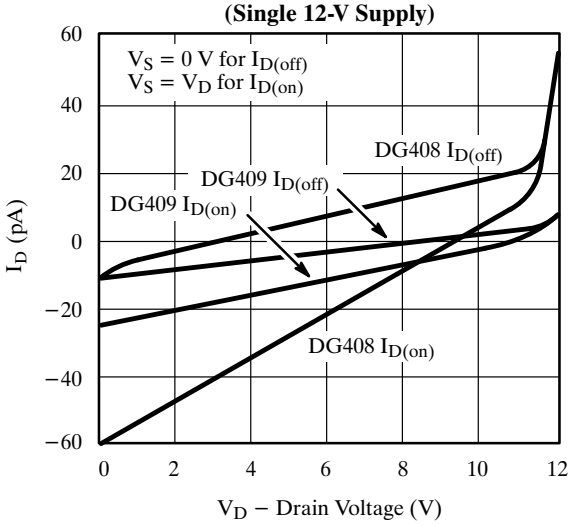
Notes
a. Refer to PROCESS OPTION FLOWCHART (Section 5 of the 1994 Data Book or FaxBack number 7103).
b. Room = 25°C, Full = as determined by the operating temperature suffix.
c. Typical values are for DESIGN AID ONLY, not guaranteed nor subject to production testing.
d. The algebraic convention whereby the most negative value is a minimum and the most positive a maximum, is used in this data sheet.
e. Guaranteed by design, not subject to production test.
f. V_{IN} = input voltage to perform proper function.
g. $\Delta r_{DS(on)} = r_{DS(on)}$ Max − $r_{DS(on)}$ Min.
h. Worst case isolation occurs on Channel 4 do to proximity to the drain pin.

Typical Characteristics

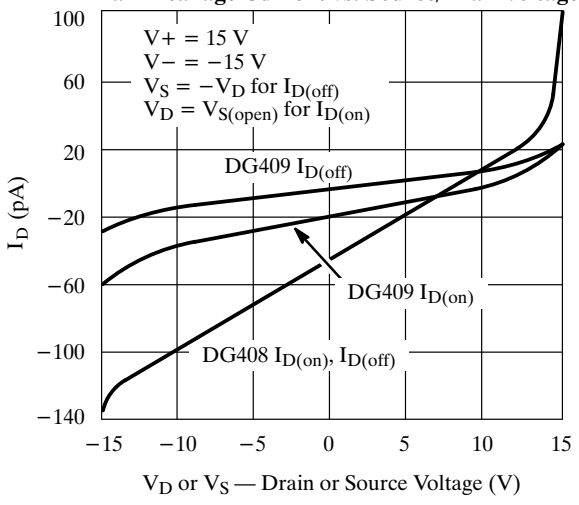
Source/Drain Capacitance vs. Analog Voltage



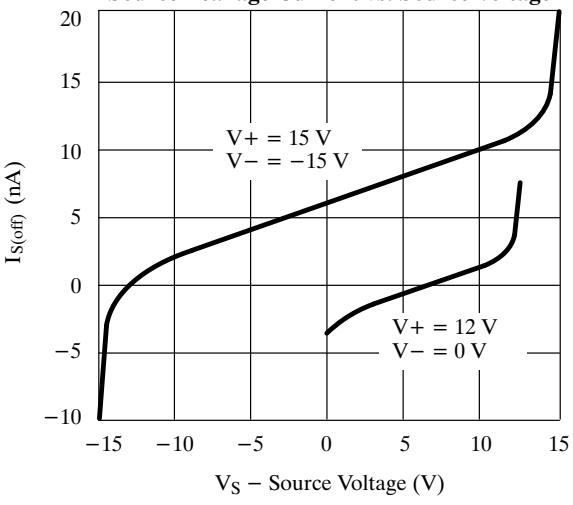
Drain Leakage Current vs. Source/Drain Voltage (Single 12-V Supply)



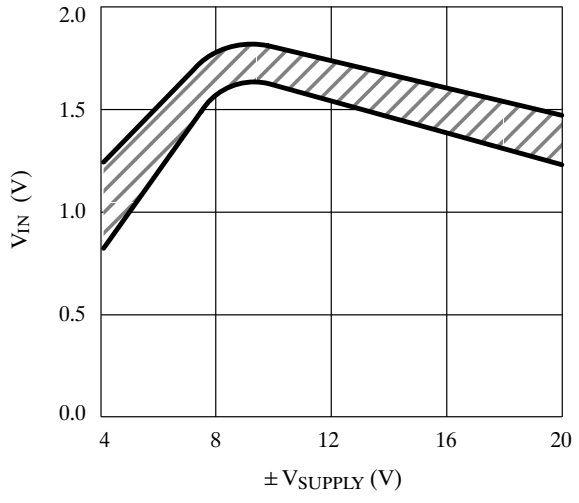
Drain Leakage Current vs. Source/DrainVoltage



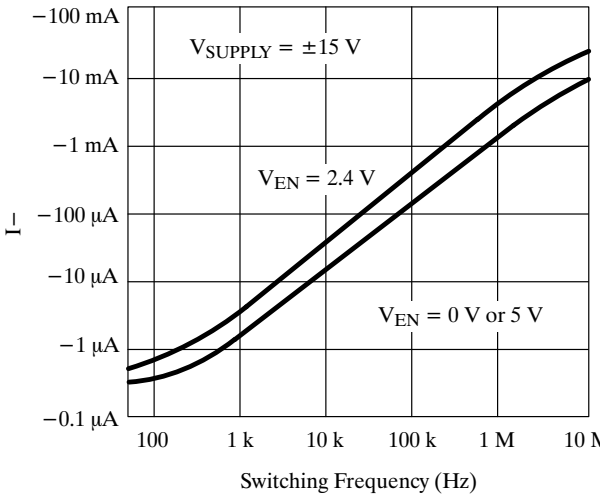
Source Leakage Current vs. Source Voltage



Input Switching Threshold vs. Supply Voltage

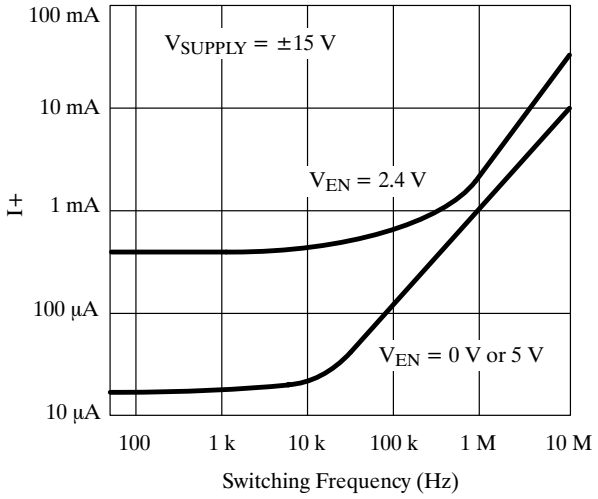


Negative Supply Current vs. Switching Frequenc

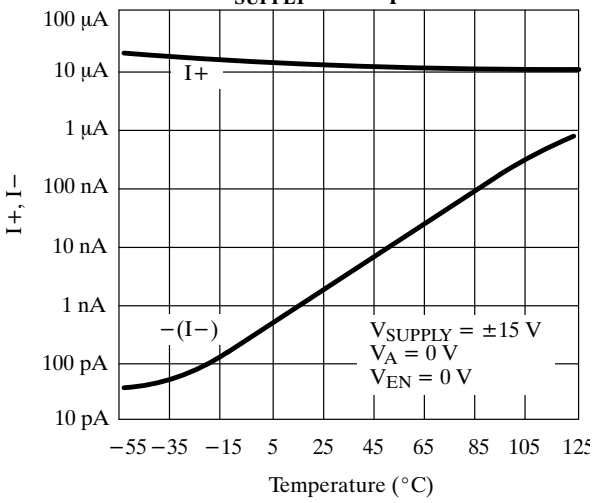


Typical Characteristics (Cont'd)

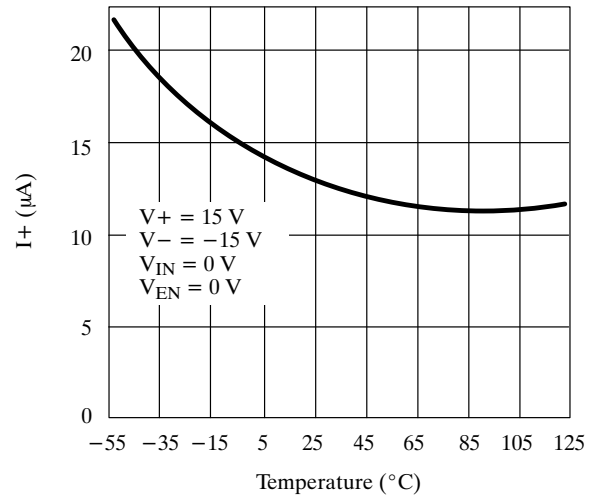
Positive Supply Current vs. Switching Frequency



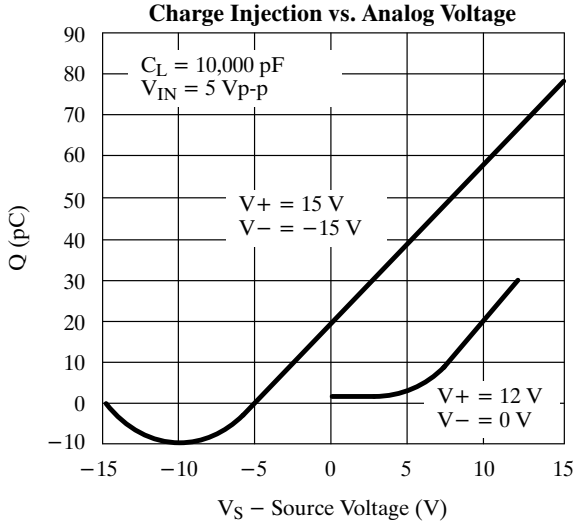
I_{SUPPLY} vs. Temperature



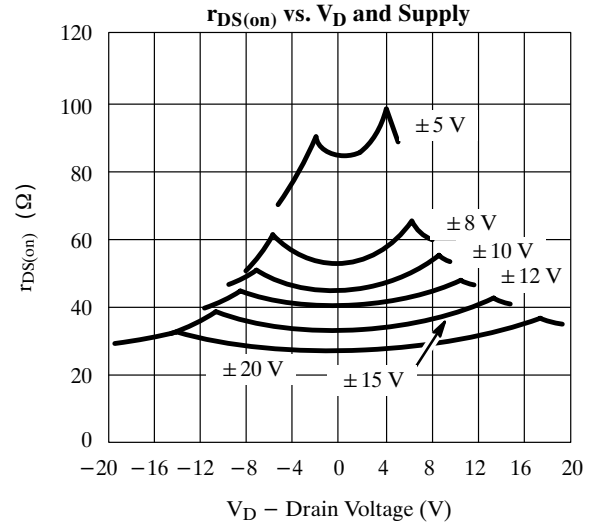
Positive Supply Current vs. Temperature (DG408)



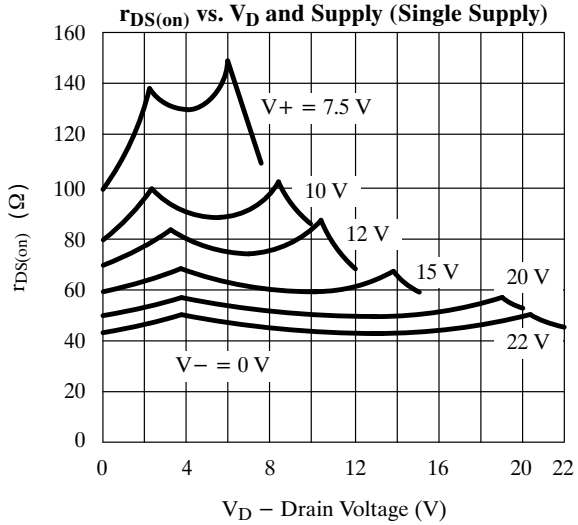
Charge Injection vs. Analog Voltage



$r_{DS(on)}$ vs. V_D and Supply

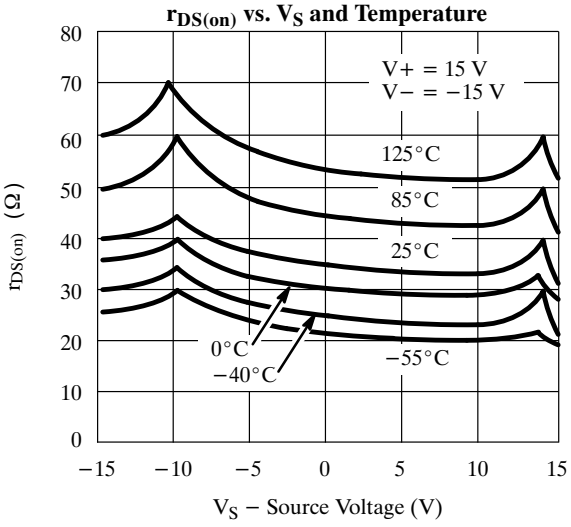


$r_{DS(on)}$ vs. V_D and Supply (Single Supply)

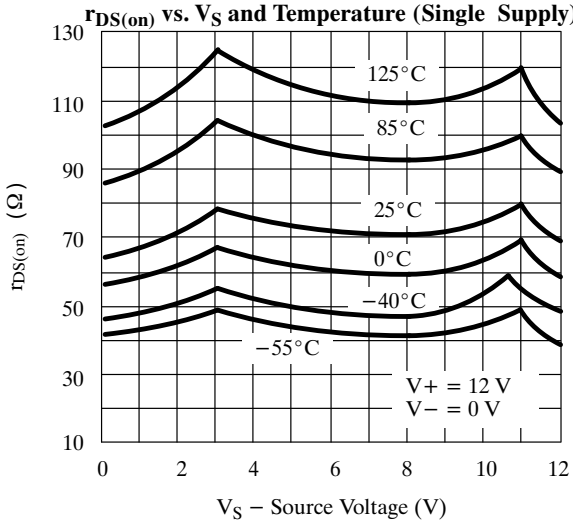


Typical Characteristics (Cont'd)

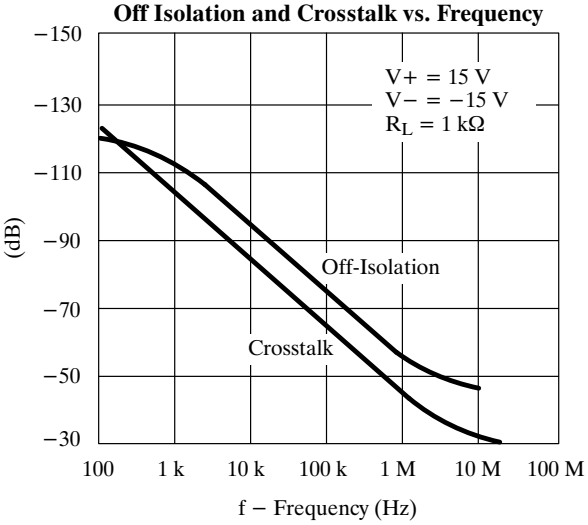
$r_{DS(on)}$ vs. V_S and Temperature



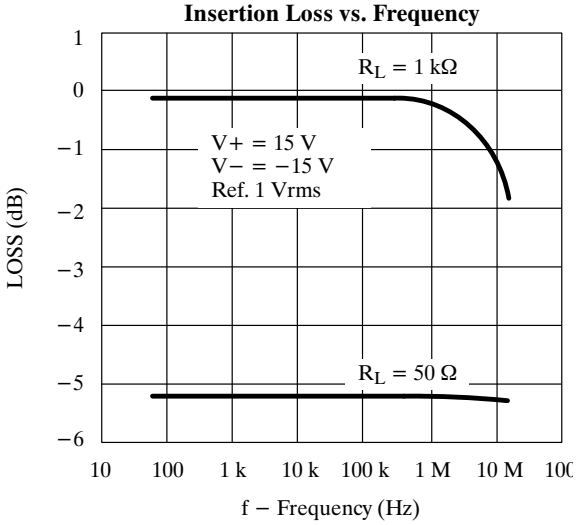
$r_{DS(on)}$ vs. V_S and Temperature (Single Supply)



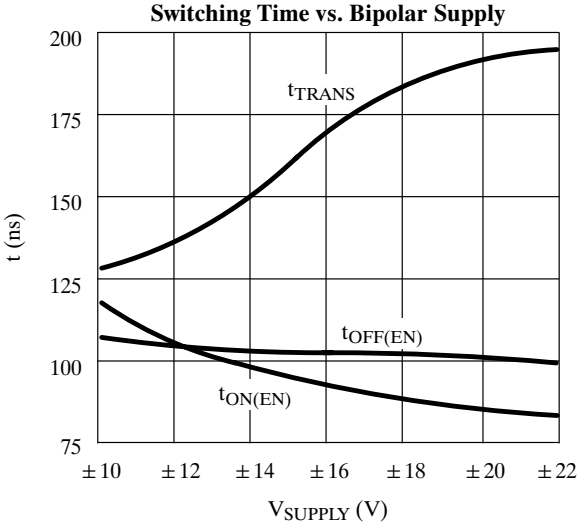
Off Isolation and Crosstalk vs. Frequency



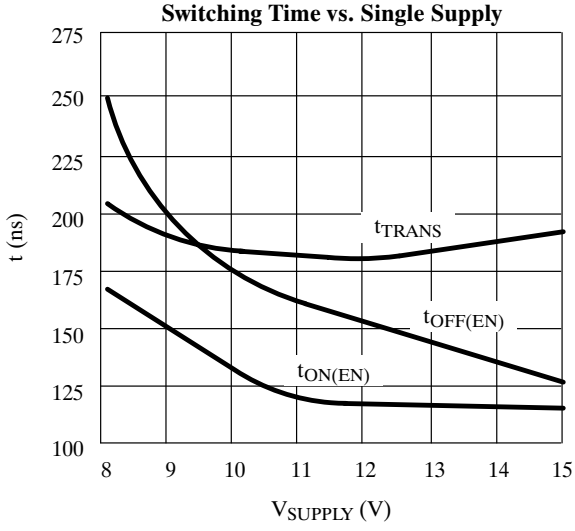
Insertion Loss vs. Frequency



Switching Time vs. Bipolar Supply



Switching Time vs. Single Supply



Schematic Diagram (Typical Channel)

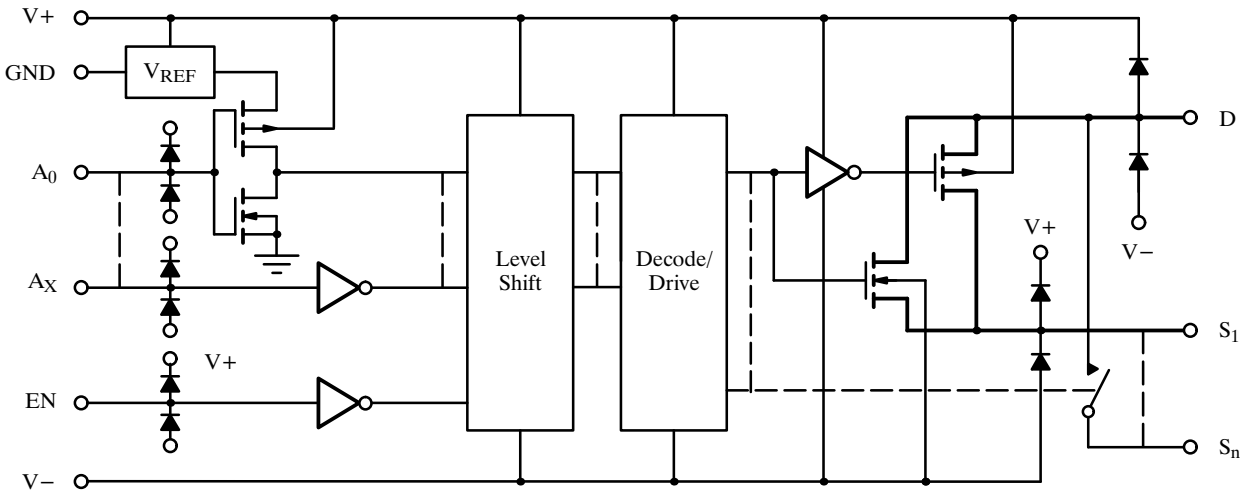
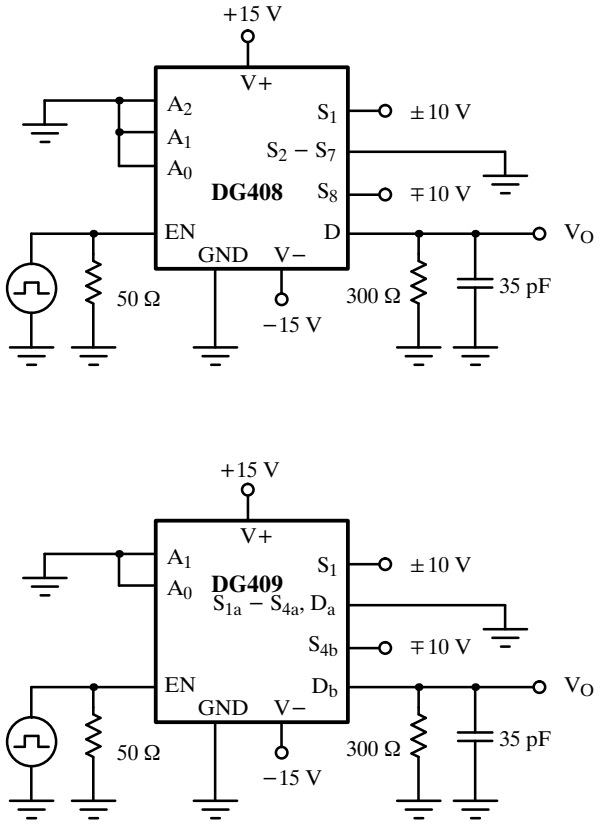


Figure 1.

Test Circuits



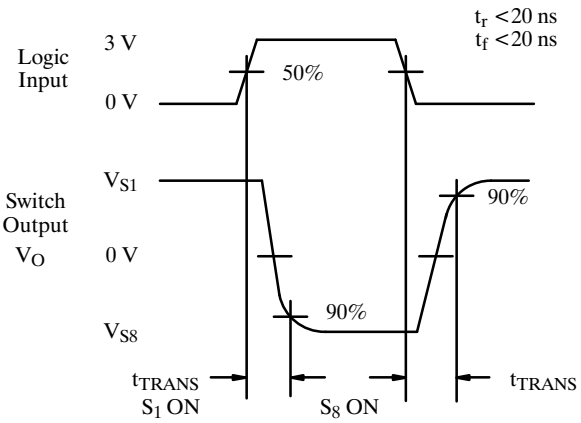


Figure 2. Transition Time

Test Circuits

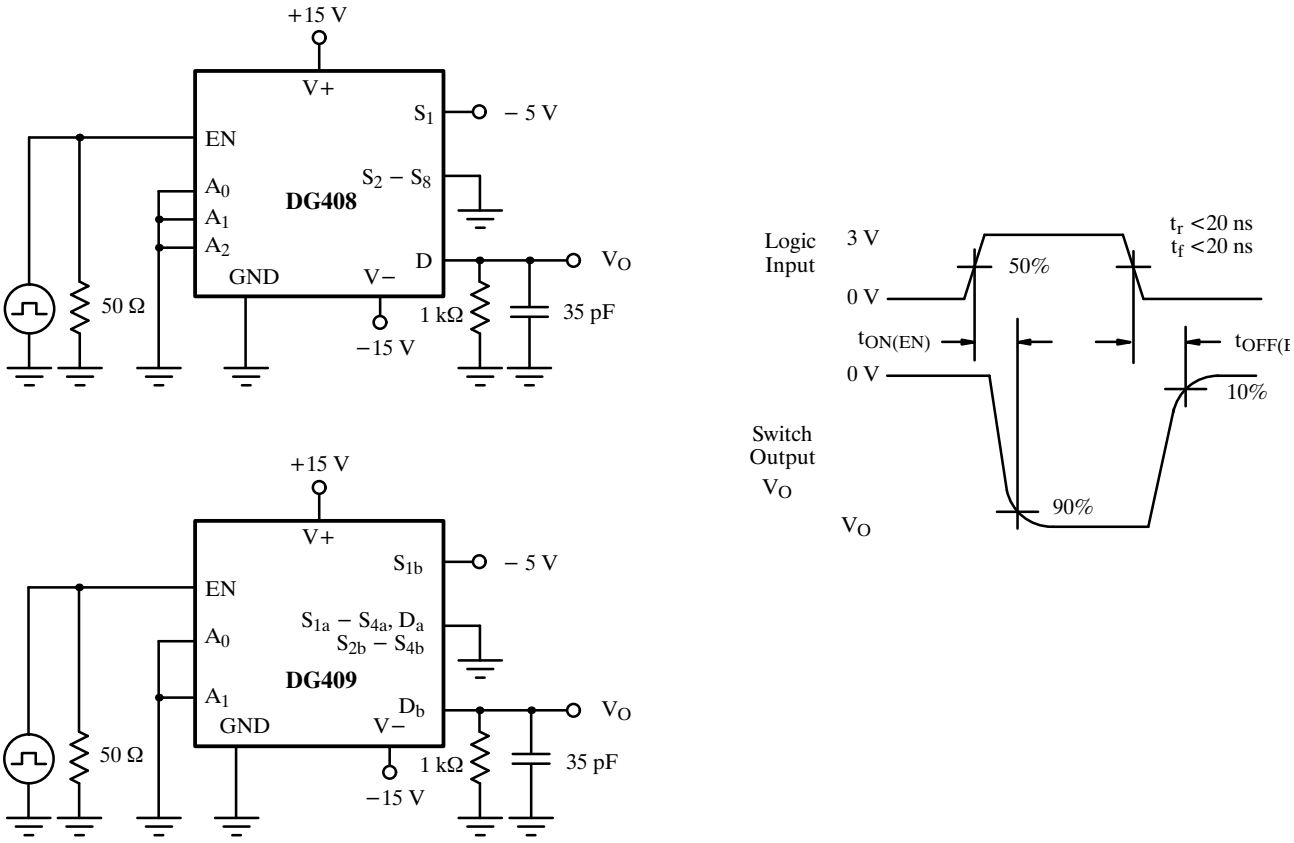


Figure 3. Enable Switching Time

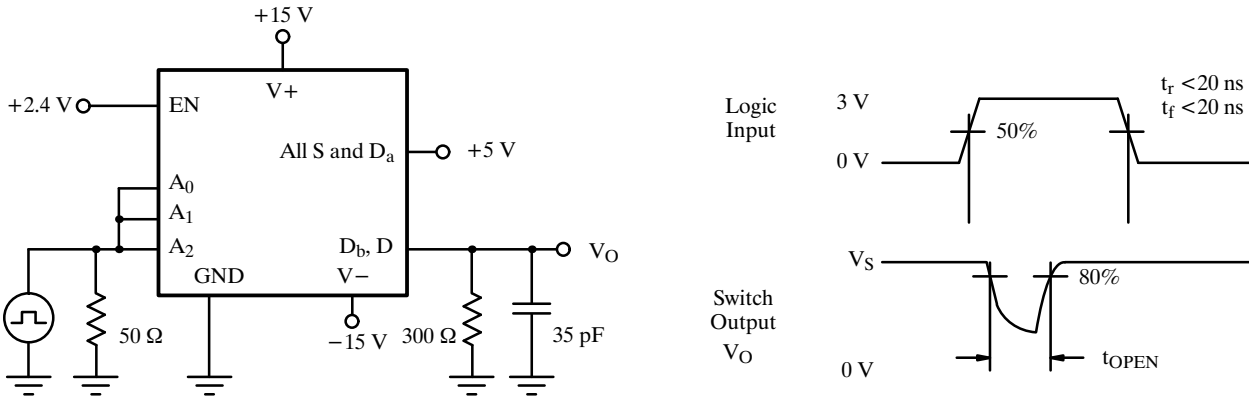


Figure 4. Break-Before-Make Interval

Test Circuits

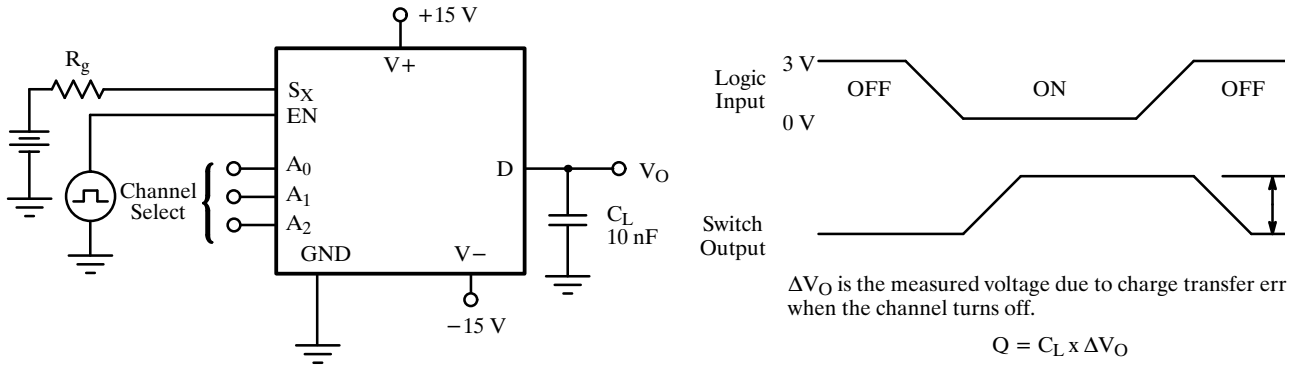


Figure 5. Charge Injection

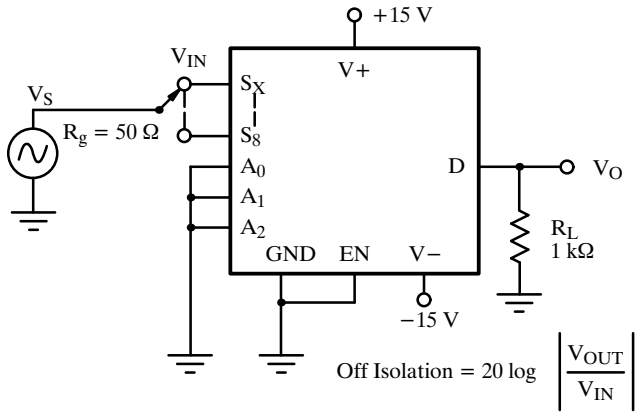


Figure 6. Off Isolation

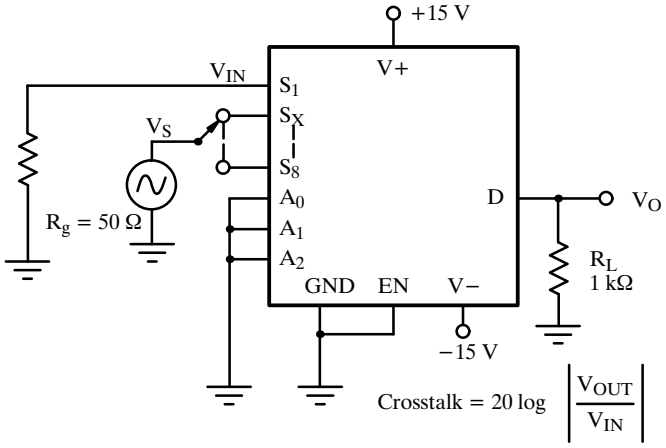


Figure 7. Crosstalk

Test Circuits

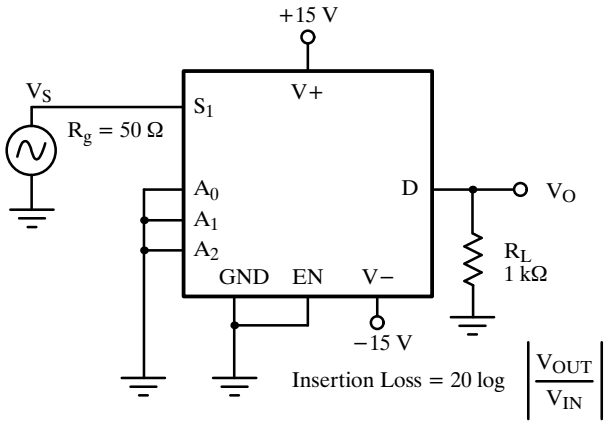


Figure 8. Insertion Loss

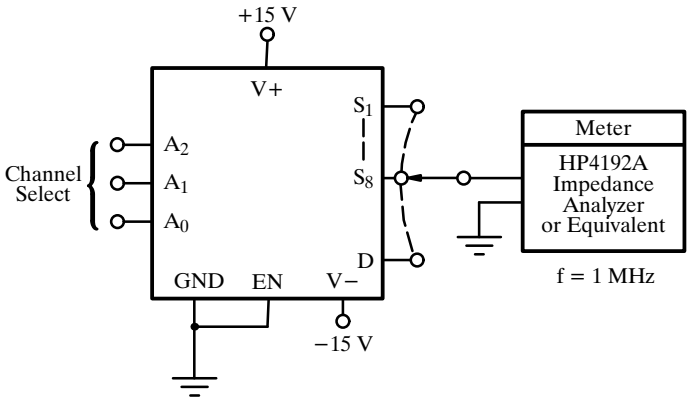


Figure 9. Source Drain Capacitance

Application Hints

Overvoltage Protection

A very convenient form of overvoltage protection consists of adding two small signal diodes (1N4148, 1N914 type) in series with the supply pins (see Figure 10). This arrangement effectively blocks the flow of reverse currents. It also floats the supply pin above or below the normal V+ or V− value. In this case the overvoltage signal actually becomes the power supply of the IC. From the point of view of the chip, nothing has changed, as long as the difference V_S − (V−) doesn't exceed +44 V. The addition of these diodes will reduce the analog signal range to 1 V below V+ and 1 V above V−, but it preserves the low channel resistance and low leakage characteristics.

Application Hints (Cont'd)

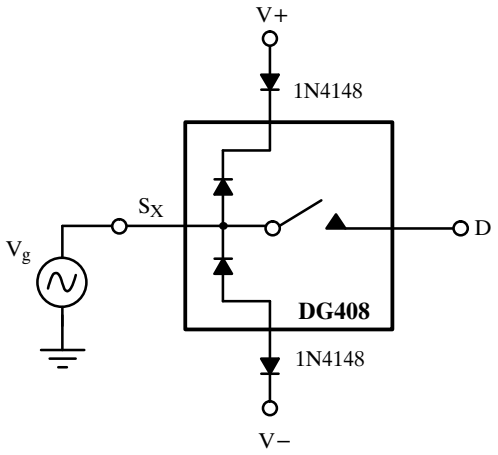
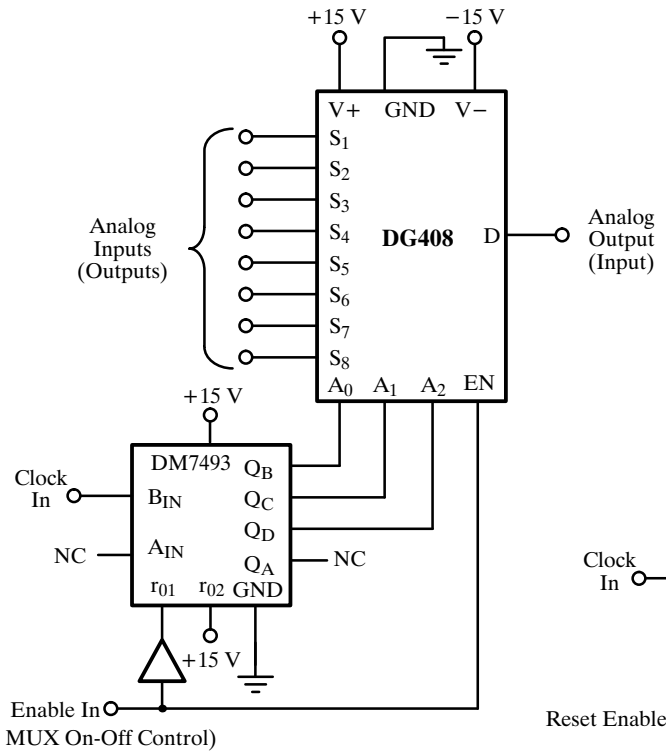


Figure 10. Overvoltage Protection Using Blocking Diodes

8-Channel Sequential Multiplexer/Demultiplexer



Differential 4-Channel Sequential Multiplexer/Demultiplexer

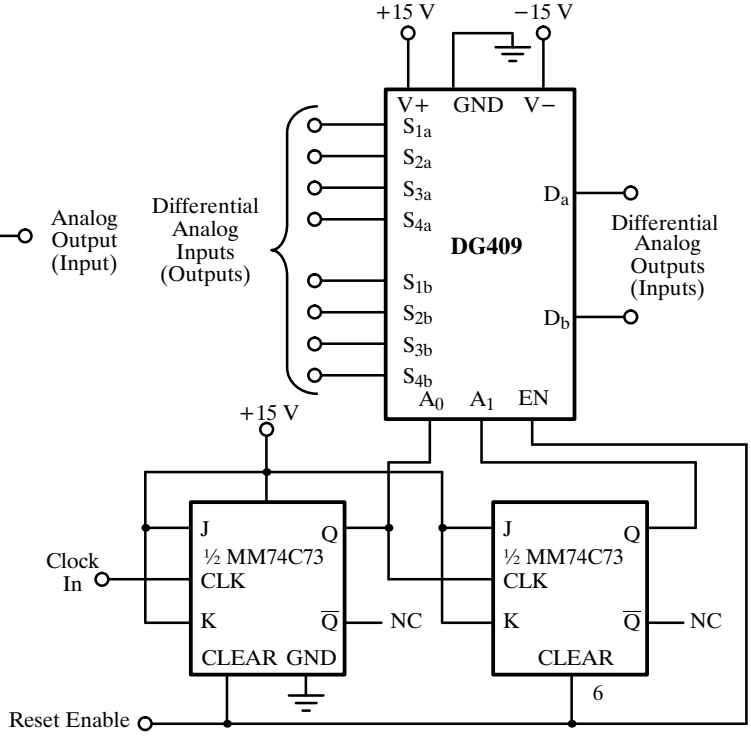


Figure 11.