Designing Low-Voltage DC/DC Converters with the Si9145

Bijan E Mohandes and Chae Lee

Introduction

The Siliconix Si9145 switchmode controller IC is designed to make dc-to-dc conversion smaller and more efficient in low-voltage, low-power applications such as portable cellular phones and other battery-operated equipment. Compared with conventional bipolar and BiCMOS devices, the Si9145 offers extremely low power consumption and propagation delay times, as well as operation down to very low voltages. Built on Siliconix' proprietary BiC/DMOS technology, the Si9145 features an operating voltage range from 2.7 V to 7 V, enabling the use of single-cell lithium ion (Li+) batteries, as well as 3- to 4-cell NiCd and NiMH batteries.
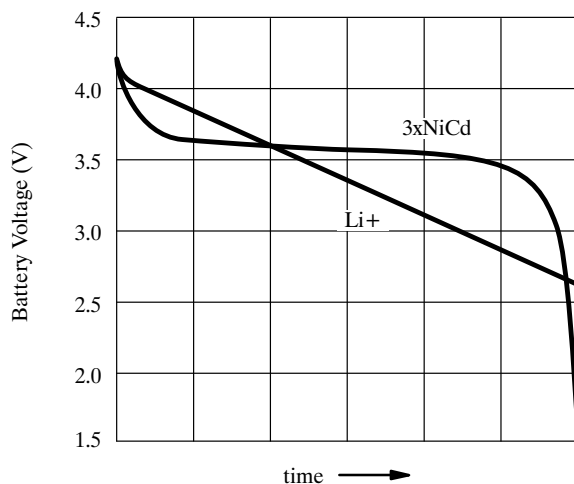

Figure 1. Discharge Comparison NiCd vs. Li+ (*)

An Overview of Lithium Ion Technology

Lithium ion batteries are becoming more readily available, and their introduction into consumer products such as camcorders and minidisk players will likely make lithium ion the technology of choice for the foreseeable future. Lithium batteries have several advantages over their nickel-based counterparts, including higher volumetric capacity, the absence of a memory effect, and built-in protection features supplied by the manufacturer. A single cell will produce an almost linear voltage discharge curve starting at 4 V and ending at around 2.9 V (Figure 1). The final discharge value varies by manufacturer. Compared with three NiCd batteries, however, there is a substantial voltage change over the operational platform of the battery. Presently most NiCd battery designs use a linear regulator, but with the new Li+ batteries, this would yield a substantial drop in the efficiency of the system. The Li+ battery will require a high-efficiency switchmode regulator solution to maintain all of its benefits.

Commonly Used DC/DC Topologies

There are numerous types of dc-to-dc converters, but most practical designs are variations of the Buck or boost topologies. The Si9145 has been configured so that the most popular conventional topologies, including Buck, synchronous Buck, and boost can be easily implemented.
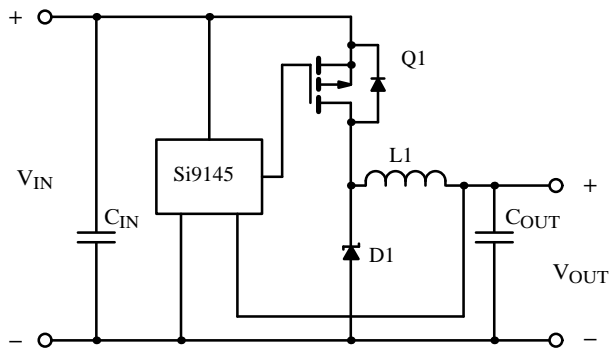
(01/12/95)

Figure 2. Buck Converter

The Buck converter (Figure 2) produces output voltages lower than the input, using a high-side switch (Q1). During the conduction time, current flows through Q1 and L1, and during the OFF time, current flows through D1 and L1, thus maintaining a continuous current.

The synchronous Buck converter (Figure 3) is identical to the Buck converter, except that a MOSFET is used to replace the rectifier. This substitution allows higher efficiencies, as well as a continuous current, even down to virtually no load.

The Boost Converter (Figure 4) is used when a higher voltage than the input is required at the output. This result is obtained by allowing energy to be stored in L1 during the ON time of Q1 and by allowing the voltage polarity of L1 to reverse during the OFF time, thus raising the voltage above V_{IN}.

Functional Description of the Si9145

Where extremely low voltages are used and high efficiencies are required, it is not practical to measure extremely low voltages across sense resistors. Therefore, the Si9145 uses voltage mode control. The Si9145 (Figure 5) is configured for operation at high frequencies, typically between 200 kHz and 1MHz, where small energy storage components (magnetic and capacitive) are required. Operation at 1 MHz allows the use of small-outline surface-mount capacitors and inductors, which keep size and volume to a minimum.

The Si9145's pin configuration allows separation of its noisy load switching sections from its low-noise analog parts.
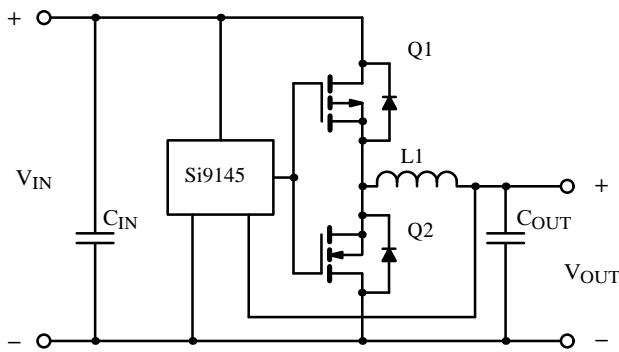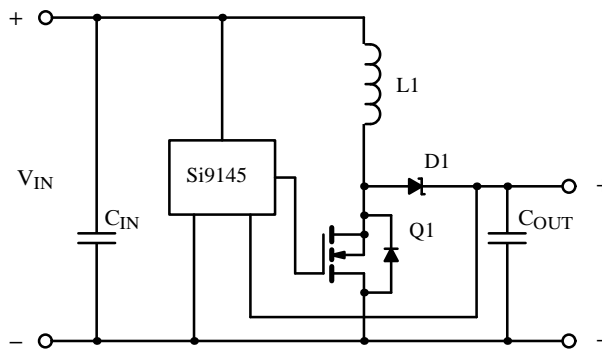
Figure 3. Synchronous Buck Regulator

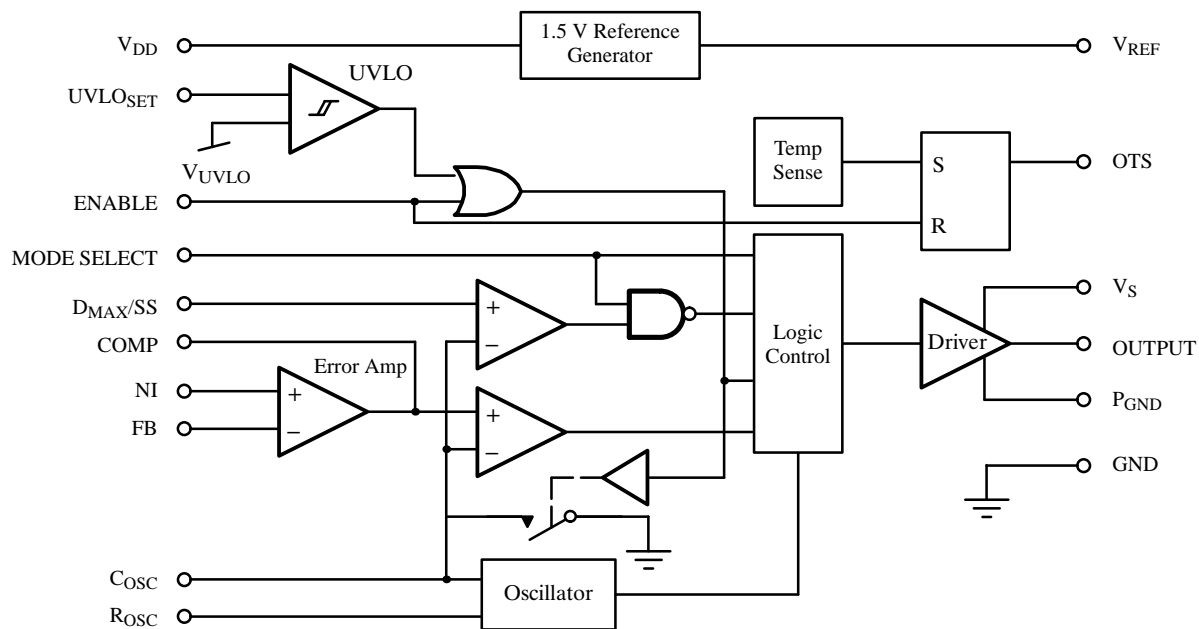**Figure 4.** Boost Converter

Figure 5. Si9145 Block Diagram

Pin 1: V_{DD}

This is the supply pin for the low-noise analog section. It should be well decoupled and separated from the V_s power pin. Good decoupling close to GND (pin 8) is recommended.

Pin 2: MODE Select

This pin allows the polarity of the output driver to be changed, to accommodate both n- and p-channel drives, as well as enabling the operation of the D_{MAX} pin (pin 3). When connected to GND, the D_{MAX} pin is disabled, allowing 100% duty cycle, and inverted output drive, suitable for p-channel MOSFETs, as would be the case in a Buck regulator.

When connected to V_{DD}, the duty cycle can be programmed by pin 3, and the output driver is configured for low-side drive of n-channel MOSFETs. This mode is suitable for boost regulators, and flyback/forward transformer isolated types, where duty cycle limitation prevents loop instability and core saturation.

Pin 3: D_{MAX}/SS

This pin allows the maximum duty cycle to be set between 0 and 100%. Below 1 V, the duty cycle is 0%, and above 1.5 V it is 100%. Users can program the exact value using a divider on this pin. In addition, soft start can be achieved by placing a capacitor in parallel with the lower divider in circuits where D_{MAX} is not

28

connected to GND. This adds a time constant to the duty cycle during start-up.

Pins 4, 5, and 6: Comp, FB, and NI

These pins are the three connections to the error amplifier. The error amplifier uses a PNP bipolar input differential stage and has a complementary NPN/PNP output driver stage.

The high frequency capability of the error amp is exceptional due to the characteristics of the BCD process used. The unity gain bandwidth (Figure 6) of the error amplifier is around 20 MHz, from 3 V to 5 V.
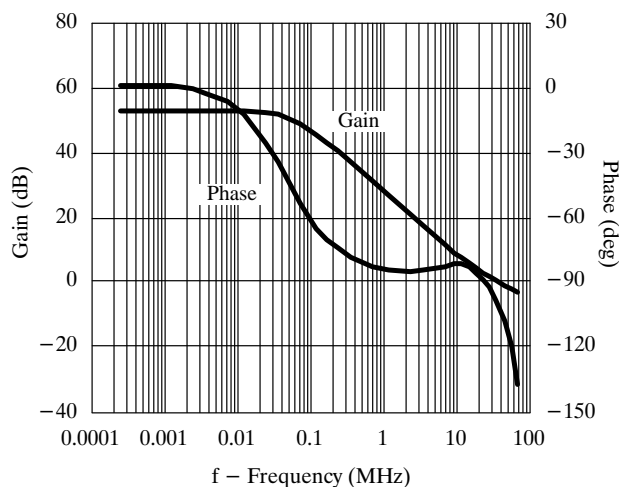

Figure 6. Si9145 Unity Gain Bandwidth and Phase

$$F_{SW} = \frac{0.9}{R_t \ x \ C_t} \tag{1}$$

This type of oscillator is difficult to synchronize. To obtain a true free running mode that can lock onto an available signal, a spike needs to be superimposed on top of the triangle ramp to pre-trigger the circuit. (Figures 7 and 8.)

Buffers 1, 2, and 3 generate a very short spike (dependent on propagation delay on the logic used) which drives Q1 on to superimpose a spike onto C_t. The spike duration should be kept to minimum, to avoid dissipating power in R1.

The oscillator frequency can be shifted to a lower value to minimize power consumption in light mode by changing the current in the timing resistor R_T with an external MOSFET (Figure 9). In normal operation Q1 is on and therefore reverse biases D1, preventing

Pin 7: V_{REF}

The internal 1.5-V band gap reference is trimmed to $\pm 1.5\%$ internally. A minimum 100-nF capacitor is recommended for de-coupling.

Pin 8: GND

This pin is the analog ground pin for all the noise sensitive functions (pins 1 through 7), and should be well decoupled with V_{DD}.

Pins 9 and 10: R_{OSC}, C_{OSC}

These pins are used to select the oscillator frequency of operation. The frequency of the oscillator is set by the value of the R_T resistor which sets the value of the current mirror that charges the timing capacitor C_T. It is recommended that capacitor values below 47 pF not be used, as stray capacitance and packaging manufacturing tolerance will affect the value selected. The frequency of operation can be calculated from the following equation:

current from R1 flowing through R_T. When Q1 is open, D1 allows the mirrow current set by R_T to be altered, thus changing the frequency.

From this data (Table 1), it can be clearly seen that the improvement in efficiency at light load, for example in a sleep mode, would be significant. The current taken from $+V_{IN}$ has not changed significantly. But V_S, which drives the MOSFET and the output stage, has a significant reduction. This means that for a converter running in normal mode, the efficiency at light load may increase dramatically: from less than 50% to more than 75%, depending on other frequency losses in the circuit. The output ripple will change, as the parameters that define it have changed, but in this case the increase is acceptable.
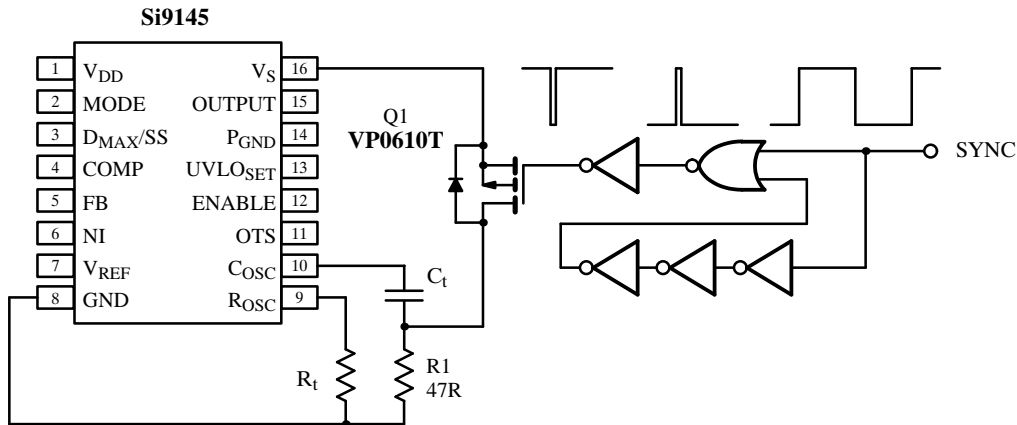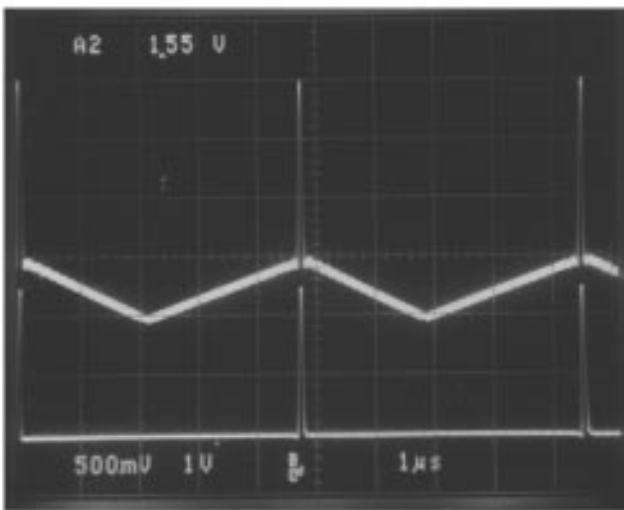
Figure 7. Synchronization to an External Source
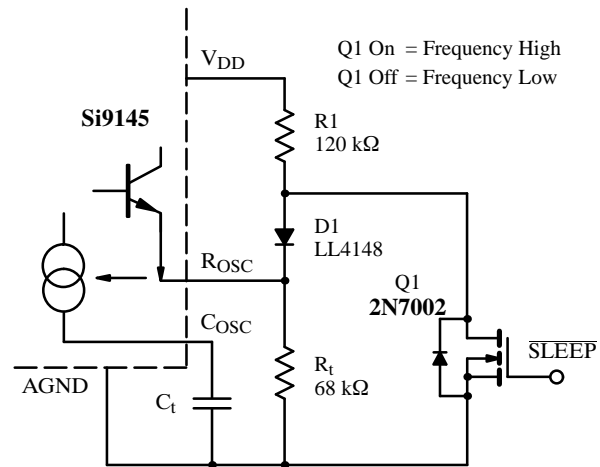

Figure 8. Oscillator Synchronization

Figure 9. Frequency Shifting the Oscillator

Table 1

	$F_{OSC} = 1$ MHz	$F_{OSC} = 150$ kHz
$+V_{IN}$ Current (mA)	1.28	0.94
V_S Current (mA)	34.2	3.94
Total Current (mA)	35.48	4.88
Total Power from 5 V Input (mW)	177	24.4
Percentage of Output Power*	**118**	**16.3**
Output Ripple (mV)	35.5	43

*Taken with output power in sleep mode (35 mW).

Pin 11: $\overline{\text{OTS}}$

This pin is used to indicate an internal overtemperature shutdown. The internal integrated sensor detects excessive die temperature and latches this pin low in the event of overtemperature. Normally this pin is connected to the enable pin to allow shutdown in the event of overtemperature. Overtemperature will most likely be encountered in the event of a short circuit failure of one or both of the devices being driven from the output driver.

(01/12/95)

Pin 12: Enable

The enable pin should be pulled high in normal operation. Pulling this pin down stops operation of the chip and allows reduce consumption mode. This pin is normally configured with the $\overline{OTS}$ pin (see pin 11).

Pin 13: UVLO$_{set}$

The UVLO pin is used to determine the circuit's cut-off point of operation in the event of a low-voltage input. This function prevents excessive discharging or damage to batteries. The internal 1.2-V reference is compared with this pin, and a built in 200-mV hysteresis prevents oscillations close to the threshold of operation. This might be encountered with high-impedance sources, such as a battery at its end-of-charge.

Pins 14, 15, 16: PGND, Output, V$_S$

These pins are the three connections to the output driver stage, supplying the output buffer. The output buffer is a complementary MOS type, with very fast transition times and extremely low output impedance. It is also capable of generating noise in the area close to the chip. Access to pins 14, 15, and 16 allows proper decoupling and can minimize supply and return current paths to the load being driven. The output driver transition time is fast enough to drive a pair of complementary MOSFETs directly with common gate connections, while maintaining very low shoot-through current. Significant improvements in efficiency can be achieved by using an external break-before-make circuit, (see Figure 10). Using this circuit, efficiencies of better than 90% can be obtained with proper MOSFETs. It is important not to oversize the MOSFET(s) being driven for the application required. Using a larger, lower on-resistance MOSFET will not necessarily produce a better result.
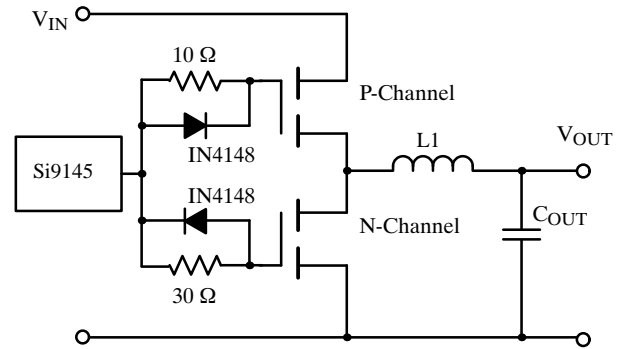

Figure 10.

The output driver of the Si9145 has been optimized for driving low on-resistance MOSFETs in the Siliconix LITE FOOT™ and LITTLE FOOT® series. The recently introduced LITE FOOT series offers similar or better performance to the LITTLE FOOT while using the smaller TSSOP outline. Changes introduced in the lead connections in the LITE FOOT have allowed the creation of low-voltage, low-gate threshold devices that can be used in low-profile, small-surface area power converters.

To design a highly efficient dc-to-dc converter, several parameters need to be considered:

- Required minimum efficiency. Usually 80 to 95% is achievable, with the higher efficiency occurring with the lowest switching frequency, and the lowest input to output voltage differential.
- Conduction losses caused by the current switching through the on-resistance of the MOSFETs.
- Gate drive losses caused by the turn ON and turn OFF gate charge (Qg) of both devices by the Si9145.
- Output capacitance losses caused by each MOSFET conducting and shorting out its own output capacitance.
- The input and output voltage ripple that appears on the input and output capacitors will be determined by the quality of the capacitor used. In experimental tests, large variations were encountered from manufacturer to manufacturer and from different series. Good, low-ESR and -ESL (Equivalent Series Resistance and Inductance) devices should be selected. In boost converters, due to the discontinuous nature of energy transfer, even higher peak currents will be encountered, which

will in turn generate higher ripple without lower ESR resistances.

- Board layout is critical to performance. Design methodology should include the minimization of all switching current paths as well as separated signal and power grounds, with single point connections.

The following design examples illustrate the types of converter that can be easily designed with the Si9145.

Design Example 1

5-V to 3-V @ 300 mA Buck Converter

Assume the following design specification:

V_{IN} (V) = 3 to 5 V dc

V_{OUT} (V) = 3 V dc

F_{SW} (MHz) = 1 MHz

I_{OUT} (A) = 0.3 A

$$\delta_{Pchannel} = \frac{V_{OUT}}{V_{IN}} \tag{2}$$

and

$$\delta_{Nchannel} = \frac{V_{IN} - V_{OUT}}{V_{IN}} \tag{3}$$

For conduction losses in the worst possible case, the temperature coefficient of a MOSFET operating at 100°C will be approximately 1.4. The required

$$r_{DS(on)P} = \frac{V_{IN} \times P_{LOSS}}{V_{OUT} \times I_{MAX}^2 \times 1.4} \tag{4}$$

and for the N channel device,

$$r_{DS(on)N} = \frac{V_{IN} \times P_{LOSS}}{(V_{IN} - V_{OUT}) \times I_{MAX}^2 \times 1.4} \tag{5}$$

Assuming that the conduction power losses of each MOSFET will be equal to 25% of the total losses at full

$$P_O = V_{OUT} \times I_{OUT} = (3 \text{ V})(0.3 \text{ A}) = 0.9 \text{ W}$$

$$P_{IN} = \frac{P_O}{\eta} = \frac{0.9 \text{ W}}{0.85} = 1.06 \text{ W}$$

$$P_D = P_{IN} - P_O = 1.06 \text{ W} - 0.9 = 0.16 \text{ W}$$

$$P_{LOSS} = (0.25)(0.16 \text{ W}) = 0.04 \text{ W}$$

P_{OUT} (W) = 0.9 W

ΔI (mA) = 30

First, select the correct inductor value: (see Appendix A and C)

L_{OUT} = 40 mH

For highest efficiency, select the synchronous Buck topology, using n- and p- channel MOSFETs. In choosing the MOSFETs, remember that the device will be driven only from rail to rail. The device selected needs to have gate thresholds specified over the input operating voltage and be suitably sized to avoid excessive power loss due to gate drive and switching losses. A small Schottky diode D1 is used to prevent current flow through the body diode of the n-channel MOSFET and to avoid recovery time through this device. D1 only conducts current during the crossover time. It therefore dissipates virtually no power, as the n-channel device shunts D1 when it is fully enhanced.

For the synchronous Buck regulator, the conduction duty cycles of the n- and p-channel devices are:

on-resistance, based on power dissipated for each device will approximately be:

load, then the losses of each device for an 85% efficient converter will be:

Then the on-resistance of each of the MOSFETs will need to be:

$$r_{DS(on)P} = \frac{V_{IN} \times P_{LOSS}}{V_{OUT} \times I^2_{MAX} \times 1.4} \qquad (6)$$

$$= \frac{5 \text{ V} \times 40 \text{ mW}}{3 \text{ V} \times (0.3 \text{ A})^2 \times 1.4}$$

$$= 0.529 \ \Omega$$

and for the N channel device

$$r_{DS(on)P} = \frac{V_{IN} \times P_{LOSS}}{(V_{IN} - V_{OUT}) \times I^2_{MAX} \times 1.4} \qquad (7)$$

$$= \frac{5 \text{ V} \times 40 \text{ mW}}{(5 \text{ V--}3 \text{ V}) \times (0.3 \text{ A})^2 \times 1.4}$$

$$= 0.794 \ \Omega$$

The total gate charge losses of the MOSFET need also to be considered. If the gate charge losses of both devices were equal to half of the full load conduction

$$P_{QGTOT} = V_{IN} \times I_{QGTOT} \qquad (8)$$

$$= V_{IN} \times F_{OSC}(Qg_P + Qg_N)$$

then

$$(Qg_P + Qg_N) = \frac{P_{QGTOT}}{V_{IN} \times F_{OSC}} = \frac{20 \text{ mW}}{5 \text{ V x 1 MHz}}$$

$$= 4 \text{ nC}$$

Ideally, n- and p-channel devices with 2 nC each should be selected.

A complete schematic of a 5-V to 3-V converter is shown in Figure 11. In this circuit example, the Si9145's power consumption was measured at 974 μA.

Loop Stability

To optimize the stability of the loop, the

losses, then these would be approximately 20 mW. The required gate charges would be determined from:

POWER456[2] software was utilized.

The data parameters for the Buck converter stage were entered and the resulting loop compensation components were extracted. For a manual detailed analysis of voltage mode loop stability should review Siliconix application note AN710[3].

Figure 11. Complete Buck Regulator Schematic
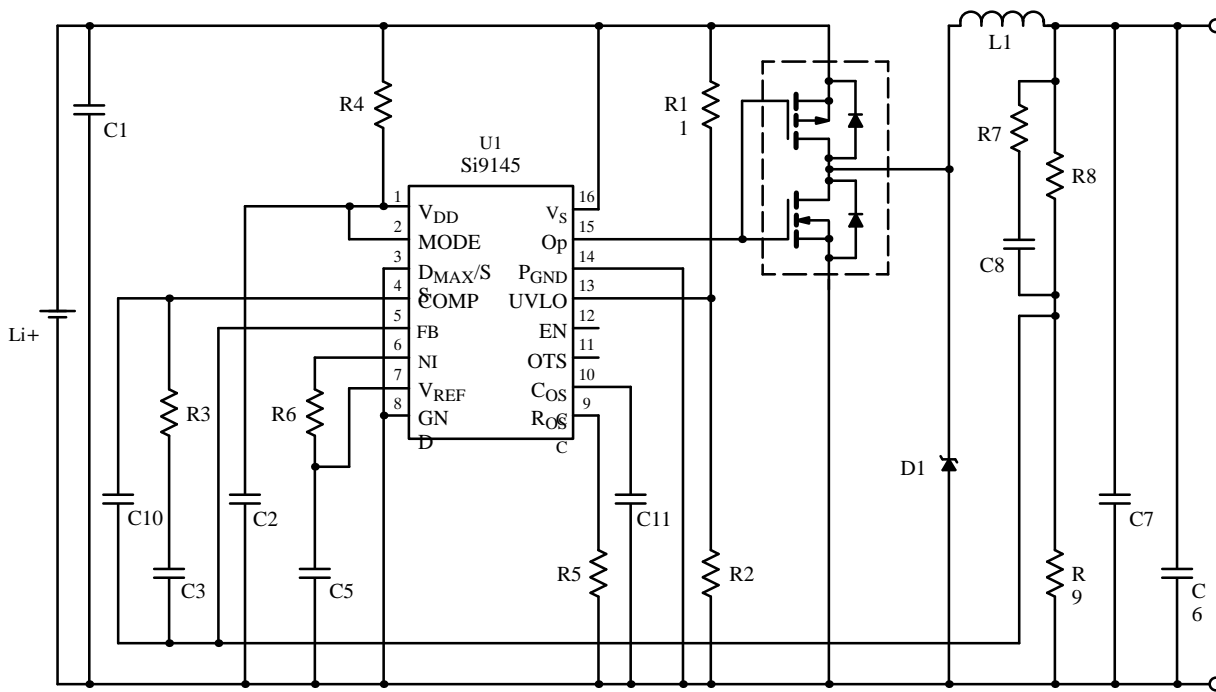
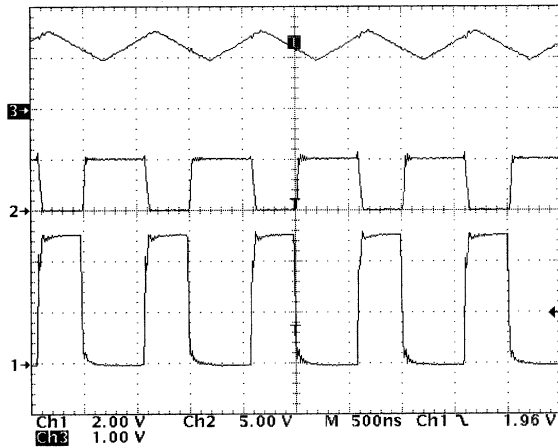Note: See Appendix D for component specifications

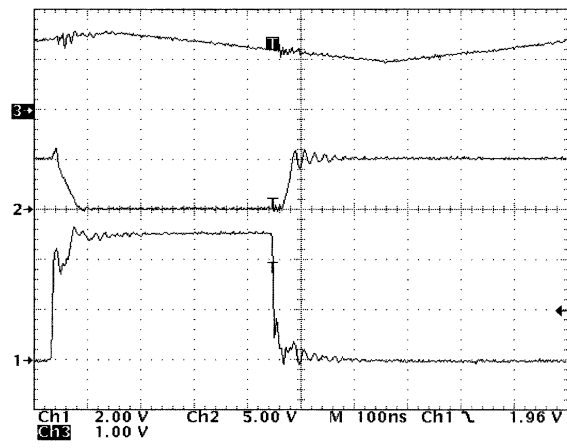**Figure 12.** Synchronous Buck Switching Waveforms

Figure 13. Synchronous Buck Switching Waveforms (Expanded)

Figure 12 shows the converter switching waveforms. The middle trace shows the input voltage node to the choke, which is also the common drain of both MOSFETs. The bottom trace shows the common gate connection of both MOSFET.

Figure 13 shows the same waveforms but greatly expanded, showing the rise and fall times of the output driver. The effect of noise is clearly apparent on the timing capacitor waveform.

34

(01/12/95)

Design Example 2

3-V to 6-V @ 500 mA Continuous Boost Converter

Assume the following Design specification:

V_{IN} (V) = 3 to 5 V dc

V_{OUT} (V) = 6 V dc

F_{SW} (MHz) = 1 MHz

I_{OUT} (A) = 0.1 to 0.5 A

P_{OUT} (W) = 0.6 to 3.0 W

Target Efficiency (η%) = 88%

First , select the correct inductor value (see Appendix B and C):

$$P_{LOSS} = I^2_{RMS} \times r_{DS(on)} \qquad (9)$$

Therefore, the MOSFET will need to have an on-resistance of:

$$r_{DS(on)} = \frac{P_{LOSS}}{I^2_{RMS}} = \frac{0.164 \text{ W}}{(0.842 \text{ A})^2} = 0.231 \ \Omega \qquad (10)$$

Allowing for worst case heating effect, a factor of 1.4 must be added to obtain a data sheet specification of 231/1.4 = 165 mΩ. It is important to remember that this value needs to be specified for operation with the input voltage to the Si9145, as this is the only source

Ipeak = 1.296 A equivalent to Irms = 0.842 A

L = 4.7 μH

Assume that the MOSFET conduction losses will represent 40% of the total losses and that the V_{D1} of the Schottky diode is 0.3 V.

Total losses:

$$P_T = \frac{P_{OUT(MAX)}}{\eta} - P_{OUT(MAX)}$$

$$= \frac{3.0 \text{ W}}{0.88} - 3.0 \text{ W} = 0.409 \text{ W}$$

The power dissipated by the MOSFET will be:

for the gate drive. In this case, it would be advisable to select a device with this on-resistance rated at 2.7 V V_{GS} to allow for other losses in series (such as output stage and tracking losses).
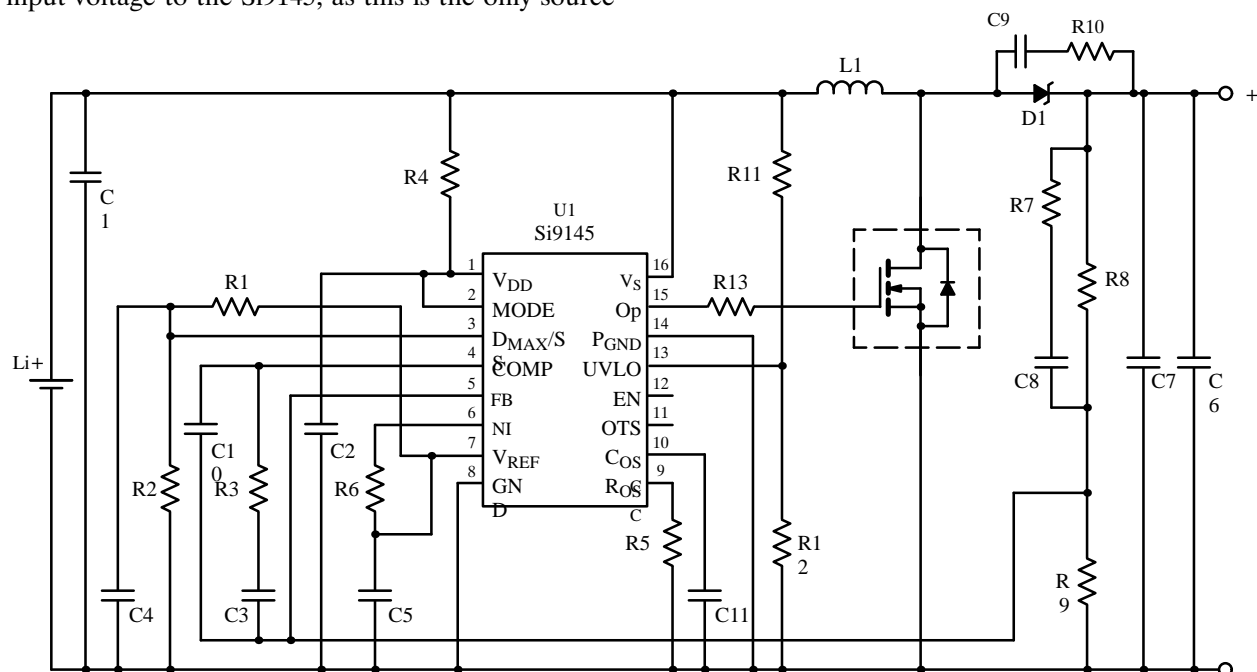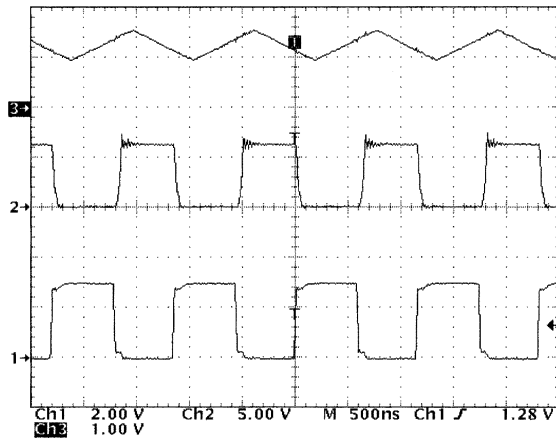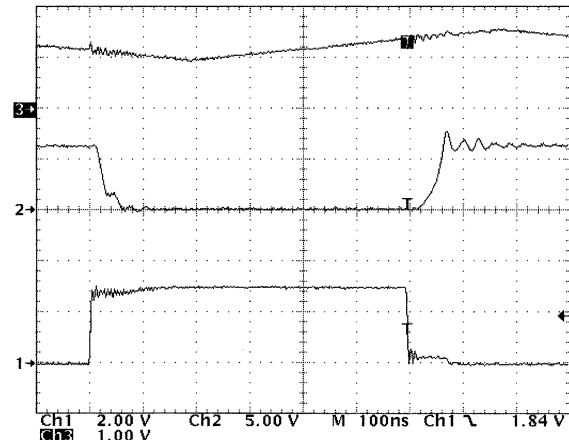
Figure 15. Boost Switching Waveforms

Figure 16. Boost Switching Waveforms (Expanded)

The gate charge losses should also be considered. In the case of the boost converter, the drain of the MOSFET is switched to the same voltage as the output (ignoring diode voltage drop). If the gate charge losses of the MOSFET were equal to half of the full load

$$Q_{gN} = \frac{P_{QG}}{V_{IN} \times F_{OSC}} = \frac{82 \text{ mW}}{(5 \text{ V}) \times 1 \text{ MHz}} = 16 \text{ nC} \quad (11)$$

Ideally, an n-channel device with less than 16 nC gate charge should be selected. A complete schematic of a 3-V to 6-V converter is shown in Figure 14. The

conduction losses, then these would be approximately 82 mW.

The required gate charge would be determined from:

waveforms in Figure 15 and Figure 16 show typical results obtained.

References

1. Mohandes, Bijan. 1993. "Designing High Frequency DC-to-DC Converters with the Si9114." Siliconix Application Note.

2. Riddley, Ray. 1992. POWER 456 - Power Supply Simulation Software. [Riddley Engineering, 152 Jacaranda Drive, Battle Creek, Michigan 49017]

Tel:+1-616-962-1181, Fax:+1-616-962-1180.

3. Blattner, Robert. 1992. "High Efficiency Buck Converter for Notebook Computers." Siliconix Application Note AN710.

4. McLymann, Colonel Wm. "Designing Magnetic Components for High Frequency dc-dc Converters", Kg Magnetics, ISBN #1-883107-00-8
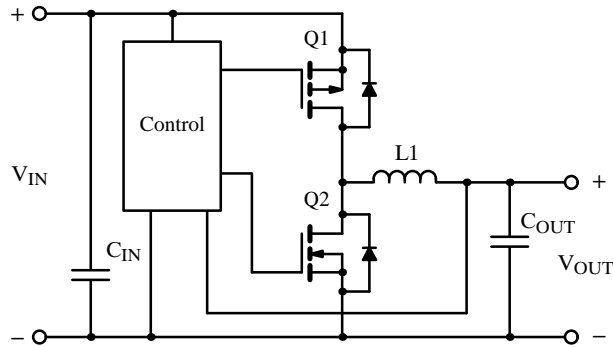
5.Coilcraft , Cary, Illinois, IL60013, USA,

In USA: Tel:+1-708-639-6400, Fax:+1-708-639-1469

In Europe: Tel:+44-236-730595, Fax:+44-236-730627

In Hong Kong: Tel:+852-770-9428, Fax:+852-770-0729

Appendix A: Buck Converter Inductor Design

Specification requirements:

Input Voltage (V_{IN}) = 3 V_{MIN}, 4 V_{MAX} dc

Output Voltage (V_{OUT})= 3 V dc

Switching Frequency (F_{SW}) = 1 MHz

$$V_L = L \times \frac{di}{dt}$$

where V_L is the voltage across the inductor.

At maximum input voltage the voltage across the inductor is:

$$L = \frac{(V_{IN} - V_{OUT}) \times T_{ON}}{\Delta I_L}$$

Assuming that the Q1 and Q2 are ideal components, then at maximum input voltage the duty cycle will be:

$$\delta_{MIN} = \frac{V_{OUT}}{V_{IN}}$$

In this case,

$$\delta_{MIN} = \frac{V_{OUT}}{V_{IN}} = \frac{3 \text{ V}}{5 \text{ V}} = 0.6$$

Therefore,

$$T_{ON} = \frac{\delta_{MIN}}{F_{SW}} = \frac{0.6}{1 \text{ MHz}} = 0.6 \text{ μs}$$

Then

$$L = \frac{(V_{IN} - V_{OUT}) \times T_{ON}}{DI_{OUT}}$$

$$(5 \text{ V} - 3 \text{ V}) \times 0.6 \text{ μs}$$

Output Current (I_{OUT}) = 300 mA

Ripple Current (DI_{OUT}) = 30 mA pk-pk

Ripple Voltage (DV_{OUT}) = 30 mV pk-pk

From basic electrical circuit theory, the voltage across an inductor is given by:

$$V_L = V_{IN} - V_{OUT} \text{ and } di = \Delta I_L$$

Therefore

The value of the capacitor required for the output ripple needs to be:

$$C_{OUT} = \frac{\Delta I_{OUT}}{8 \times F_{SW} \times \Delta V_{OUT}}$$

$$C_{OUT} = \frac{30 \text{ mA}}{8 \times 1 \text{ MHz} \times 30 \text{ mV}} = 0.125 \text{ } \mu F$$

To ensure that the ripple voltage is not exceeded, the ESR (Equivalent Series Resistance of the capacitor) needs to be less than:

$$ESR_{MAX} = \frac{\Delta V_{OUT}}{\Delta I_{OUT}} = \frac{30 \text{ mV}}{30 \text{ mA}} = 1 \text{ } \Omega$$

In practice, other factors such as ESL will also have an effect on the output ripple, as well as noise, and capacitors in the 1- to 10-μF range are more practical.

Appendix B: Continuous Boost Converter Inductor Design

$$T = \frac{1}{F_{SW}} = \frac{1}{1\ MHz} = 1\ \mu s$$

Next calculate the minimum and maximum output power:

$$P_{OUT(MIN)} = V_{OUT} \times I_{OUT(MIN)} = 6\ V \times 0.1\ A = 0.6\ W$$

$$P_{OUT(MAX)} = V_{OUT} \times I_{OUT(MAX)} = 6\ V \times 0.5\ A = 3.0\ W$$

Now calculate the maximum input current:

$$I_{IN(max)} = \frac{P_{OUT(MAX)}}{V_{IN(min)} \times \eta} = \frac{3.0\ W}{3\ V \times 0.88} = 1.136\ A$$

Calculate the minimum and maximum duty cycle:

$$\delta_{MIN} = \frac{V_{OUT} + V_{D1} - V_{IN(MAX)}}{V_{OUT} + V_{D1} - V_{DSQ1}} =$$

$$\frac{6\ V + 0.3\ V - 5.0\ V}{6\ V + 0.3\ V - 0.25\ V} = 0.215$$

$$\delta_{MIN} = \frac{V_{OUT} + V_{D1} - V_{IN(MIN)}}{V_{OUT} + V_{D1} - V_{DSQ1}} =$$

$$\frac{6\ V + 0.3\ V - 3.0\ V}{6\ V + 0.3\ V - 0.25\ V} = 0.545$$

Now calculate the minimum and maximum load resistance:

$$R_{MIN} = \frac{V_{OUT}}{I_{OUT(MAX)}} = \frac{6\ V}{0.5\ A} = 12\ \Omega$$

$$R_{MAX} = \frac{V_{OUT}}{I_{OUT(MIN)}} = \frac{6\ V}{0.1\ A} = 60\ \Omega$$

The minimum required inductance can now be calculated:

Specification requirements and design example:

Input Voltage (V_{IN}) = 3 V_{MIN}, 5 V_{MAX} dc

Output Voltage (V_{OUT})= 6 V dc

Switching Frequency (F_{SW}) = 1 MHz

Output Current (I_{OUT}) = 100 to 500 mA

Ripple Voltage (DV_{OUT}) = 60 mV (usually 10% of V_{OUT})

Target efficiency (η%) = 88%

First calculate the period of operation:

$$L \geq \frac{V_{IN}^2 \times \delta \times T \times \eta}{2 \times P_{OMIN}}$$

From the equation above, minimum inductance required to maintain continuous inductor current is a function of input voltage. Inductance versus input voltage is plotted in the graph below.
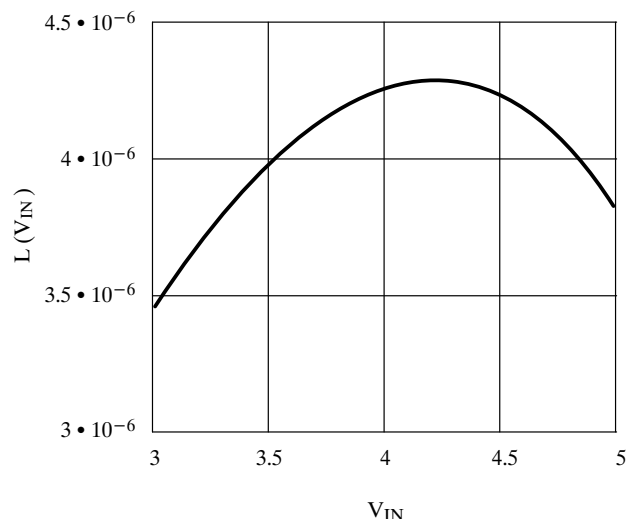
From the graph above, one can clearly see that the minimum inductance required to operate in continuous conduction mode throughout the entire 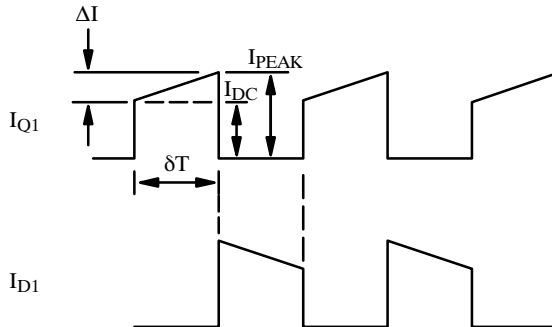input voltage range must be greater than 4.3 µH. An inductance value greater than 4.3 µH should be used to provide additional margin, 4.7 µH will be used in this example.

$$L = 4.7 \ \mu H$$

The peak current can now be determined under the worst case condition during minimum input voltage with maximum load.

$$\Delta I = \frac{(V_{IN(MIN)} - V_{DSQ1}) \ x \ \delta_{MAX} \ x \ T}{L}$$

$$= \frac{(3.0 \ V - 0.25 \ V) \ x \ 0.545 \ x \ 1 \ \mu s}{4.7 \ \mu H}$$

$$= 0.319 \ A$$

$$ESR_{MAX} \ = \ \frac{DV_{OUT}}{I_{PEAK}} \ = \ \frac{30 \ mV}{1.296 \ A} \ = \ 0.023 \ \Omega$$

To minimize the ESR effects, ceramic capacitors should be used.

$$I_{IN(MAX)} = I_{DC} + 0.5 \ x \ \Delta I$$

$$I_{DC} = I_{IN(MAX)} - 0.5 \ x \ \Delta I$$

$$I_{DC} = 1.136 \ A - 0.5 \ x \ 0.319 \ A$$

$$I_{DC} = 0.977 \ A$$

$$I_{PEAK} = I_{DC} + \Delta I$$

$$I_{PEAK} = 0.977 \ A + 0.319 \ A$$

$$I_{PEAK} = 1.296 \ A$$

From this, the RMS current can be calculated:

$$I_{RMS} \ = \ \sqrt{(I_{PEAK}^2 + I_{PEAK} \ x \ I_{DC} + I_{DC}^2) \ x \ \frac{\delta_{MAX}}{3}}$$

$$I_{RMS} \ = \ \sqrt{(1.296A^2 + 1.296A \ x \ 0.977A^2) \ x \ \frac{0.545}{3}}$$

$$I_{RMS} \ = \ 0.842 \ A$$

Output capacitance and ESR (equivalent series resistance) calculation:

Boost converter's output ripple voltage is determined by the output capacitance and ESR. Equal contribution of ripple voltage from capacitance and ESR will be assumed for this example.

$$C_{OUT} = \frac{I_{OUT} \ x \ \delta_{MAX} \ x \ T}{DV_{OUT}}$$

$$= \frac{(0.5 \ A)(0.545)(1 \ \mu sec)}{0.03 \ V} = 9.091 \ \mu F$$

Appendix C: Standard Inductor Selection[*]

Buck and boost inductors used in the design examples in this literature were selected from the Coilcraft "Surface-Mount Products" catalog. These devices are suggested for the benefit of designers. For further information contact Coilcraft.

Part Number	L at I_{DC} = 0 A (μH)	L at I_{DC} (μH)	IDC_{MAX} (mA)	DCR (mΩ)
DT3316-102	1.0	0.5	5.0	25
DT3316-152	1.5	0.7	5.0	30
DT3316-222	2.2	1.0	5.0	35
DT3316-332	3.3	1.5	5.0	40
DT3316-472	4.7	2.0	3.0	45
DT3316-682	6.8	4.0	2.5	50
DT3316-103	10	5.0	2.0	55
DT3316-153	15	6.0	1.8	60
DT3316-223	22	10	1.5	84
DT3316-333	33	12	1.3	90
DT3316-473	47	27	1.0	110
DT3316-683	68	40	0.9	150
DT3316-104	100	50	0.8	290
DT3316-154	150	80	0.6	360
DT3316-224	220	90	0.5	390
DT3316-334	330	150	0.4	730
DT3316-474	470	200	0.35	880
DT3316-684	680	300	0.3	1150
DT3316-105	1000	420	0.25	1450
DT1608-102	1.0	0.5	5.0	45
DT1608-152	1.5	0.7	5.0	50
DT1608-222	2.2	1.0	5.0	60
DT1608-332	3.3	1.5	5.0	70
DT1608-472	4.7	2.0	3.0	80
DT1608-682	6.8	4.0	2.5	85
DT1608-103	10	5.0	2.0	95
DT1608-153	15	6.0	1.8	135
DT1608-223	22	10	1.5	160
DT1608-333	33	12	1.3	275
DT1608-473	47	27	1.0	340
DT1608-683	68	40	0.9	575
DT1608-104	100	50	0.8	1100
DT1608-154	150	80	0.6	1400
DT1608-224	220	90	0.5	2250
DT1608-334	330	150	0.4	2900
DT1608-474	470	200	0.35	3600
DT1608-684	680	300	0.3	4550
DT1608-105	1000	420	0.25	8100

[*] This data is supplied for information purposes only. Siliconix does not recommend or endorse suppliers of components. Designers must determine the suitability of the data and the supplier for use in their applications.

AN715

Appendix D:
Figure 10 and Figure 14 Component Specifications

Figure 10: Synchronous Buck Converter	
C1	2.2 µF, 10 V
C2	0.1 µF
C3	0.01 µF
C4	N/A
C5	0.1 µF
C6	2.2 µF, 10 V
C7	100 nF
C8	2200 pF
C9	N/A
C10	N/A
C11	100 pF
R1	N/A
R2	N/A
R3	3.32 k
R4	100 R
R5	9.09 k, ±1%
R6	N/A
R7	221 R
R8	6.81 k
R9	6.81 k
R10	N/A
R11	10 k
R12	10 k
L1	4.7 µH
D1	DISC 4

Figure 14: Boost Converter	
C1	47 µF, 10 V
C2	10 nF
C3	22 nF
C4	1 nF
C5	100 nF
C6	10 µF, 25 V
C7	100 nF
C8	1800 pF
C9	(Optional)
C10	10 pF
C11	100 pF
R1	1 k
R2	10 k
R3	511 R
R4	100 R
R5	9.09 k, ±1%
R6	1 k
R7	1 k
R8	10 k
R9	3.3 k
R10	10 R (Optional)
R11	10 k
R12	10 k
R13	15 R
L1	4.7 µH
D1	DISC 4