# Designing with the Si9976DY N-Channel Half-Bridge Driver and LITTLE FOOT Dual MOSFETs

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## Introduction

The Si9976DY is a fully integrated half-bridge driver IC which was designed to work with the LITTLE FOOT® family of power MOSFET products in 20- to 40-V systems. The Si9976DY provides the gate drive for both the low- and high-side MOSFETs while the Si9959DY (SO-8, 2.0 A), Si9955DY (SO-8, 3.0 A), Si9945 (SO-8, 3.3A) or Si9940DY (SO-16, 5.0 A) dual n-channel LITTLE FOOT MOSFETs provide power handling capability without the need of a heatsink. All of these devices are supplied in surface-mount packages. The combination of the Si9976DY and one of the dual n-channel MOSFETs creates a powerful and flexible solution for power switching in dc motor drives.

## Si9976DY Overview

The Si9976DY is an integrated driver for an n-channel MOSFET half-bridge (see Figure 1). Schmitt trigger inputs provide logic signal compatibility and hysteresis for noise immunity. Low impedance outputs are provided to drive both the low- and high-side MOSFETs of the half-bridge. The addition of a bootstrap capacitor allows the internal circuitry to level shift both the power supply and the logic signals that are required for the high-side n-channel MOSFET gate drive. A charge pump has been included to replace the leakage current in the high-side driver, which allows static (dc) operation.

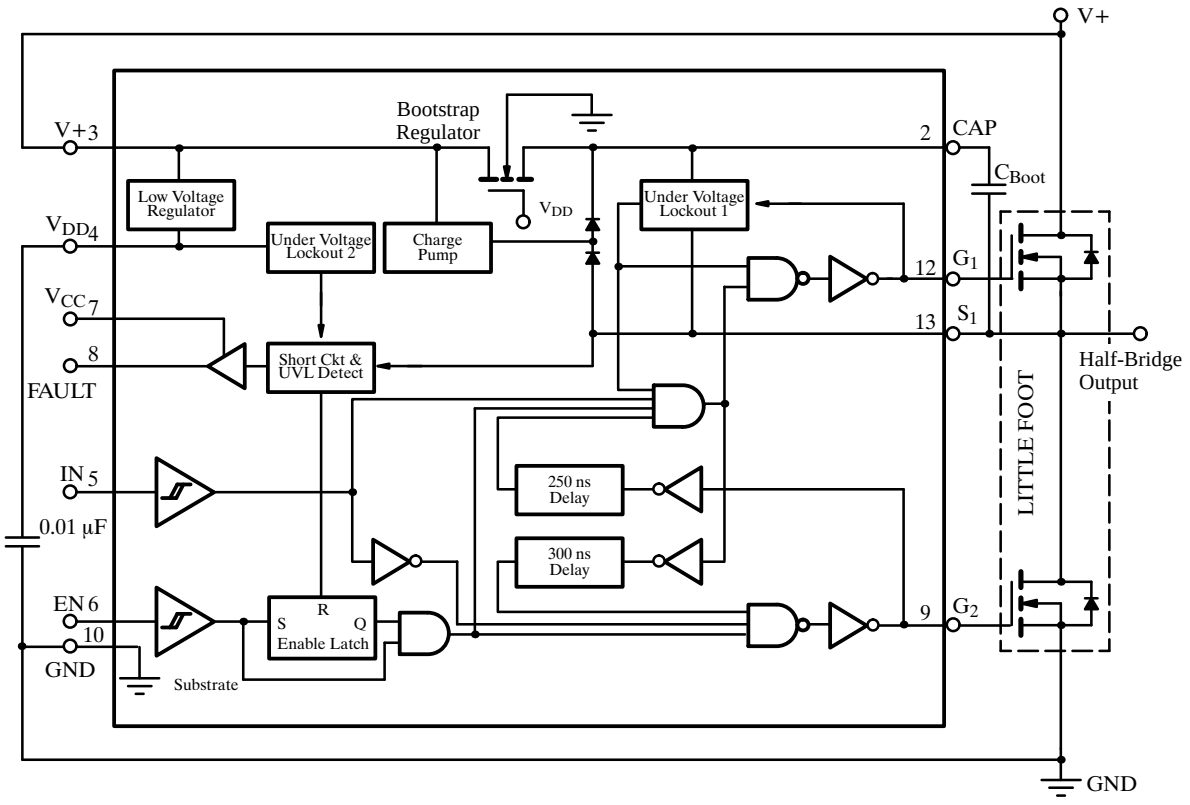


Figure 1. Si9976DY Functional Block Diagram

A separate voltage input, $V_{CC}$, powers the FAULT output to allow easy interfacing to the user's system. Protection circuits include an undervoltage lockout to assure safe gate-drive levels, timing delays to prevent cross-conduction, and a monitor for short circuits on the half-bridge output (S1). An internal voltage regulator drops the input voltage (V+) to a nominal 16 V for the low-side circuitry, which allows the Si9976DY to operate over an input voltage range of 20 to 40 V. The device is specified over the industrial temperature range (–40° to +85°C).

## Input Voltage Requirements

The Si9976DY operates from a single supply voltage of 20 to 40 V dc. This voltage feeds both the bootstrap and the low-voltage regulators. The bootstrap voltage regulator charges the bootstrap capacitor, while the low-voltage regulator drops the input voltage to a nominal $V_{DD}$ of 16 V for the low-side logic and the output drive for the low-side MOSFET.

If the FAULT output is used, a separate voltage (4.5 to 16 V), must be applied to the $V_{CC}$ pin. This guarantees compatibility with the logic levels in the motor controller.

## Output Drive Details

A unique feature of the Si9976DY is the integral high-side drive circuitry. This includes logic-signal level shifting, a bootstrap power supply, a charge pump, an undervoltage lockout, and a 40-mA output driver.

A bootstrap supply and a charge pump comprimise the high-side power supply, and utilize the benefits of each technique. By itself, bootstrap supply provides sufficient charge for MOSFET turn-on. However, it has two drawbacks when used alone. First, a bootstrap capacitor must be recharged after every MOSFET turn-on. Second, a bootstrap supply cannot sustain a MOSFET in the on state indefinitely because the gate leakage current continues to deplete the charge on the bootstrap capacitor. A charge pump meanwhile, can provide a continuous source of charge, but in fully integrated form it cannot provide sufficient charge for MOSFET turn-on at typical modulation frequencies. Combining the two techniques solves these problems. The bootstrap supply provides the turn-on charge while the charge pump provides the leakage current to allow static operation.

Because a bootstrap supply is used, the bootstrap capacitor must get charged immediately after power on and then be recharged after every high-side turn on. Likewise, the low-side MOSFET must be turned on to complete the charging circuit for the bootstrap capacitor. Some drive schemes toggle between the top and bottom MOSFETs, which accomplishes the required charge and recharge of the bootstrap capacitor automatically. It is important to understand that the charge pump operates only when the high-side is turned on.

The bootstrap capacitor provides the charge that turns on the high-side MOSFET. This capacitor should be sized such that it will hold 10 times the charge required to turn on a MOSFET fully (i.e., $V_{GS}$ = 10 V). A typical capacitor value can be calculated by using the equation $C_{BOOT}$ = 10 x ($Q_g/V_{GS}$). The value of $Q_g$ is taken from the gate charge curve of the MOSFET being driven at $V_{GS}$ =10 V. Using this method of capacitor selection, the bootstrap voltage will drop approximately 1 V when the MOSFET is turned on. A 0.01 µF capacitor works well for the Si9955DY, which requires a 10-nC charge to turn on with $V_{GS}$ = 10 V.

A certain minimum recharge time is required for the bootstrap capacitor after each high-side turn-on. The recharge time is a function of the amount of charge which has been used to turn on the high-side MOSFET, the size of the bootstrap capacitor, and the drain current

**Table 1.** Recommended Values

| Part Number | $r_{DS(on)}$ | $Q_g$ @ $V_{GS}$ = 10 V (nC) | Minimum Recommended $C_{BOOT}$ (µF) |
|---|---|---|---|
| Si9940 | 0.05 | 30 | 0.039 |
| Si9945 | 0.10 | 15 | 0.018 |
| Si9955 | 0.13 | 8 | 0.01 |
| Si9959 | 0.30 | 4.7 | 0.0056 |

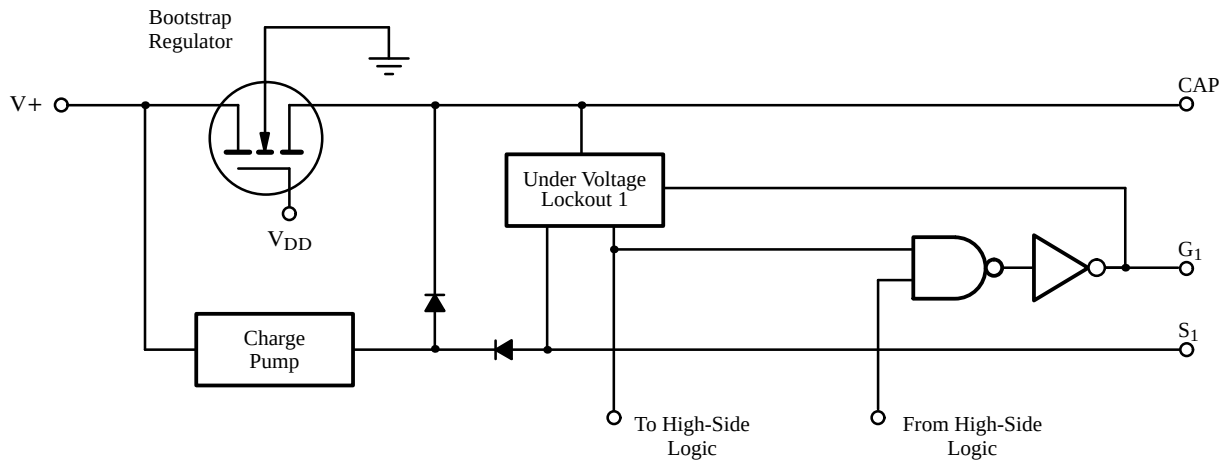


**Figure 2.** High-Side Drive

of the bootstrap transistor in the Si9976DY. In the case of the Si9976DY, the recharge time decreases as V+ increases. Part of this decrease is due to the contribution of the charge pump to the recharging of the bootstrap capacitor. As V+ increases, the charge pump contribution increases. In some cases, the charge pump becomes the only source of charge required to recharge the bootstrap capacitor.

Figure 3 shows the typical recharge time for the Si9959DY, Si9955DY, and Si9940DY LITTLE FOOT power MOSFETs as a function of V+. The bootstrap capacitor for each MOSFET was selected using the method described, and the switching frequency was 20 kHz.

If a shorter recharge time is required, an external signal diode can be added from $V_{DD}$ to the positive side of the bootstrap capacitor (CAP). This increases the charging current, especially at the lower values of V+. Also, the value of the capacitor on $V_{DD}$ should be increased, since this is the source of the additional charging current. The reduced recharge time is shown in Figure 4.

The low-side drive circuitry operates directly from $V_{DD}$ and does not have recharge requirements. The capacitor connected to $V_{DD}$ supplies the charge required to turn on the low-side MOSFET. It must be sized to ensure that $V_{DD}$ does not drop below 14 V, which would trigger an undervoltage condition. As in the case of the bootstrap capacitor, the $V_{DD}$ bypass capacitor should be sized such

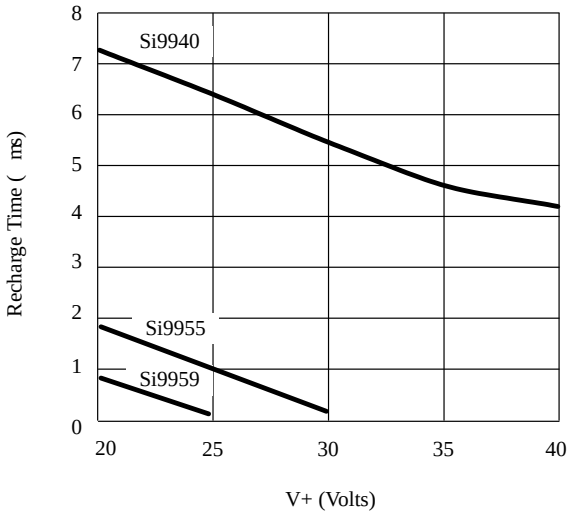


**Figure 3.** V+ vs. Re-

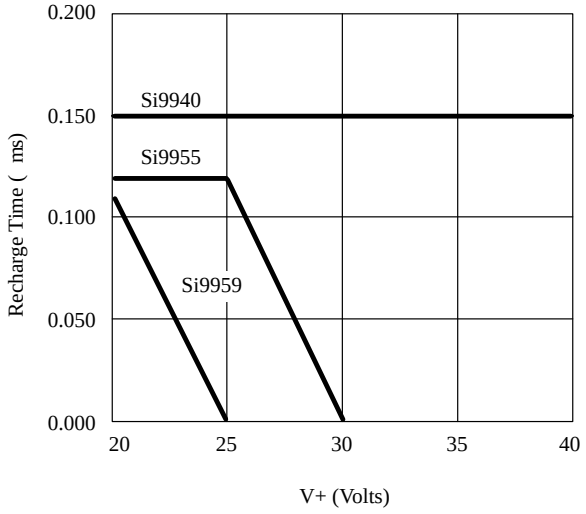


**Figure 4.** V+ vs. Recharge Time with

that it will hold 10 times the charge required by the MOSFET at a $V_{GS}$ = 10 V (C = 10 x $Q_g/V_{GS}$). The Si9955DY requires a 10-nC charge for turn on with $V_{GS}$ = 10 V. Therefore, a 0.01 µF capacitor will work well. Since the requirements for value selection are the same as for the bootstrap capacitor, the recommended values in Table 1 also apply to the $V_{DD}$ bypass capacitor. If an external bootstrap diode is used to reduce the bootstrap capacitor recharge time, the value of the $V_{DD}$ bypass capacitor should be doubled. This compensates for the additional load of recharging the bootstrap capacitor and prevents the occurrence of an undervoltage condition.

## Cross Conduction Protection

Turn-on delays have been incorporated to prevent cross conduction of the half-bridge MOSFETs (Figure 5). The high-side MOSFET can be turned on only after a 250-ns time delay, which is initiated by the low-side output, G2, switching to ground. The low-side MOSFET can be turned on only after a 300-ns delay which is initiated by the high-side control logic. These delays prevent one half-bridge MOSFET from turning on before the other is completely turned off. The difference in the method of generating the delays occurs because the high-side output, G1, is level shifted with respect to S1.

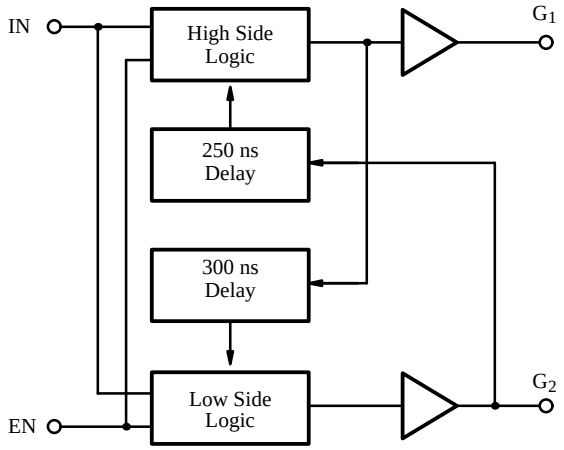


**Figure 5.** Cross Conduction Protection

## Undervoltage Lockout

During power up, both MOSFETs are held off until the internal power supply, $V_{DD}$, is within approximately 0.7 V of the final value, which is nominally 16 V. After power up, the low-side undervoltage lockout circuitry, UVL2, continues to monitor $V_{DD}$. If an undervoltage condition occurs, both the high-side and the low-side MOSFETs will be turned off, and the FAULT output will be high. When the undervoltage condition no longer exists, the FAULT output will be cleared and normal function will resume.

A separate undervoltage lockout circuit, UVL1, monitors the bootstrap voltage. If an undervoltage condition exists when the IN line is switched high, this circuit will prevent the high-side MOSFET from turning on. In addition, one of the following conditions will exist. If S1 is high (as the result of inductive flyback current through the high-side MOSFET's body-drain diode or a short from S1 to V+), the high-side MOSFET will be allowed to turn on as soon as the undervoltage condition has been removed. If S1 is low, the high-side MOSFET will be allowed to turn on only after the undervoltage condition has been removed and the IN line has been toggled low and back to high.

## Short Circuit Protection

If the load voltage, S1, does not make the intended transition through ½ $V_{DD}$ to either ground or V+ before a specified time, the Si9976DY sees this as an output short circuit (Figure 6). The transition should take place in less than 300 ns for a transition to V+, and 200 ns for a transition to ground. Detection of a short circuit condition latches both outputs off and the fault line high. The outputs are re-enabled by a rising edge on the enable line, EN.

## FAULT Output

The FAULT output goes high whenever the Si9976DY detects an output short circuit or a $V_{DD}$ undervoltage condition. The detection of the short circuit inhibits operation and sets a fault latch which is cleared by a rising edge on the enable line, EN. The $V_{DD}$ undervoltage condition inhibits operation and indicates a fault but is nonlatching.

**Table 2.** FAULT Output Truth Table

| EN | IN | Condition | FAULT Output | G1 Out | G2 Out |
|---|---|---|---|---|---|
| 1 | 0 | Normal Operation | 0 | Low | High |
| 1 | 1 | Normal Operation | 0 | High | Low |
| 0 | X | Disabled | X | Low | Low |
| 1 | 0 | Load Shorted to V+ | 1 | Low | Low |
| 1 | 1 | Load Shorted to Ground | 1 | Low | Low |
| 1 | 1 | Undervoltage on $C_{BOOT}$ | 0 | Low | Low |
| 1 | 0 | Undervoltage on $C_{BOOT}$ | 0 | Low | High |
| X | X | Undervoltage on $V_{DD}$ | 1 | Low | Low |

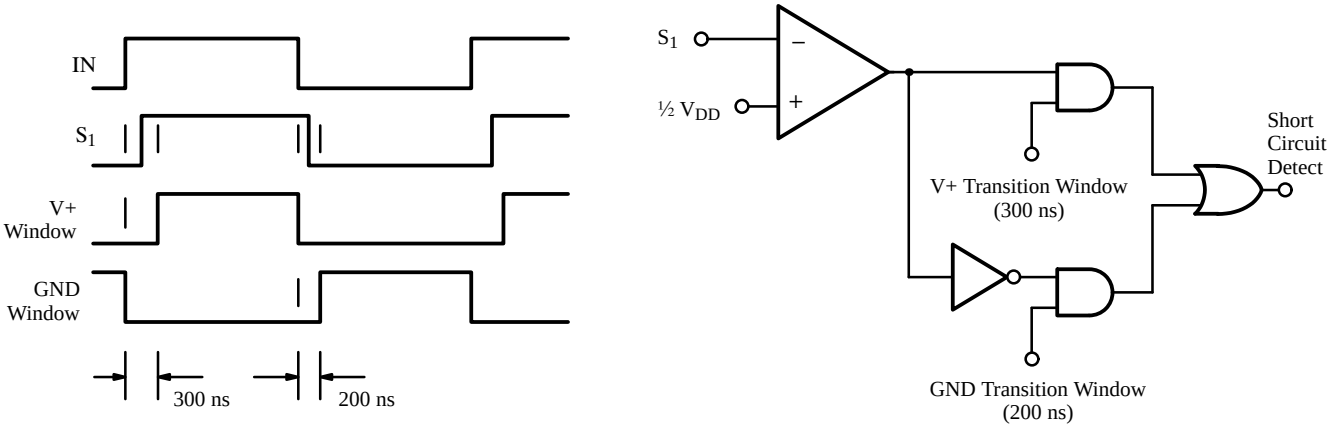


**Figure 6.** Short Circuit Protection

The system-logic supply voltage of 4.5 to 16.5 V can be applied to $V_{CC}$ to facilitate interfacing of the FAULT output to the user's system. If $V_{CC}$ is not supplied, there will be no signal on the FAULT output. However, the fault protection circuitry will continue to function as described.

## PWM Circuits in H-Bridges

### Anti-Phase Control

The Si9976 was designed to be used in an anti-phase control strategy. This approach is unique in that the PWM signal controls both speed and direction with duty cycle alone. Zero to 50% duty cycle defines zero to full speed in one direction, 50% duty cycle is zero speed, and 50% to 100% duty cycle defines zero to full speed in the opposite direciton. This approach ensures that the bootstrap capacitor is always charged, since the H-bridge is continuously switching.

The basic hook-up of an anti-phase H-bridge is very simple. One half-bridge is driven directly with the PWM signal, and the other half-bridge is driven with the inverse of the PWM signal (see Figure 7).

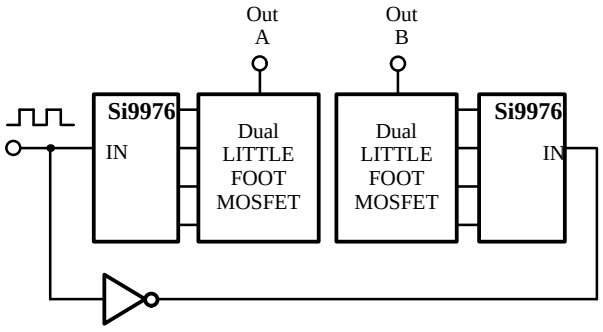


Figure 7. Anti-Phase Control

## Sign-Magnitude Control

As a secondary function, the Si9976 can be used in sign-magnitude controls. In this approach, direction of rotation is determined by the diagonal pair of MOSFETs that are turned on, and speed is controlled by pulse width modulation of the active diagonal pair.

The logic required to control the H-bridge is more complex due to the need to steer the pulse width modulation signal to the active MOSFET pair. The circuit in Figure 7a applies the PWM signal only to the low-side active MOSFET.

There are a couple of things to be aware of in this mode of operation. Application of the PWM signal to the EN input when the IN input is held low will create an erroneous Fault signal which is the inverse of the PWM signal. This can be eliminated by applying the inverse of the PWM signal to the IN input as shown in Figure 7b. Secondly, care must be taken to ensure that the bootstrap capacitor has been charged prior to a high-side turn on. As low-side on-times decrease, this becomes of greater concern. Minimum low-side on-times must be observed to ensure that the high-side will turn on. Remember that this minimum time can be reduced by adding an external bootstrap diode (see Figure 8). When this is done, it increases the load on $V_{DD}$ and therefore on the decoupling capacitor. The value of the $V_{DD}$ decoupling capacitor should be doubled to prevent an undervoltage condition from occurring.

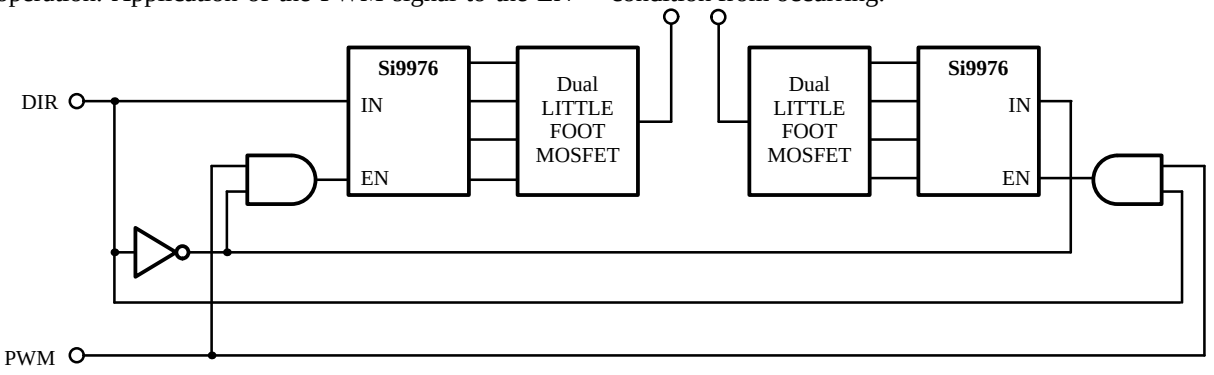


Figure 7a. Sign-Magnitude Control

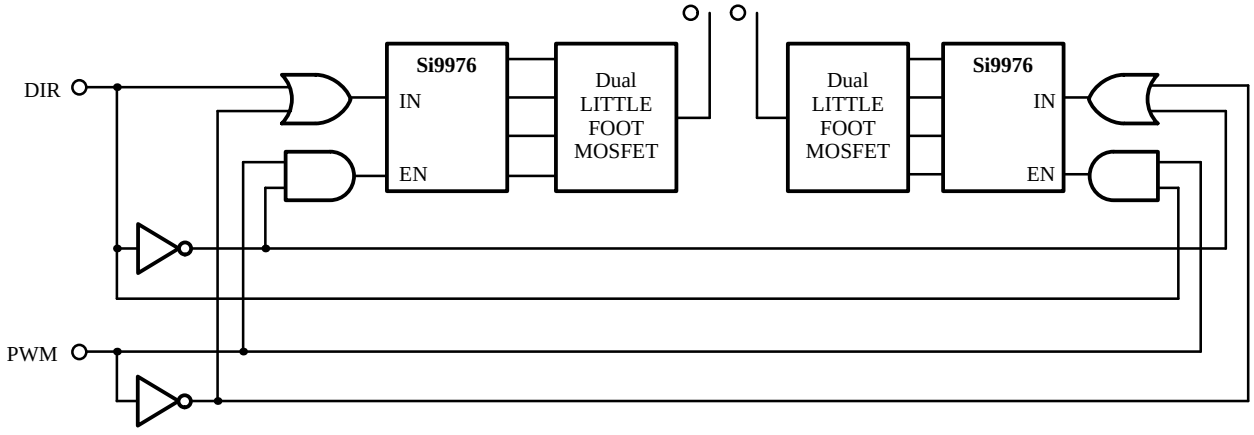


Figure 7b. Sign-Magnitude Control for Low-Side MOSFET PWM

## Braking

Braking is accomplished by turning on both upper or both lower MOSFETs in the H-bridge so the motor windings are shorted together. If the upper MOSFETs are used for this function, be certain that the bootstrap capacitors are charged prior to turning them on.

## Current Sensing

If current sensing is required, a fractional Ω resistor can be inserted in between the low-side MOSFET source connection and ground. External op amps or comparators can then be used to implement current limit or some other current control. A Schottky diode must be connected from the half-bridge output to ground to protect output from negative voltage spikes. In addition to causing potential damage to the Si9976, negative spikes can cause an erroneous latching FAULT. The sensing resistor provides a small amount of isolation of the MOSFET decoupling capacitors from ground. Make sure that decoupling capacitors on MOSFETs are connected directly across the MOSFET pair, high-side drain to low-side source to maximize their effectiveness at reducing noise (see Figure 9).

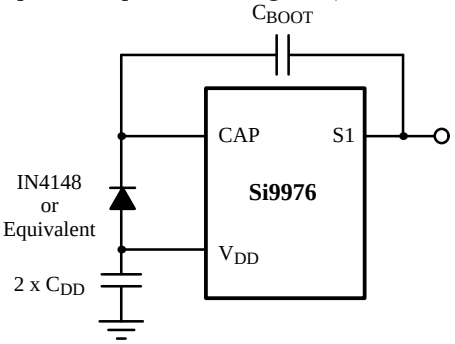


Figure 8. External Bootstrap Diode

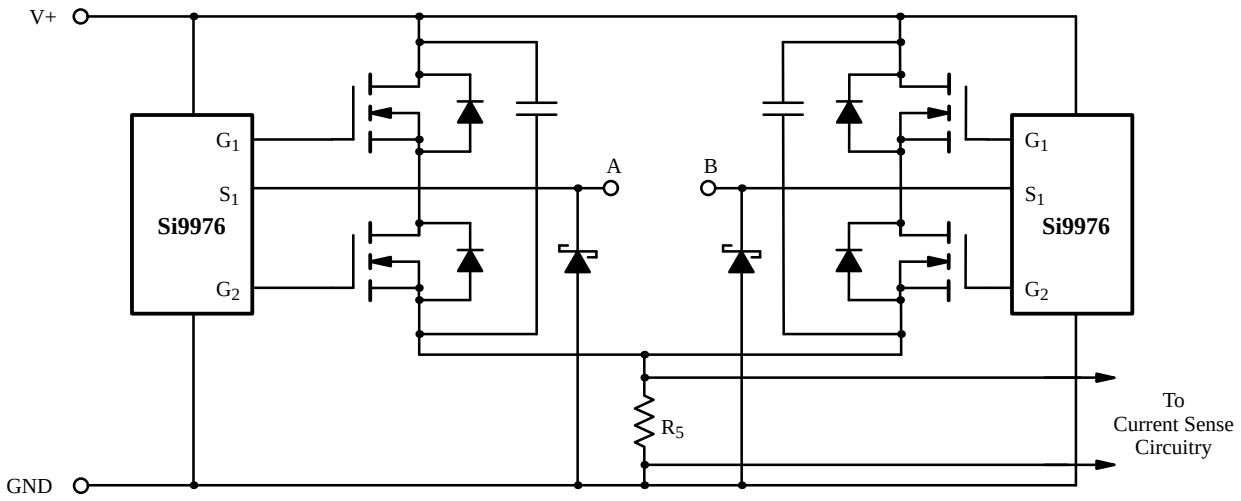


Figure 9. Current Sensing

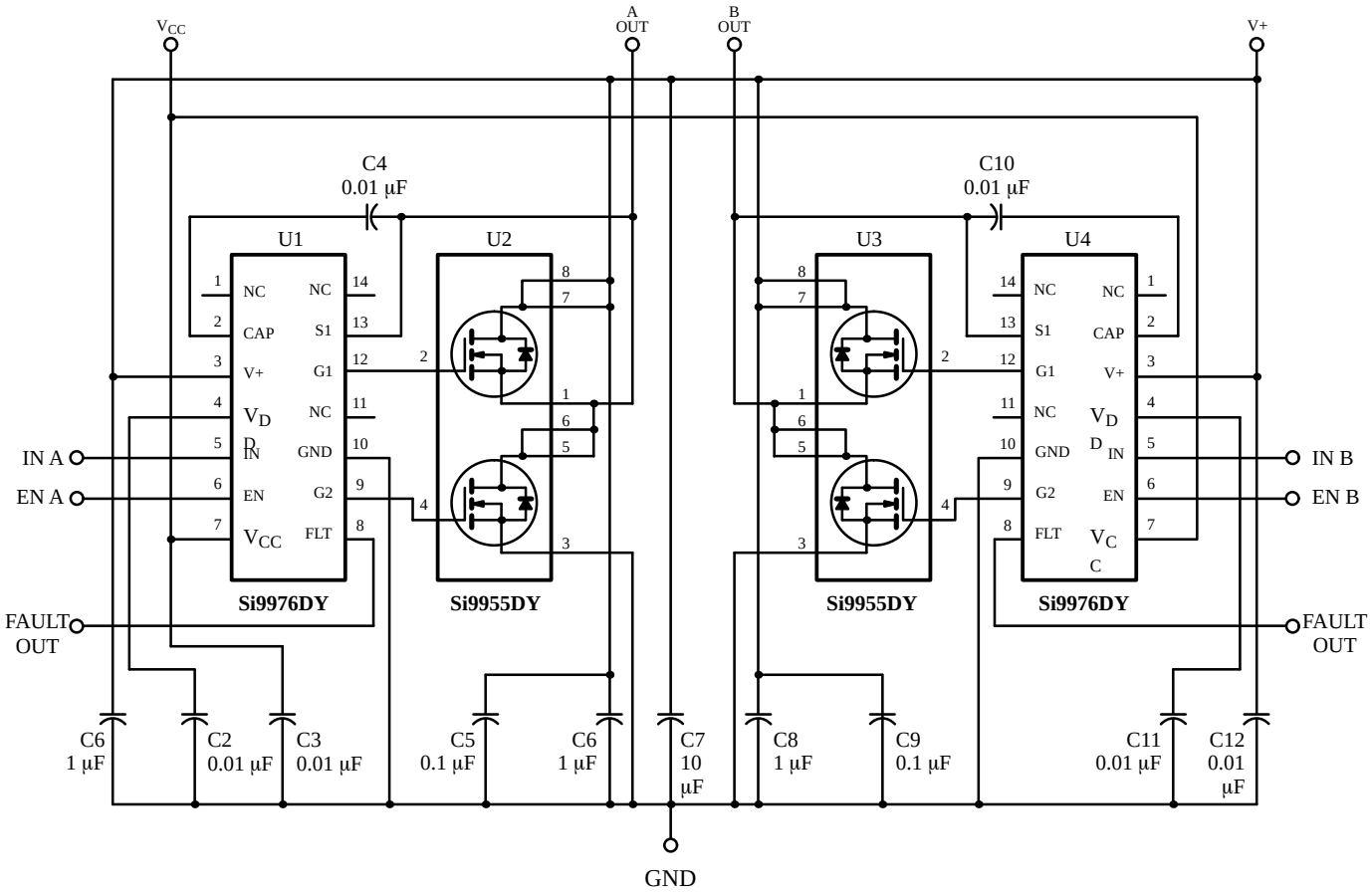


Figure 10 Full-Bridge Configuration with the Si9976DY and the Si9955DY

## A Full-Bridge Application

Figure 10 shows a basic implementation of the Si9976DY and Si9955DY in a full-bridge configuration. Each half-bridge is made up of one Si9976DY driver IC, one Si9955DY LITTLE FOOT dual n-channel MOSFET, a bootstrap capacitor, a filter capacitor for $V_{DD}$, and decoupling capacitors for each IC. This configuration yields a full-bridge circuit with a continuous current rating of 3 A without heatsinking. Use of the Si9959DY or the Si9940DY yields current ratings of 2 A or 5 A, respectively.

Any circuit which generates signals with fast rise and fall times can generate noise. This noise, if not dealt with, can affect the operation of the circuit. Proper PC board layout techniques and device decoupling will take care of these problems. The signal ground trace from the Si9976DY and the trace from the low-side MOSFET source should be run separately to the common ground point. This prevents the noise generated by fast MOSFET transitions from modulating the signal ground of the Si9976DY. Similarly, the trace to the V+ input of the Si9976DY and the trace to the drain of the high-side MOSFET should be connected separately to the supply bypass capacitor.

In addition to layout considerations, decoupling capacitors are required to deal with noise. Adding capacitors across the power supply lines, V+, $V_{DD}$, and $V_{CC}$, provides a low impedance to ground for switching noise and serves as a local energy reservoir when there is a demand for surge current. The $V_{DD}$ capacitor provides the surge current required to turn on the low-side MOSFET.

In addition to basic decoupling, the capacitors added across the half-bridge itself minimize the surge current in the power supply traces, and therefore reduce the generated noise. Although a single capacitor, typically 0.01 µF, works well to decouple a single pin, it is advisable to apply several decades of capacitance across the input power, V+ to GND, to handle the broad spectrum of noise that can be present. The high-frequency (lower value) capacitors should be located as close as possible to the device being decoupled, while the larger capacitors (> 1 µF) can be located farther away and bypass only the power supply.

Figure 11 shows a typical layout for a Si9976DY with LITTLE FOOT dual n-channel MOSFETs. The use of surface-mount packages allows automated assembly of the entire motor drive circuit, without the need for a separate heatsink and its associated material and assembly costs.

## Summary

The Si9976DY provides both low- and high-side gate drive, high-side level shifting, a bootstrap/charge pump high-side power supply, and protection for undervoltage and short circuit conditions in a single surface-mount IC. The Si9940DY, Si9945DY, Si9955DY and Si9959DY are surface-mount MOSFETs for power switching over a broad current range (2 to 5 A) and require no heatsinking. The use of surface-mount packages allows automated assembly of the entire drive system while minimizing use of PC board space.The Si9976DY, when used with one of the dual n-channel LITTLE FOOT power MOSFETs, provides a very flexible approach to power switching in dc motor drives.

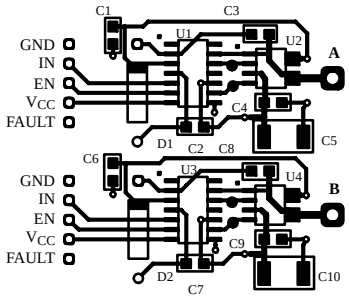


Figure 11 Typical PC Board Layout (Scale 1:1)