

Designing DC/DC Converters to Meet CCITT Specifications for ISDN Terminals

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Integrated Services Digital Network (ISDN) standards are a major step towards the realization of a worldwide information grid. Just as power system standards allow the connection of either a microwave oven or a television set into a power receptacle, so ISDN will allow information appliances, such as facsimile machines, computer terminals, and telephones to plug into a standard socket. It will be possible to move office equipment either down the hall or around the world and immediately "plug in" to the information grid. ISDN will allow the travelling worker to communicate (using portable computers and facsimile machines) with customers or manufacturing sites worldwide. And this will be accomplished without modems, which slow data transmission rates.

One of the larger technical problems in achieving such a powerful information network is that the existing telephone system was designed over eighty years ago for the more limited purpose of reliably transmitting voice signals. Plain old telephone service, or POTS, has such an excellent reliability record that the general public takes for granted that the phone still works when the lights go out. But the simple power feeding method (a central office battery connected to the telephone via a pair of copper wires) is inadequate for ISDN. Nonetheless, ISDN must not achieve upgraded data communication capability at the expense of voice communication reliability. That is, when the lights go out, the new digital telephones must still operate.

The Deutsche Bundespost (DBP) took the lead several years ago^[1] in defining a methodology for feeding power to ISDN terminals which is compatible with the data transmission requirements of ISDN and the reliability requirements of POTS. The DBP proposals have been incorporated into the CCITT standard I.430, which defines the physical characteristics of the ISDN interfaces. [The Consultative Committee for International Telegraph and Telephone (CCITT) is part of the International Telecommunications Union of the United Nations.] The standard calls for galvanic isolation in terminal equipment (TE) connected to the subscriber- or S-bus. This requires the use of an efficient switchmode dc/dc converter in each TE. Also, while the older analog telephony circuits can get by on about 100 mW, the new digital telephones (D-phones) require approximately 300 mW.

Up to eight D-phones or other TEs can be connected to each S-bus, but the CCITT recommendation allows that

only one terminal be operational during restricted power conditions. When the network terminal (NT) senses the loss of normal power, it reverses the polarity of the dc feeding voltage on the S-bus. Non-emergency-designated terminals have a reverse polarity diode which effectively removes their loads from the S-bus during the outage. The emergency-designated terminal uses a diode bridge at the input, so that it remains connected across the bus at all times. This application note specifically addresses design issues relating to emergency-designated ISDN terminals and presents design details for a dc/dc converter which conforms to the international standard.

CCITT Standard I.430

Table 1 summarizes the CCITT document as it applies to dc/dc converters in emergency-designated TEs. During normal-mode operation, terminals may have multiple power sources, including up to 1 W from the S-bus (Power Source 1), whose dc voltage must be between 24 and 42 V measured at the input to the TE. During the restricted power condition the designated TE in the active state must draw less than 380 mW from Power Source 1 (PS1), and the input voltage magnitude must be 32 to 42 V. Eighty percent efficiency has previously been demonstrated for dc/dc converters at these power levels^[2].

The difficult problem presented by the CCITT specification occurs when the phone is on-hook (deactivated state) during the restricted power condition. In order that the terminal be capable of receiving incoming calls, the line activity detection circuitry in the TE must continue to operate while the total power consumption must be maintained below 25 mW. Also, the "Terminal Endpoint Identifier (TEI)" must be retained, which means that some power is required for memory holdup. These functions require approximately 13 mW, and the input voltage is still in the 32- to 42-V range.

Needless to say, off-the-shelf +40-V to +5-V dc/dc converters with 55% worst-case efficiency at an output power level of 13 mW do not exist today. They can, however, be designed using readily available off-the-shelf components, but the methodology for their design is different from that of conventional power supplies.

Design Methodology

A flyback converter topology provides galvanic isolation while requiring only one magnetic energy storage device. This minimizes cost since inductors and transformers are the most expensive components in switch mode power converters. Selection of the primary inductance value was discussed in a previous Siliconix Application Note, AN87-2, which analyzes the start-up constraints of dc/dc converters fed from high-impedance sources. The result of that analysis was a primary inductance of 3.75 mH. Since the S-bus is relatively short compared to the subscriber loop, and it is fed from a dc/dc converter in the NT, the source impedance seen by the dc/dc converter in the TE is relatively low. This indicates that a lower primary inductance, L_P , can be chosen, which allows the inductor to be smaller.

There is, however, another reason to utilize a high inductance value. The energy transferred to the inductor during each cycle is given by Equation 1.

$$E = \frac{1}{2} L_P I_{PK}^2 \quad (1)$$

I_{PK} is the peak inductor current, and it is assumed that the initial current is zero. The same amount of energy transfer can be achieved with a small L_P and large I_{PK} , or vice versa. But the RMS value of the current is less for the case of large L_P and small I_{PK} . This reduces the conduction losses in the primary winding, MOSFET, and sense resistor, which is essential to achieving high efficiency at the milliwatt power level. With a total power budget of only 25 mW, every milliwatt lost causes a four percent reduction in efficiency.

To minimize dynamic losses, defined as those dependent upon operating frequency, it is advantageous to use the

smallest switching frequency, f_S , which is practical. If possible, this frequency should be above the audible range. 18 kHz was selected for the nominal switching frequency when the oscillator is free-running (36 kHz for the oscillator, which includes a divide-by-two). This occurs during start-up or under restricted power conditions. For operating conditions other than the deactivated state in the restricted power mode, a system clock should be available. It is desirable to synchronize the dc/dc converter to a signal derived from this clock to minimize noise coupling into the A/D and D/A converter (CODEC) circuits. The synchronization frequency should be 10 to 20% above the free-running frequency.

Another choice must be made which has a large impact on the dc/dc converter cost, light load efficiency, and output voltage regulation. Voltage feedback must be implemented while at the same time maintaining galvanic isolation. There are two possible approaches. The first is to use optical isolation and place the error amplifier and voltage reference on the secondary side. This gives the best result in terms of load regulation, but it costs more and it decreases light load efficiency. The error amp and reference generator could be eliminated from the primary side controller and put into a separate IC on the secondary side. For these components, the power losses thus remain approximately the same. But the optical isolator consumes some additional power and increases total converter cost.

The second option, which is used here, is to employ an auxiliary winding to indirectly sense the output voltage. This winding is essentially free, since it must be used anyway to provide the bootstrap supply for the switchmode regulator IC. Using this technique, the output voltage regulation is dependent upon the coupling between the secondary and auxiliary windings as well as upon the switching frequency.

Table 1. Power Source 1 Requirements Emergency – Designated ISDN TE's

| Power Mode | TE State | Voltage Range | Max Power to TE |
|------------|-------------|---------------|-----------------|
| Normal | Active | + 24 to +42 V | 1 W |
| Normal | Deactivated | +24 to +42 V | 100 mW |
| Restricted | Active | -32 to -42 V | 380 mW |
| Restricted | Deactivated | -32 to -42 V | 25 mW |

The total variation in output voltage as the load current is varied from the minimum (3 mA at +5 V, 0 mA at -5 V) to the maximum level (100 mA at +5 V, 30 mA at -5 V)

was 10%. This should permit a specified regulation range of $\pm 7\%$ at the converter output. If tighter regulation is

required for a given application, then the opto-isolation approach will be required.

Circuit Description

The complete schematic for the dc/dc converter is given in Figure 1, and the block diagram of the Si9105 switchmode regulator IC is shown in Figure 2. The Si9105 is a variation of the original Si9100 switchmode regulator which was introduced in March, 1987. It includes an oscillator, an error amplifier, a pre-regulator/start-up circuit, a trimmed voltage reference, low-power CMOS logic and comparators, undervoltage lockout and current-limit protection circuitry, and a high-voltage MOSFET transistor—all on a single chip in a 14-pin DIP or 20-pin PLCC for surface-mount assembly.

The block diagram of the Si9105 is the same as that for the Si9100, but several key specifications are upgraded. The

most important specification here is the maximum power dissipation of the chip. The supply current, I_{CC} , is 0.5 mA maximum (0.35 mA typical), giving $P_D = 5$ mW maximum for $V_{CC} = 10$ V. The start-up circuit shuts off the 120-V rated pre-regulator transistor after start-up so that I_{CC} is taken from the auxiliary 10-V output rather than from the 40-V input bus. The power saved is approximately

$$\begin{aligned}
 P_{\text{Saved}} &= \\
 (40 \text{ V}) (0.35 \text{ mA}) - (10 \text{ V}) (0.35 \text{ mA}) &= \\
 14 \text{ mW} - 3.5 \text{ mW} = 11.5 \text{ mW} & \quad (2)
 \end{aligned}$$

Without such an auxiliary supply, it is easy to see from Equation 2 that 55% efficiency with 25 mW at the input is not possible.

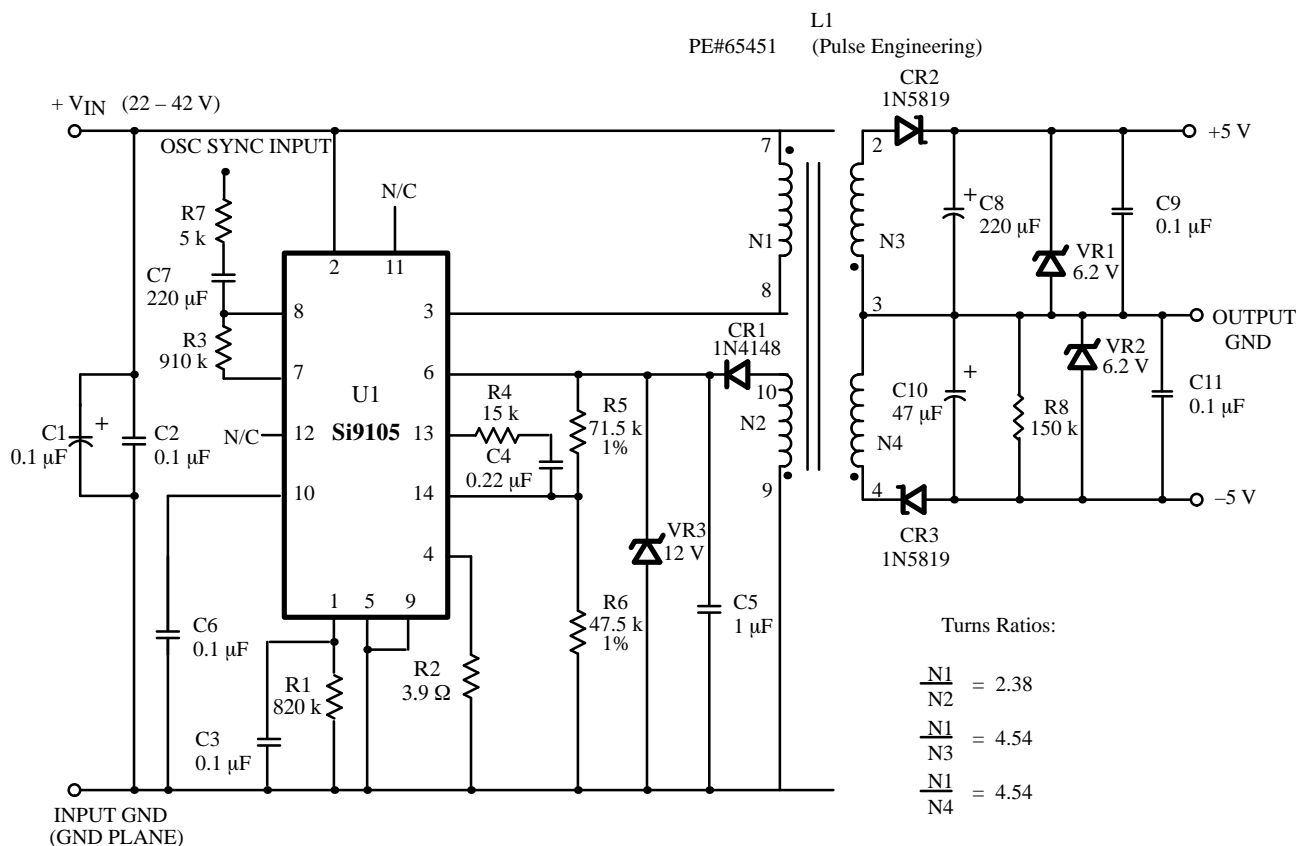


Figure 1. dc/dc Converter Schematic for Emergency—Designated ISDN Terminals

* Pulse Engineering, Inc., P.O. Box 12235, San Diego, CA 92112, (619) 268-2400

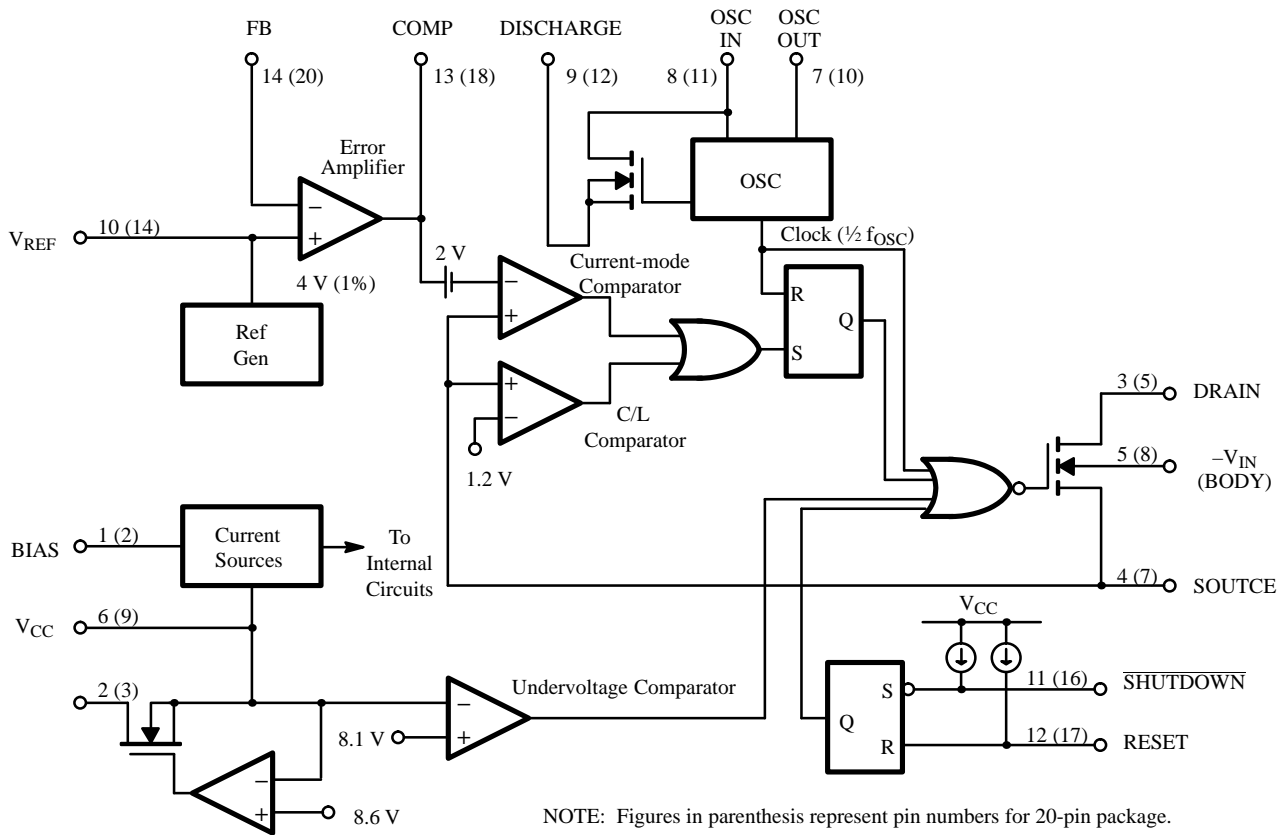


Figure 2. Si9105 Block Diagram

The 4-V reference of the Si9105 is a temperature compensated buried Zener, which is trimmed to 1% initial accuracy at a specified bias current of 7.5 μ A. This is one-half of the bias current specified for the Si9100, and a bias resistor equal to 820 k Ω from pin 1 to ground is all that is required to program I_{BIAS} . Finally, the MOSFET switching transistor in the Si9105 has been rated at a higher breakdown voltage, 200 V versus 150 V, at the same time its $r_{DS(ON)}$ has been maintained at 5 Ω maximum.

The other key component in the converter circuit is the coupled inductor, L1. Pulse Engineering* has provided a cost-effective inductor design, part number PE65451, specifically designed for this ISDN terminal application. L1 has an isolation voltage specification of 1750 V_{RMS} .

Measured Circuit Performance

Figure 3 shows an oscilloscope photograph of the primary side voltage and current waveforms for operation under the emergency load conditions.

The calculated peak current is

$$P_{IN} = 25 \text{ mW} = \frac{1}{2} L_P I_{PK}^2 f_S$$

For $L_P = 3.8 \text{ mH}$ and $f_S = 18 \text{ kHz}$, I_{PK} equals 27 mA. The MOSFET conduction time is calculated from

$$\frac{V_{IN}}{L_P} = \frac{I_{PK}}{t_{ON}} \tag{4}$$

For $V_{IN} = 40 \text{ V}$, $L_P = 3.8 \text{ mH}$, and $I_{PK} = 27 \text{ mA}$, t_{ON} is equal to 2.6 μ s and the duty cycle is $(2.6 \mu\text{s}) \cdot (18 \text{ kHz}) = 0.046$ (or about 5%). Figure 4 shows the corresponding waveforms during full load operation.

An efficient power supply which self-destructs when its output is shorted to ground is of limited value. Some additional components are needed to protect the power supply and its loads from overcurrent and overvoltage transients.

Figure 5 shows the converter waveforms with the output terminals shorted to ground. Note that the converter goes into the continuous conduction mode of operation (the current waveform is trapezoidal), but the dc input current was measured at 10.5 mA. The power dissipation of $(10.5 \text{ mA}) \cdot (40 \text{ V}) = 420 \text{ mW}$ can be sustained indefinitely without damage to the converter.

When the short circuit is removed from the converter output, the control loop forces the duty ratio to increase to its maximum value since the error amplifier output will be near the positive rail. The control loop has been made purposely slow to prevent it from being susceptible to noise when operating at very light loads. This causes the recovery time from the short circuit condition to be long, and the output and auxiliary winding voltages become excessive unless clamped by Zener diodes VR1, VR2, and VR3. As a final note, the recommended procedure for oscillator synchronization is to feed a positive going SYNC pulse through an R-C network to pin 8. The recommended values are 5 kΩ and 220 pF.

A summary of the dc/dc converter specifications is given in Table 2 for reference.

Circuit Analysis

It is instructive to calculate the converter losses for the restricted power condition in the inactive state to gain some insight as to the relative importance of the design parameters. In other words, how important are MOSFET $r_{DS(on)}$ and output capacitance, leakage inductance, switching frequency, etc. to the converter efficiency?

Table 2.

| | |
|------------------------------|---|
| Input Voltage Range | Max. Load 22 – 42 V Min. Load 30 – 42 V |
| Output Load Current | Min. Load 3 mA @ +5 V 0 mA @ -5 V Max. Load 100 mA @ +5 V 30 mA @ -5 V |
| Regulation | ±7% worst case (±5% typical) |
| Output Ripple | 100 mV Max. at full load (60 mV typical) at full load |
| Conversion Efficiency | Max. Load 80% min (85% typical) Min. Load 55% min.(67% typical) |
| Isolation Voltage | 1750 V _{RMS} primary to secondary |

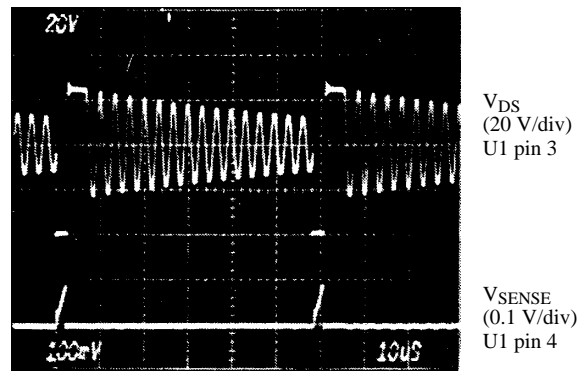


Figure 3. MOSFET drain voltage and current waveforms for emergency-power operation

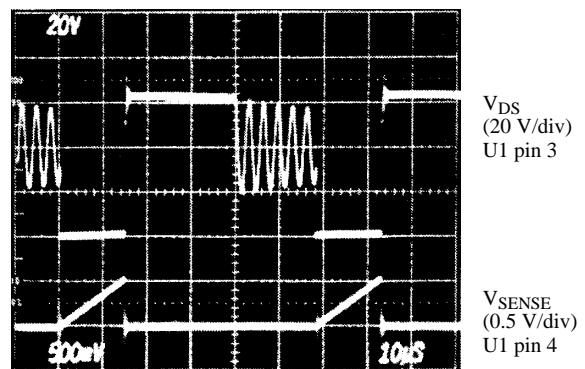


Figure 4. MOSFET drain voltage and current waveforms for full-load operation

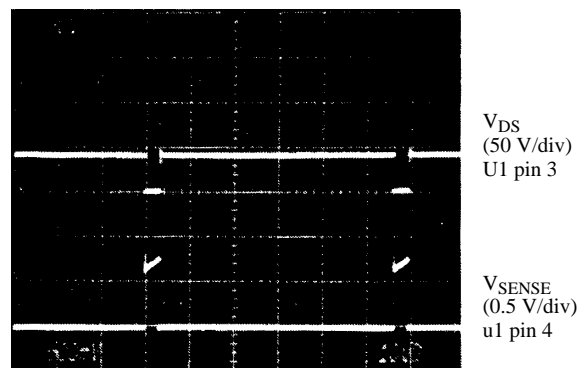


Figure 5. MOSFET drain voltage and current waveforms for the output short circuit condition.

Table 3. Power Loss Calculations (Emergency Power-Down State)

| Source of Loss | Dynamic Losses (freq. dep.) | Static Losses (not freq. dep.) | Load-Dependent Losses | No-load losses |
|--|-----------------------------|--------------------------------|-----------------------|----------------|
| MOSFET + R _{sense} (conduction) | | 0.09 | 0.09 | |
| Feedback Voltage Divider Network | | 0.84 | | 0.84 |
| Rectifier Conduction | | 1.58 | 1.58 | |
| -5 V Pre-Load | | 0.18 | | 0.18 |
| Si9105 Controller (REF Gen + Analog) | | 2.85 | | 2.85 |
| Si9105 Controller (Logic + OSC + Driver) | 0.50 | | | 0.50 |
| Turn-On (½ CV²f _s) | 1.08 | | | 1.08 |
| TOTAL | 1.58 mW | 5.54 mW | 1.67 mW | 5.45 mW |

7.12 mW

7.12 mW

Measured: P_{IN} = 22.92 mW, P_O = 15.25 mW, h = 66.6%, P_{Ioss} = 7.67 mW

The exercise of “counting the milliwatts” was performed and is included in Appendix A for reference. The summary appears in Table 3. Power losses are sorted in two different ways: 1) according to whether or not they should be expected to vary with the choice of operating frequency (dynamic vs. static losses) and 2) according to whether or not they vary with the output load current. The power consumption of the Si9105 is divided into two components: one which is frequency dependent (logic gates plus oscillator plus MOSFET drive) and the other which is constant (voltage reference plus analog circuits).

Several interesting conclusions can be drawn from Table 3. An observation which may well have been expected is that most of the losses are not load dependent at the 25 mW power level. But one may not have expected that the MOSFET conduction and sense resistor losses should be nearly negligible. These losses, together with the rectifier losses, totally dominate for the full load condition. A final observation is that MOSFET and transformer parasitic capacitances, which cause negligible losses at higher power levels, have significant effect at such low current levels.

As a final summary of the power converter efficiency, Figure 6 plots the measured efficiency as a function of output power. It should be noted that these efficiencies do not include losses in the input rectifier bridge to the emergency-designated terminal. The worst-case input current is given by Equation 5.

$$I_{IN(max)} = \frac{P_{IN(max)}}{V_{IN(min)}} = \frac{25 \text{ mW}}{32 \text{ V}} = 780 \mu\text{A} \quad (5)$$

Assuming two diode drops at 0.6 V each gives a power loss of

$$P_D = (1.2 \text{ V}) (780 \mu\text{A}) = 940 \mu\text{W}.$$

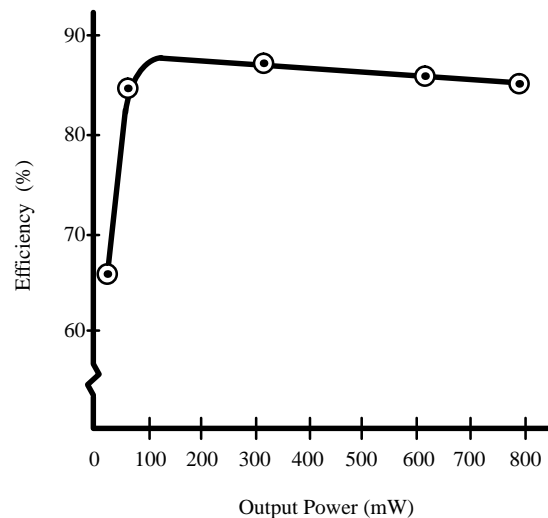


Figure 6. Measured Efficiency vs. Output Power

If the worst case for the Si9105 power consumption is taken into account, then an additional 1.5-mW loss is possible. The 7.7-mW measured loss plus 1.0 mW for the rectifier bridge, 1.5 mW for the regulator IC, and 1.0 mW for other miscellaneous circuit losses gives a worst-case power dissipation of 11.2 mW. Output power is a minimum of 13.8 mW, and the minimum efficiency is 55%.

Conclusion

Worst case efficiency of 55% is a realizable goal for dc/dc converters in ISDN terminals which meet CCITT specifications. The Si9105 switchmode regulator is the

first fully-integrated solution which has been demonstrated to provide the required efficiencies over the 13 mW to 650 mW output power range.

References

- 1) Rosenbaum, D. and Stolp, K., "The Feeding Conception of the ISDN Basic Access," IEEE INTELEC Conference Proceedings, Munich, FRG, Oct 14-17, 1985, pp. 505-512.
- 2) "A One-Watt Flyback Converter Using the Si9100", Siliconix Application Note, AN87-1, March 1987.

APPENDIX A
Calculated Power Losses

1. MOSFET conduction losses –

RMS current is given by

$$I_{\text{RMS}} = I_{\text{PK}} \sqrt{\frac{D}{3}} = 27 \text{ mA} \sqrt{\frac{0.046}{3}} = 3.34 \text{ mA}$$

$$P_{\text{COND}} = I_{\text{RMS}}^2 \cdot r_{\text{DS(ON)}} \\ = (3.34 \text{ mA})^2 \cdot 4 \Omega = 45 \mu\text{W}$$

2. Current sense resistor –

$$P_{\text{SENSE}} = (3.34 \text{ mA})^2 \cdot 3.9 \Omega = 44 \mu\text{W}$$

3. Feedback divider resistor network –

$$P_{\text{DIV}} = \frac{V_{\text{CC}}^2}{R_5 + R_6} = \frac{(10 \text{ V})^2}{71.5 \text{ k}\Omega + 47.5 \text{ k}\Omega} = 840 \mu\text{W}$$

4. Rectifier conduction –

The inductance of the +5 V winding is

$$L_5 = L_P \left(\frac{N_3}{N_1} \right)^2 = 3.8 \text{ mH} \left(\frac{1}{4.54} \right)^2 = 184 \mu\text{H}$$

Peak secondary current is

$$I_S = \left(\frac{N_1}{N_3} \right) I_{\text{PK}} = (4.54) (27 \text{ mA}) = 123 \text{ mA}$$

The diode conduction time is

$$t_{\text{cond}} = \frac{\Delta I}{di/dt} = \frac{I_s}{V/L} = \frac{123 \text{ mA}}{\left(\frac{5.5 \text{ V}}{184 \mu\text{H}} \right)} = 4.10 \mu\text{s}$$

$$T_S = \frac{1}{f_s} = \frac{1}{18 \text{ kHz}} = 55.5 \mu\text{s}$$

The duty ratio for rectifier condition is

$$D_R = \frac{4.10 \mu\text{s}}{55.5 \mu\text{s}} = 0.074$$

 Assuming a constant diode drop, V_F , of 0.35 V at this current level gives

$$P_{\text{RECT}} = \left(\frac{I_s}{2} \right) (V_F) (D_R) \\ = \left(\frac{123 \text{ mA}}{2} \right) (0.35 \text{ V}) (0.074) = 1.58 \text{ mW}$$

5. Pre-load resistor on -5 V output –

$$P_{\text{PL}} = \frac{V_O^2}{R} = \frac{(-5.25)^2}{150 \text{ K}} = 184 \mu\text{W}$$

6. Turn-on losses –

 $P_{\text{ON}} = \frac{1}{2} C_{\text{STRAY}} V_{\text{DS}}^2 f_s$, where C_{STRAY} includes the transformer winding capacitance plus the MOSFET output capacitance.

$$C_{\text{STRAY}} = C_{\text{DS}} + C_{\text{WIND}} \\ \approx 35 \text{ pF} + 40 \text{ pF} = 75 \text{ pF} \\ P_{\text{ON}} = \frac{1}{2} (75 \times 10^{-12}) (40)^2 (18 \times 10^3) = 1.08 \text{ mW}$$

7. Quiescent power for PWM IC –

$$\text{Reference generator } (60 \mu\text{A})(10 \text{ V}) = 0.6 \text{ mW}$$

$$\text{Analog Circuits } (7.5 \mu\text{A})(30)(10 \text{ V}) = 2.25 \text{ mW}$$

 (30 internal current sources at 7.5 μA each)

Logic plus oscillator

$$\left(\frac{1.5 \mu\text{A}}{\text{kHz}} \right) (18 \text{ kHz}) (10 \text{ V}) = 0.27 \text{ mW}$$

MOSFET Driver –

$$P_{\text{DRIV}} = C_{\text{GS}} S V_{\text{GS}}^2 S f_s \\ = (125 \text{ pF}) (10 \text{ V})^2 (18 \text{ kHz}) = 0.225 \text{ mW}$$

Total quiescent power of Si9105 = 3.35 mW