AN627
APPLICATION NOTE

Serial EEPROM Compatible With Plug-and-Play VESA Display Data Channel (Versions 1.0 and 2.0)

The ST products whose names are of the form ST24xy21 are Application Specific Memory devices (ASM). As well as containing 1 Kb of EEPROM, organized as 128 x 8, they are fully compatible with the VESA Data Display Channel (VDDC) modes, DDC1 and DDC2B. When installed in a Plug-and-Play PC display, the device can work in DDC1 mode, using only a 2 wire bus, or in both DDC1 and DDC2B modes, using a 3 wire bus.

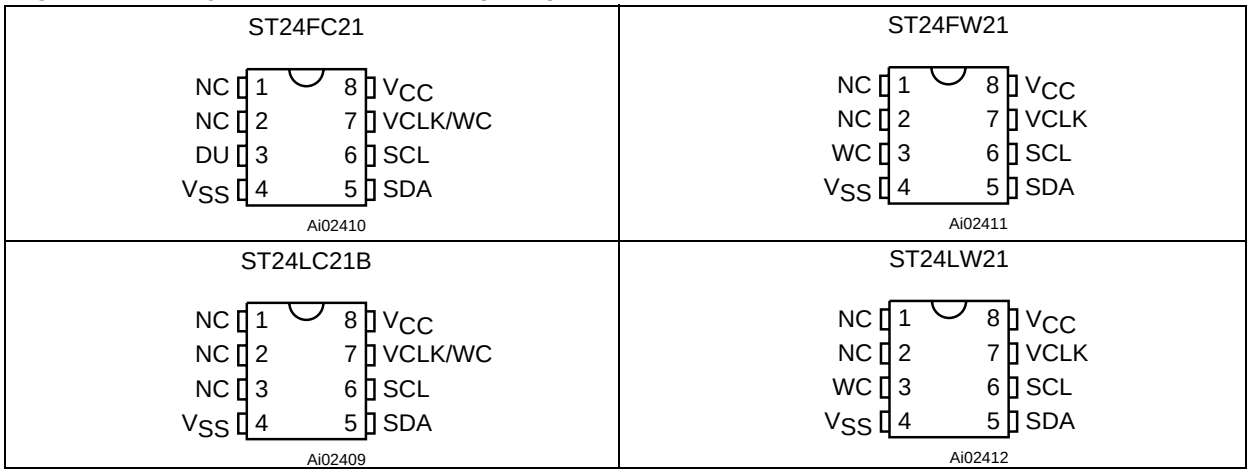
- DDC1: a unidirectional data channel from the display to the host PC, continuously transmitting Extended Display Identification, EDID, information.
- DDC2B: a bidirectional data channel based on the I^2C ™ protocol. The host PC can request Extended Display Identification information, EDID, or Video Display Interface information, VDIF, over the DDC2B channel. In addition to this, the DDC2B channel can act as a transparent channel for ACCESS.bus ™ communication, allowing the direct replacement to be made.

Table 1. Members of the ST24xy21 Family

	Write Control on VCLK (pin 7)	Write Control on pin 3
Conformance to VDDC Version 2.0	ST24FC21	ST24FW21
Conformance to VDDC Version 1.0	ST24LC21B	ST24LW21

Table 1 summarizes the ST24xy21 naming convention. Those products whose names are of the form ST24Ly21 conform to version 1.0 of the VDDC specification. Those products whose names are of the form ST24Fy21 conform to the more recent (March 1996) version 2.0. Those products whose names are of the form ST24xC21 use the VCLK line as the Write Control input, as described on page 7, and those of the form ST24xW21 have a separate Write Control input. All ST24xy21 devices are available in 8-pin PDIP and SO packages. Figure 1 summarizes the pin-out for PDIP.

Figure 1. ST24xy21 Pin Connections (PDIP)



DEVICE DESCRIPTION

The functionality of the ST24xy21 family greatly simplifies the design of the PC graphics board, and allows a direct connection between the display and the host PC using a standard video cable. Each member of the family has a standard I^2C interface, including the SCL and SDA lines, and an additional clock input, VCLK, as required by the V.D.D.C. specification. This additional clock input allows the host PC to receive, from the display, all information required to configure the graphics board and the display's software driver. ST24xy21 serial communication runs at 400 kHz in both DDC1 and DDC2B modes, with a supply voltage between 3.6 V and 5.5 V.

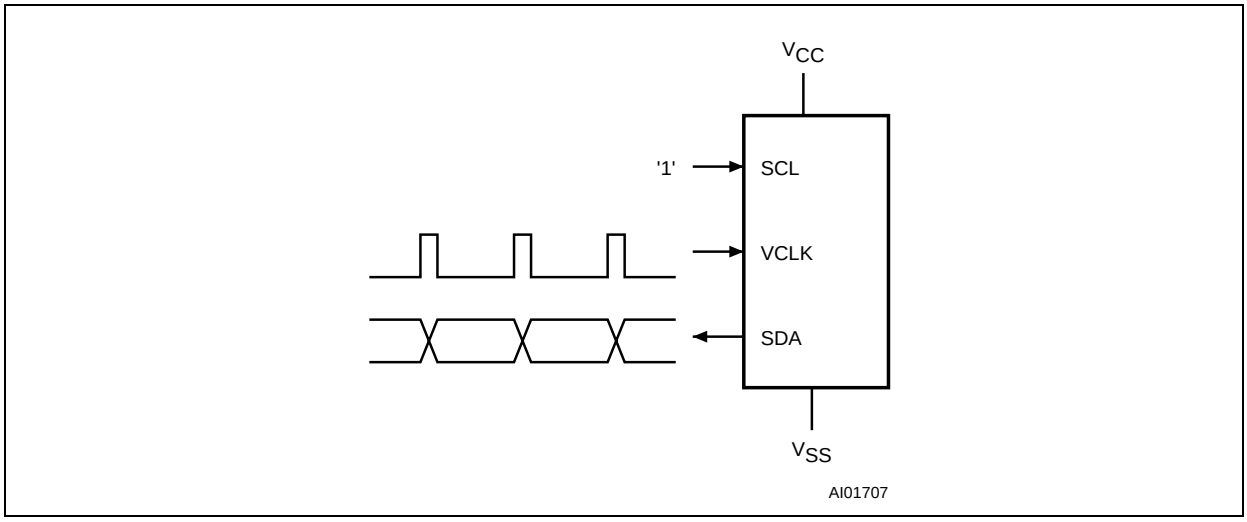
Each member of the ST24xy21 family operates in the two modes of the VDDC specification. The "Transmit Only" mode of the ST24xy21 corresponds to the "DDC1" mode of the VDDC, and the "I^2C Bidirectional" mode corresponds to the "DDC2B" mode.

All members of the ST24xy21 family power-up in DDC1 mode. The device will switch to the DDC2B mode upon the falling edge of the signal applied on SCL pin. Once in the DDC2B mode, the ST24LC21B and ST24LW21 cannot switch back to the DDC1 mode, except by first removing the power supply. However, the ST24FC21 and ST24FW21 enter a transition state after the falling edge of SCL, during which the device will switch back to the DDC1 mode if no valid I^2C activity is observed.

DDC1: Transmit Only Mode

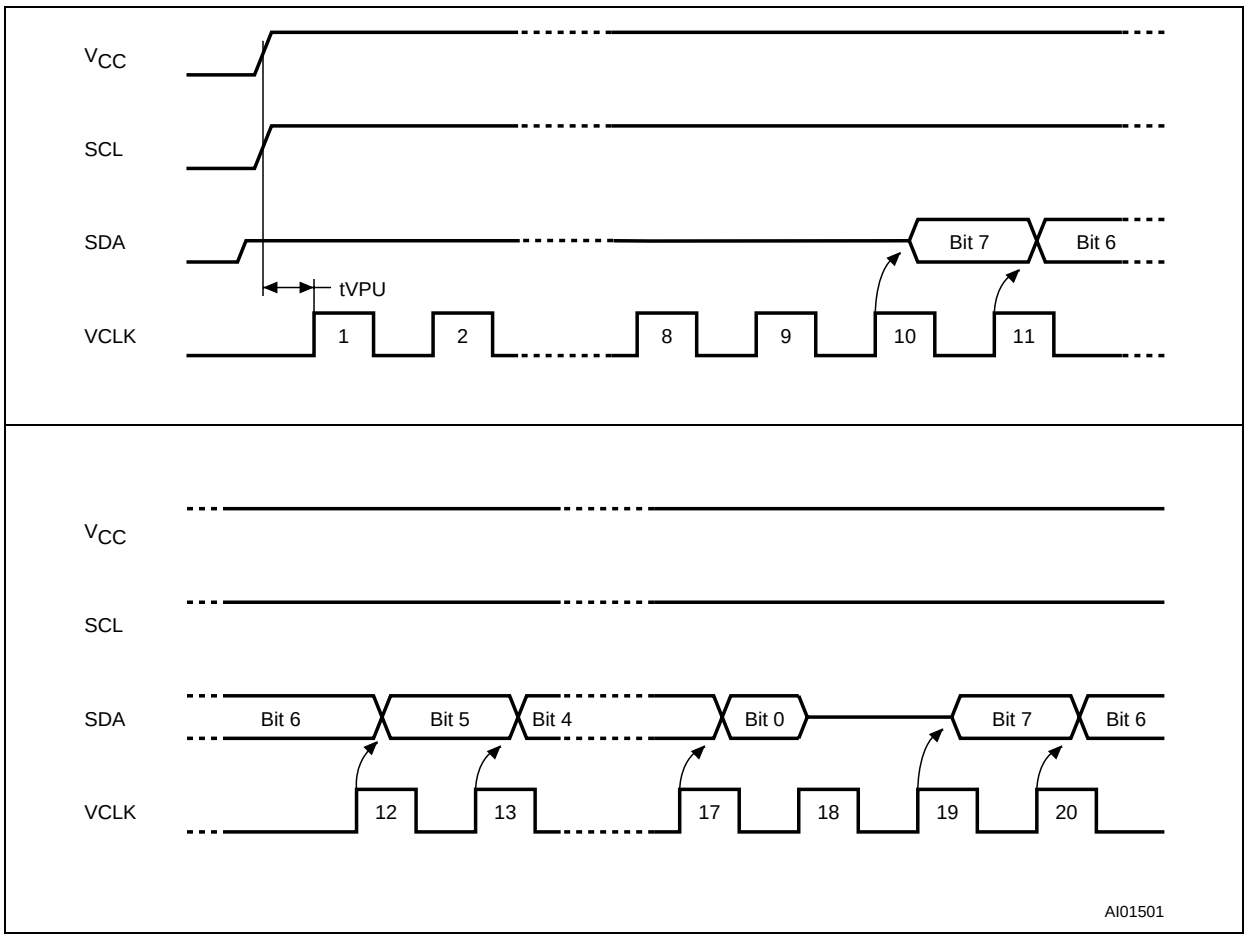
Figure 2 shows how, in the DDC1 mode, the ST24xy21 uses the VCLK input as a clock and the SDA line for data output. The EEPROM data are clocked out on the rising edge of VCLK signal (pin 7). The SCL input must be held high.

Figure 2. Summary of the Use of the ST24xy21 in the DCC1 Mode



First, though, the device passes through an initial, internal, synchronization sequence, as depicted in Figure 3. VCLK is given nine free clock cycles, during which the SDA pin is held in its high impedance state. On the rising edge of the tenth VCLK pulse, the device starts to output, on the SDA line, the data byte that is located at address 00h. This is transmitted serially, during the next nine clock cycles. The first eight cycles are used for transmitting the data bits themselves, with the most significant bit first. During the ninth cycle, the SDA line is held in its high impedance state. This last bit, therefore, is readable as a logic '1' due to the pull-up resistor on the SDA line.

Figure 3. Timing Diagram for the DDC1 Mode



The internal address register is incremented automatically, and the data at the next location is transmitted during the next nine clock periods. This cycle continues indefinitely, so long as the SCL line is held high, with the address wrapping round from 7Fh (the 127th byte) back to 00h.

Unlike the DDC2B mode, the DDC1 mode does not provide for the issuing of instructions or commands to the memory, and does not provide for the writing of data.

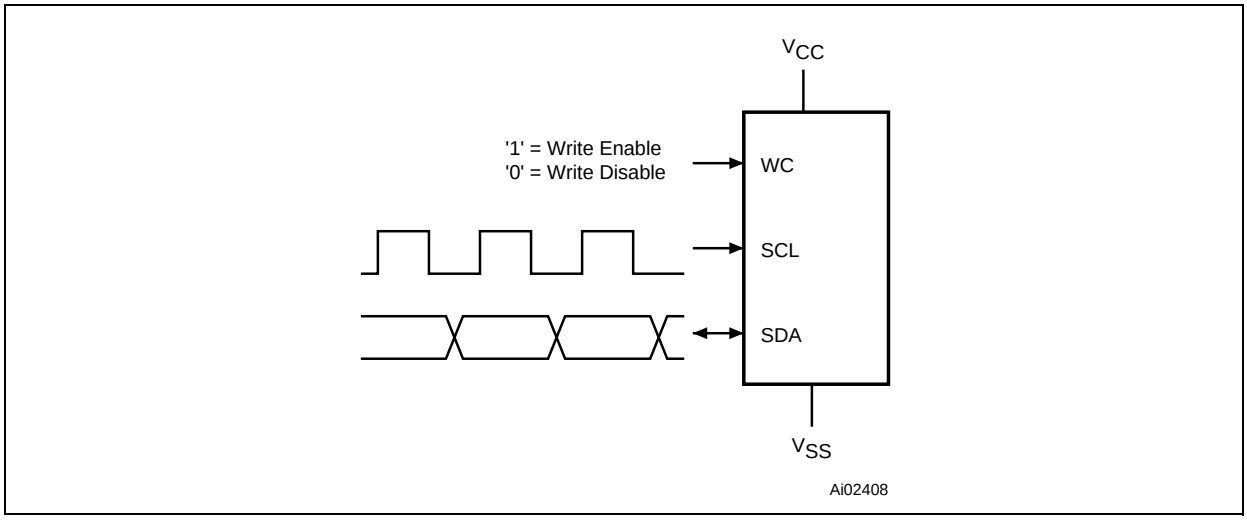
The detection of a logic ‘0’ for the ninth bit indicates that the memory has lost synchronization, and that the data are no longer valid. It is then necessary to re-synchronize the communication by turning off the power to the memory, and then back on again, or by checking the synchronization block of data written in the ST24xy21 device.

DDC2B: I²C Bidirectional Mode

The I²C standard two-wire serial interface includes a bidirectional data line (SDA) and a serial clock (SCL), as indicated in Figure 4. In addition, the whole ST24xxx and ST25xxx family offers a write control feature, as described in Application Notes *AN404* and *AN1006.* For the ST24xy21 family, this is appears as described in the following list:

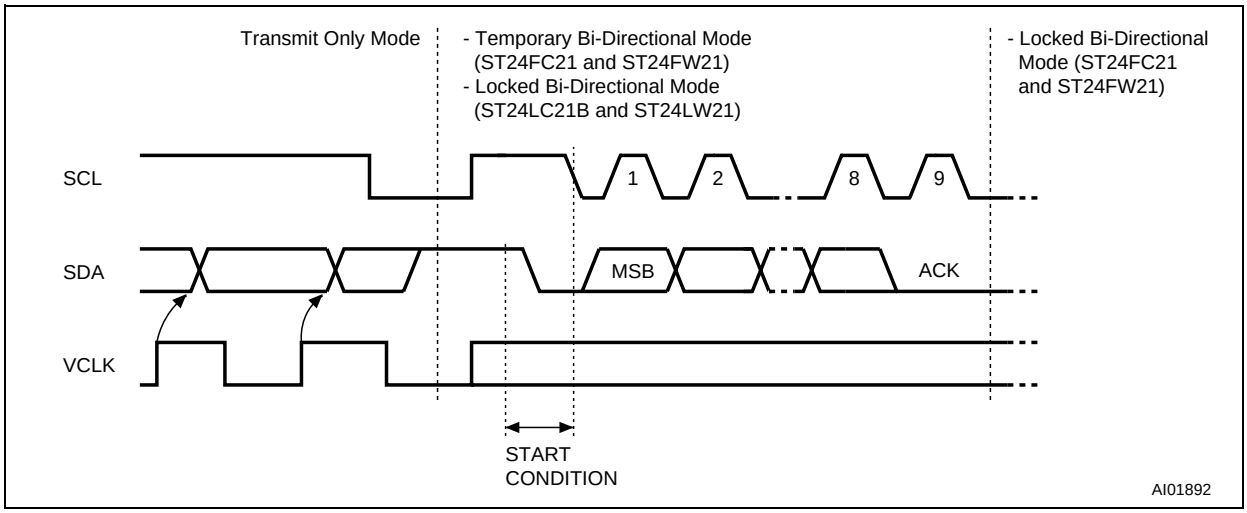
- When the ST24LC21B or ST24FC21 is in the DDC2B mode, the VCLK input (pin 7) acts as the write enable/$\overline{\text{disable}}$ control.
  - When VCLK = 1, write instructions are permitted
  - When VCLK = 0, write instructions are ignored.
- When the ST24LW21 or ST24FW21 is in the DDC2B mode, the Write Control input (WC), pin 3, acts as the write enable/$\overline{\text{disable}}$ control.
  - When WC = 1, write instructions are permitted
  - When WC = 0, write instructions are ignored.

Figure 4. Summary of the Use of the ST24xy21 in the DCC2B Mode



The ST24xy21 is switched from the DDC1 mode to the DDC2B mode by taking the SCL pin low, as indicated in Figure 5.

Figure 5. Timing for the Transition from DDC1 Mode to DDC2B Mode



The ST24xy21 takes the role of the slave device in the I^2C protocol, with all memory operations synchronized by the serial clock, SCL. The VCLK input (pin 7) is ignored during read accesses, but for the ST24FC21 and ST24LC21B, it has an effect on write accesses, as described on page 7.

Table 2 shows that all read and write operations are initiated by a START condition generated by the bus master. The START condition is followed by a stream of 7 device select bits (transmitted with the most significant bit first), plus one read/write bit, and is terminated by an acknowledge bit.

Table 2. Device Operations

Mode	R/$\overline{W}$ bit	ST24LC21B ST24FC21 VCLK/WC[1]	ST24LW21 ST24FW21 WC[1]	Bytes	Initial sequence
Current address read	1	X	X	1	START, device select, R$\overline{W}$ = 1
Random address read	0	X	X	1	START, device select, R$\overline{W}$ = 0, address
	1	X	X		reSTART, device select, R$\overline{W}$ = 1
Sequential read	1	X	X	≥ 1	Similar to current or random read
Byte write	0	VIH	VIH	1	START, device select, R$\overline{W}$ = 0
Page write	0	VIH	VIH	8	START, device select, R$\overline{W}$ = 0

1. X = Don't Care = VIH or VIL

Table 3 shows how the stream of 7 device select bits is composed of the 4 bit Device Select code (built-in with the value 1010) followed by 3 Don't Care bits (X indicating that the bit can be either '0' or '1').

Table 3. Device Select Code in the DDC2B Mode

	Device code				Chip enable			$R\overline{W}$
Bit	b7	b6	b5	b4	b3	b2	b1	b0
Device select	1	0	1	0	X	X	X	$R\overline{W}$

When the bus master writes data to the memory, the ST24xy21 responds to the eight received data bits by asserting an acknowledge bit during the 9th bit time. When data is read by the bus master, it must acknowledge the receipt of the data bytes in the same way. Data transfers are terminated with a STOP condition (as described in descriptions of the READ and WRITE sequences in the *ST24XY21* data sheet).

CONTROL OF THE WRITE OPERATION

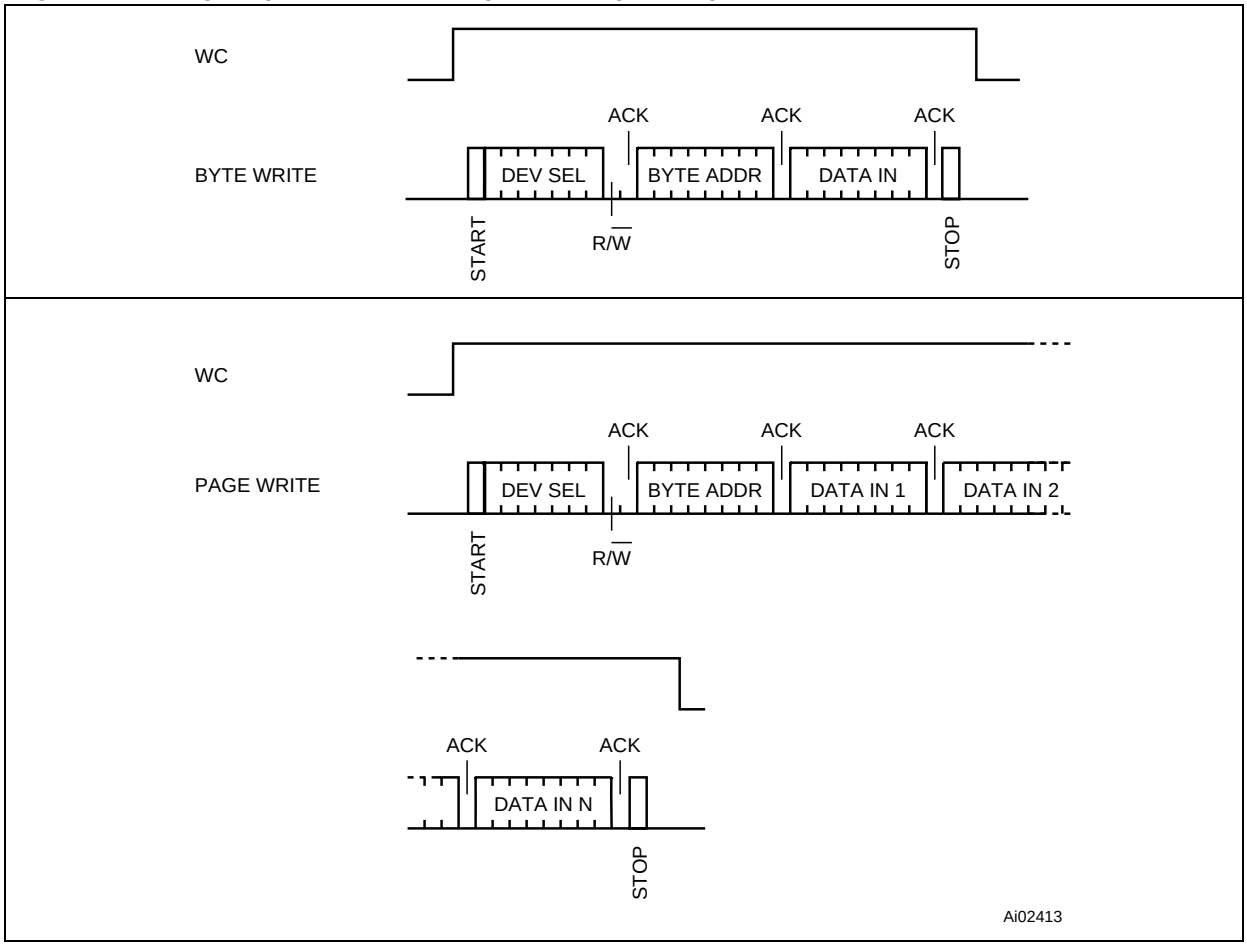
Hardware control of the write operation, using the WC input, is a useful facility for protecting the contents of the memory from inadvertent erase/write cycles (in the DDC2B mode). Not only does the device ignore the write operation if WC is not high at the start of the operation, but it aborts the operation if WC ceases to be held high, perhaps because of a noise glitch on the WC line. That is, the device errs on the side of safety, and protects itself against writing if there is any question as to the validity of the incoming data.

Table 4. Availability of the Write Control Input

	ST24FC21 ST24LC21B	ST24FW21 ST24LW21
DDC2B, I^2C Bidirectional Mode	pin 7 = WC	pin 7 = Don't Care pin 3 = WC
DDC1, Transmit Only Mode	pin 7 = VCLK	pin 7 = VCLK pin 3 = Don't Care

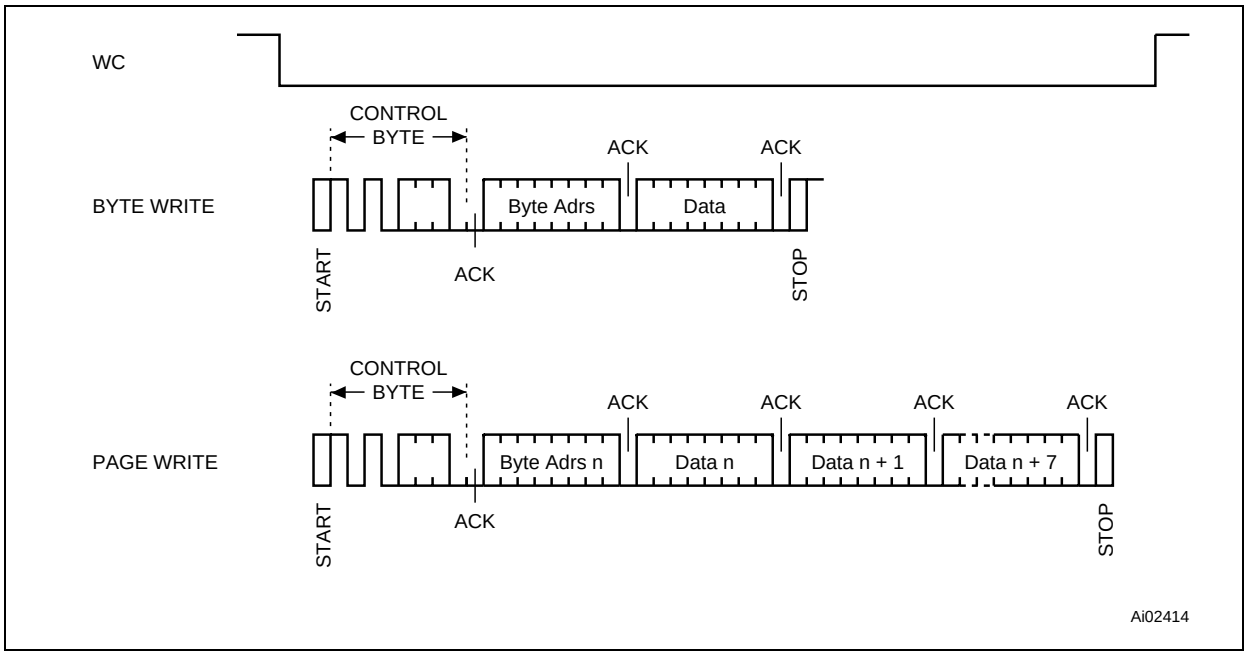
The availability of the WC input is summarized in Table 4. Writing is enabled when WC is held at VIH, and disabled when it is held at VIL. Figure 6 shows the timing of the byte-write and page-write operations, and shows how the level on the WC input must be taken high before commencing the START condition, and must be held high until after the STOP condition has finished.

Figure 6. Timing Sequence of Write Operations (WC = 1)



Write operations are ignored when WC is taken low, as depicted in Figure 7. However, the timing remains the same, with nine clock cycles per data byte, including an acknowledge bit at the end of each.

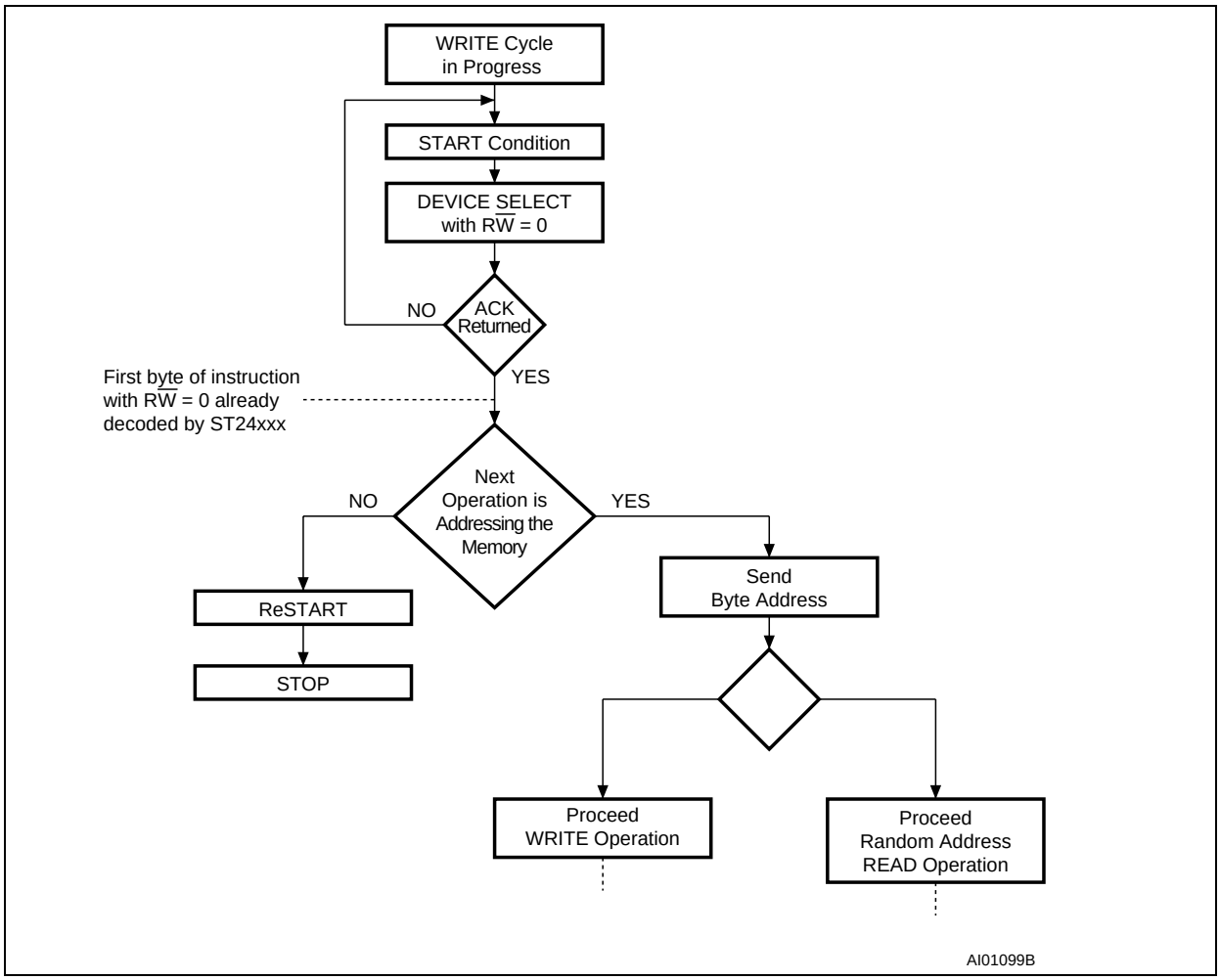
Figure 7. Timing Sequence of Inhibited Write Operations (WC = 0)



Because the device is designed to abort from a write operation if there is any question as to the validity of the incoming data, it is recommended that the status of the write operation be checked at completion.

The algorithm in Figure 8 shows an algorithm in which a test is made at the start of the write operation, to check that device has been correctly initiated. If the memory sends back the acknowledge after the first loop, no write cycle is in progress. This means that either the write sequence was corrupted by glitches or the signal applied on WC was not stable at VIH during the write sequence. This ACK polling algorithm must be used just after the write sequence because the memory will not send back the acknowledge while the internal write cycle is in progress.

Figure 8. The ACK Polling Algorithm (to check that the write cycle has started correctly)



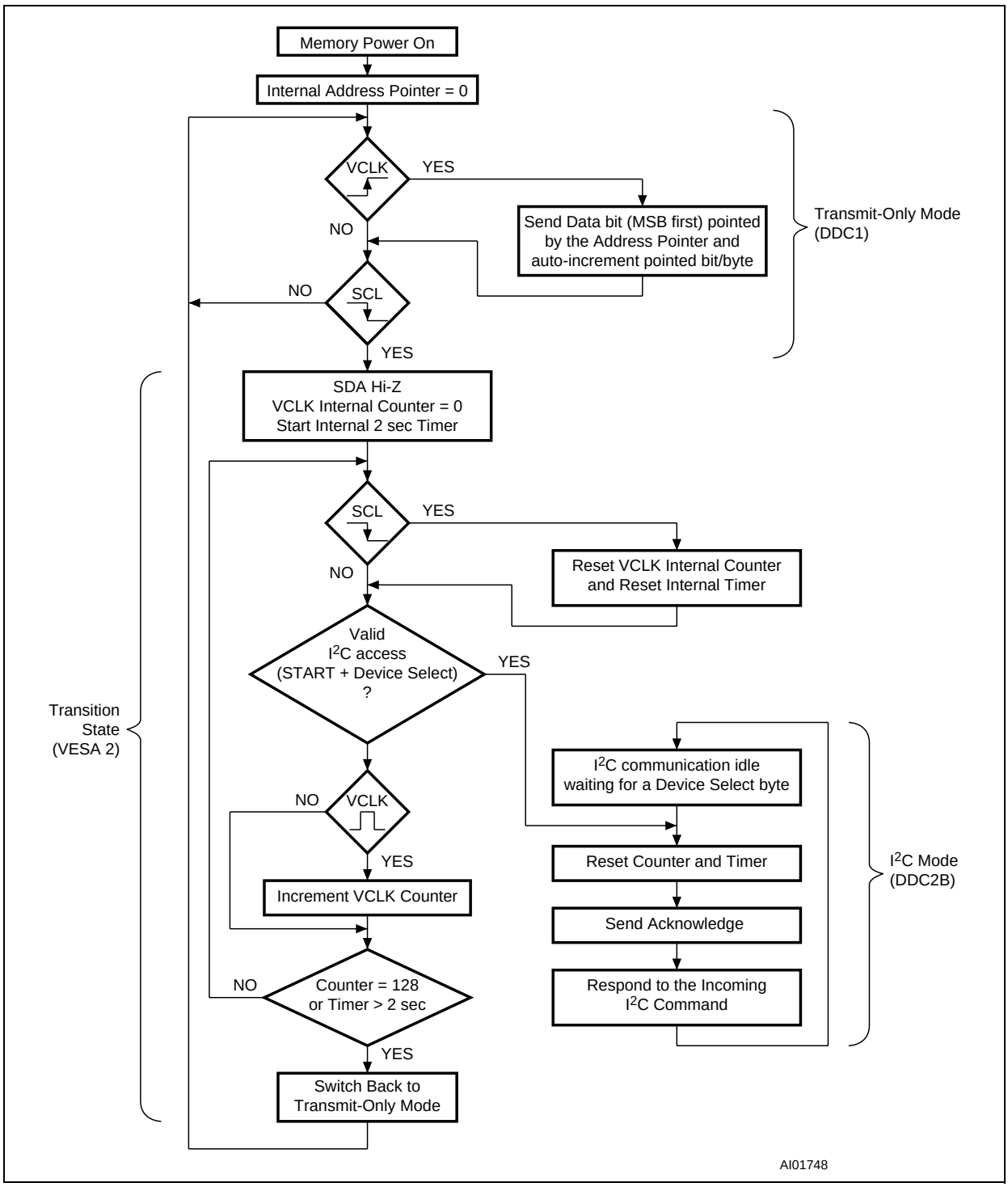
ERROR RECOVERY MODES (AVAILABLE ON ST24FC21 AND ST24FW21)

When the ST24FC21 or ST24FW21 first switches to the DDC2B mode, it enters a transition state, as shown in Figure 9.

If the device does not receive a valid I^2C sequence, that is a START condition followed by a valid Device Select code (1010XXX RW), within either 128 VCLK periods or a period of time of tRECOVERY (approximately 2 seconds), the device will return to the DDC1 mode. Whenever there is a high to low transition on the SCL input, the counter of the VCLK line and the tRECOVERY watchdog timer are both reset. If more than 128 VCLK pulses or tRECOVERY elapses between successive high to low transitions of SCL, the device returns to the DDC1 mode.

If, though, the device receives a valid I^2C sequence, it locks itself in the DDC2B mode.

Figure 9. Error Recovery Mechanism Flowchart (for the ST24FC21 and ST24FW21)



TYPICAL APPLICATION SCHEMATIC

The ST24xy21 is used in a Plug-and-Play PC display to transmit all the display information needed by the host PC in the DDC1 and DDC2B modes. In particular, during the PC boot-up and configuration process, the system software interrogates the display as to its capabilities and operating parameters.

The physical specification for the connector, between the display and the host PC graphics controller, is backward compatible to that of the standard 15-pin, VGA-type, connector. The pin-out of the VGA connector is described in Table 5. This shows how the host PC and the display connections vary, depending on the VDDC standard available in the host PC graphics controller.

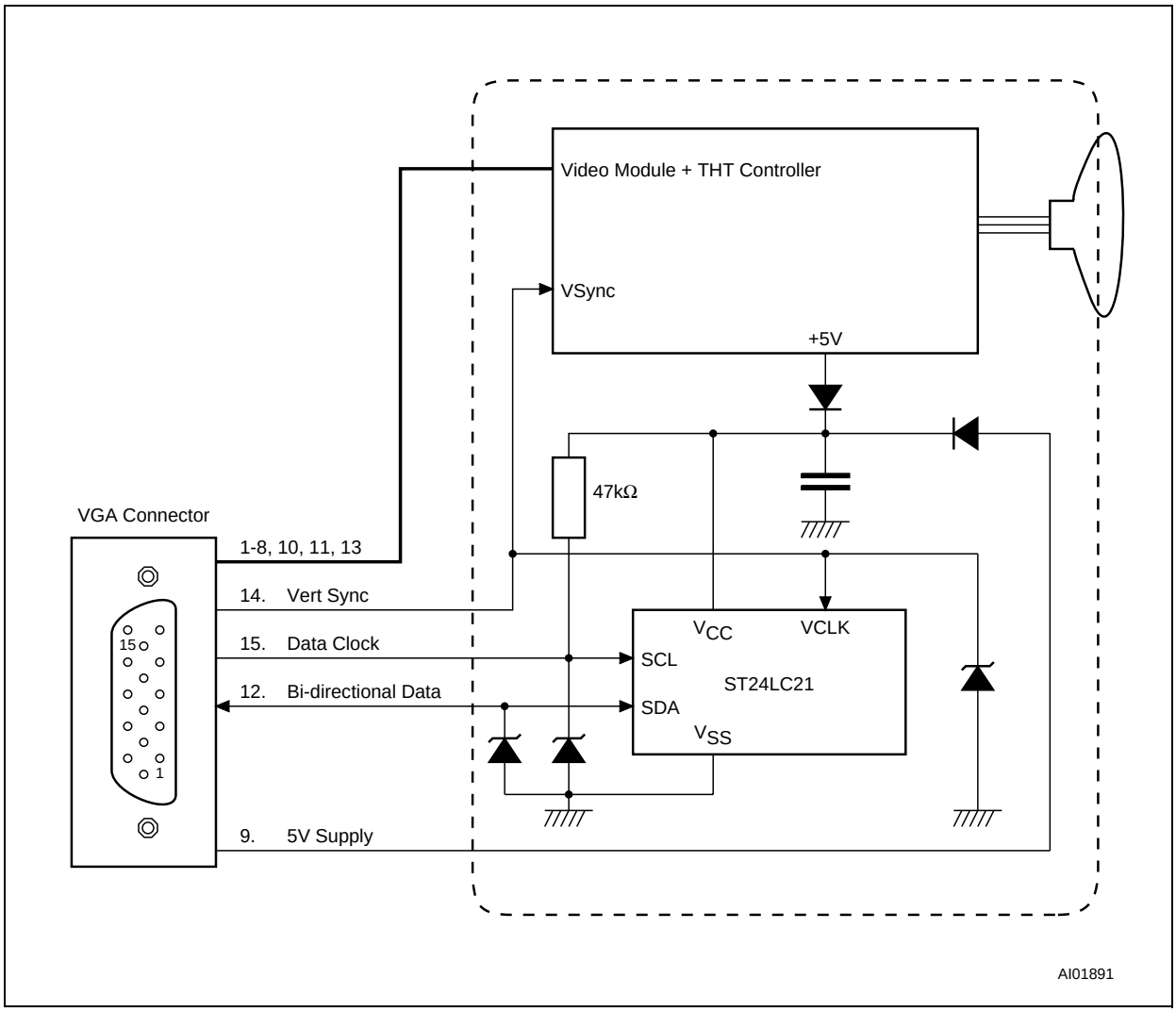
Table 5. 15-pin VGA Connector Pin-out Description

Pin	Standard VGA	DDC1 host PC	DDC2B host PC	DDC1/2B display
1	Red video	Red video	Red video	Red video
2	Green video	Green video	Green video	Green video
3	Blue video	Blue video	Blue video	Blue video
4	Display ID bit 2	Display ID bit 2	Display ID bit 2	Optional
5	Test (ground)	Return	Return	Return
6	Red video return	Red video return	Red video return	Red video return
7	Green video return	Green video return	Green video return	Green video return
8	Blue video return	Blue video return	Blue video return	Blue video return
9	no connection (mechanical key)	5 V supply	5 V supply	5 V supply
10	Sync return	Sync return	Sync return	Sync return
11	Display ID bit 0	Display ID bit 0	Display ID bit 0	Optional
12	Display ID bit 1	Data from display	Bidirectional data (SDA)	Bidirectional data (SDA)
13	Horizontal sync	Horizontal sync	Horizontal sync	Horizontal sync
14	Vertical sync	Vertical sync (VCLK output)	Vertical sync	Vertical sync (VCLK output)
15	Display ID bit 3	Display ID bit 3	Data clock (SCL)	Data clock (SCL)

According to Version 2.0 of the VESA Data Display Channel specification, the host PC graphics controller board needs to provide a 2.2 kΩ pull-up resistor on the bidirectional data line (SDA), and on the data clock line (SCL), to ensure correct switching between the DDC1 and DDC2B modes. The display PCB board also needs to provide a 47 kΩ pull-up resistor on the data clock line (SCL).

Figure 10 depicts a typical PC display application schematic using a member of the ST24xy21 family. The DDC1 clock signal, VCLK, is connected to pin 14 of the VGA connector. The data clock line, SCL, used for the DDC2B mode, is connected to pin 15 and the bi-directional data line, SDA, is connected to pin 12.

Figure 10. Schematic of a Typical PC Display Application



For the VESA 2.0 specification, a +5V supply voltage generated by the host PC is available on the pin 9 of the VGA connector (used for the ACCESS.bus protocol). This +5 V supply voltage may be used to supply the Vcc voltage of the ST24xy21. This allows a proper power-up sequence, driven only by the host PC. If the host PC and the display are powered-on asynchronously, the first to come on will power the ST24xy21 inside the display.

The SCL (the DDC2B clock) and SDA (data) pins of the ST24xy21 can be directly connected to the VGA connector. An ESDA6V1 transil array may be used in order to improve the memory protection against electrostatic discharge (ESD) and latch-up.

Diode protection is advisable on the signals that connect directly between the ST24xy21 and the external VGA connector. However, it is not necessary to provide external protection against slow rise and fall times or bounces, since the members of the ST24xy21 already contain TTL-compatible Schmitt-Triggers on these inputs.

POWER SUPPLY VOLTAGE IN THE VESA 2.0 SPECIFICATION

According to the VESA 2.0 specification, the ST24xy21 can be supplied by either the display or by the host PC power supply (using the +5 V line, pin 9, on the VGA cable). The easiest way to implement this is to use two diodes, as shown in Figure 10.

The ST24xy21 supply voltage is decreased by the diode forward voltage drop (about 0.6 V) and hence below 4.5 V. Nevertheless, the ST24xy21 remains operational, and no input will be damaged if the applied voltage on each input complies with the Absolute Maximum Ratings values. However, the threshold voltage of the Schmitt-Trigger (pin 7) needs to be decreased in this case (as described in the *ST24xy21* data sheet).

If you have any questions or suggestions concerning the matters raised in this document, please send them to the following electronic mail address:

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Please remember to include your name, company, location, telephone number and fax number.

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