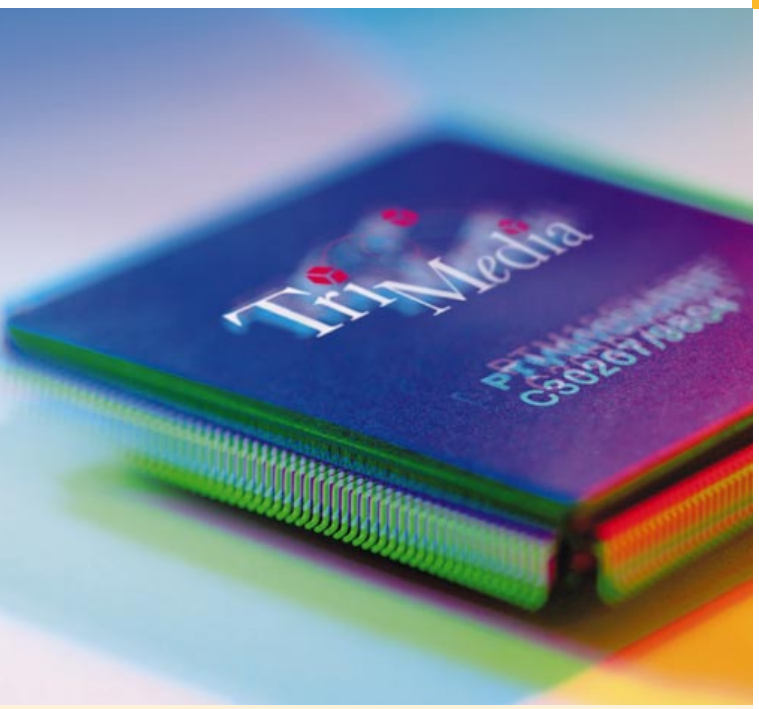
Programmable Media Processor

TriMedia TM-1100



On a single chip, a TriMedia™ TM-1100 delivers real-time processing of audio, video, graphics, and communications datastreams. With its low-cost 133-MHz CPU and a full complement of on-chip I/O and coprocessing peripheral units, the TM-1100 media processor delivers up to 5.3 BOPS to new multimedia products. 100% pin compatibility with the TM-1000 processor ensures that developers can take immediate advantage of up to 33% more processing power in their existing TM-1000 designs.

Comparable in programmability to a general-purpose processor, the TriMedia TM-1100 architecture enables development of multi-media applications entirely in the C and C++ programming languages. Programmability improves time-to-market, lowers development costs, and extends product life through software upgradability.

FEATURES

- Processes audio, video, graphics and communications datastreams on a single chip
- Powerful, fine-grain parallel, 133-MHz VLIW CPU with versatile instruction set includes special multimedia and DSP operations
- Pin compatibility with TM-1000 delivers up to 33% more performance to TriMedia TM-1000 designs
- Multiple, independent, DMA-driven multimedia I/O and coprocessing units format data and offload the CPU
- Enhanced video out functionality includes 7-bit alpha blending, full chroma keying, genlock capability, and programmable YUV color clipping
- PCI/XIO bus interface supports glueless interface to a mix of PCI and 8-bit microcomputer peripheral chips, such as ROM/Flash, EEPROM, 68K, and x86 devices
- Robust software development tools enable multimedia application development entirely in C/C++
- DVD playback authentication/descrambling functions for PC and standalone applications
- 16- and 64-Mbit SDRAM support up to 133-MHz

MULTIMEDIA APPLICATIONS

The TM-1100 is an ideal building block for any multimedia application that processes multiple multimedia and communications datastreams. It is well suited for creating a range of consumer and professional products such as videophones, videoconferencing and video editing systems, security systems, DVD encode/decode devices, and digital television appliances.

SINGLE-CHIP MULTIMEDIA ENGINE

Powered by a low-cost, 133-MHz, C-programmable CPU, the TriMedia TM-1100 strikes a perfect compromise between cost and performance. To streamline data throughput, TM-1100 incorporates independent on-chip DMA-driven peripheral units that manage datastream I/O and formatting and accelerate processing of key multimedia algorithms. To reap the full benefit of the CPU and processing units, TM-1100's sophisticated memory hierarchy manages internal I/O and streamlines access to external memory. The result — a single, low-cost programmable chip that powers standalone and PC-hosted multimedia products.

A single-chip multimedia engine

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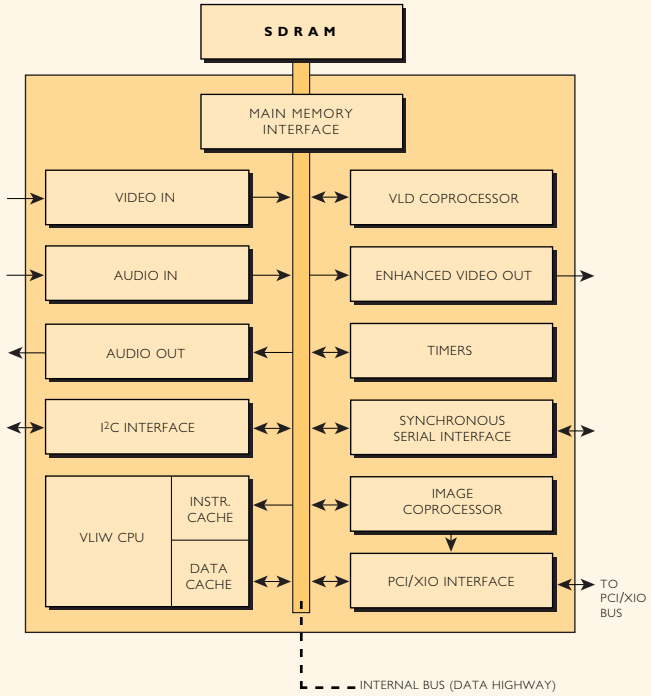


TM-1100 ARCHITECTURE
On a single chip, the TM-1100 incorporates a powerful CPU and peripherals to accelerate processing of audio, video, graphics, and communications data.

PROGRAMMABLE VLIW CPU

The TM-1100 delivers top performance through an elegant implementation of a very-long instruction word (VLIW) architecture. Key to the TriMedia processor's VLIW implementation, parallelism is optimized at compile time by the TriMedia compilation system. No specialized scheduling hardware is required to parallelize code during execution. Hardware saved by eliminating complex scheduling logic reduces cost and allows the integration of multimedia features that enhance the power of the CPU in multimedia applications.

The TM-1100 processor's powerful DSP-like, 32-bit CPU achieves fine-grain parallelism by simultaneously targeting five of its 27 pipelined functional units within one clock cycle. Most common operations have their results available in one clock cycle; more complex operations have multicycle latencies.

Functional units can access 128 fully general-purpose, 32-bit registers during execution. Since registers are not separated into banks, any operation can use any register for any operand. Both big and little endian byte ordering are supported.

The TriMedia TM-1100 CPU also provides special support for instruction and data breakpoints, useful in debugging and program development.

POWERFUL, DSP-LIKE, C-CALLABLE MULTIMEDIA OPS

In addition to traditional microprocessor operations and a full complement of 32-bit, IEEE-compliant, floating point operations, the TM-1100 instruction set includes multimedia and DSP operations that accelerate the performance of multimedia applications. Such multimedia operations can replace up to 11 traditional microprocessor operations. When incorporated into application source code, they dramatically improve performance and amplify the efficiency of the TM-1100's parallel architecture.

Multimedia operations are invoked with familiar function-call syntax consistent with the C programming language. They are automatically scheduled to take full advantage of the TriMedia processor's highly parallel VLIW implementation. As with all other operations generated by the TriMedia VLIW compilation system, the scheduler takes care of register allocation, operation packing, and flow analysis.

The TM-1100 processor enhances the multimedia operation set available for the TM-1000 with 6 additional operations that improve efficiency of MPEG-2 9-bit precise decoding, support video de-interlacing (median filtering), and more.

MEMORY SYSTEM OVERVIEW

To reap the full benefit of the TM-1100 processor's CPU and processing units, its memory hierarchy must read and write data (and instructions) fast enough to keep these units busy. Thus to meet the

TM-1100 Specifications

PHYSICAL

Process	C75: CMOS 0.35 micron; 5-layer metal
Packaging	TE_QFP
Pins	**total** 240 **I/O pins** 3.3 V with 5 V tolerance
Power	**supply** 3.3 V +/- 5% **dissipation** 6W (max) **consumption** 1808 mA 5.97 W **management** dynamic standby less than 990 mW

CENTRAL PROCESSING UNIT

Clock Speed	133 MHz
Instruction Length	variable (2 to 23 bytes); compressed
Instruction Set	arithmetic and logical ops, load/store ops., special multimedia and DSP ops., IEEE-compliant floating point ops.
Issue Slots	5
Functional Units	27, pipelined integer and floating-point arithmetic units, data-parallel DSP-like units

name	*quantity*	*latency*	*recovery*
constant	5	1	1
integer ALU	5	1	1
memory load/store	2	3	1
shift	2	1	1
DSPALU	2	2	1
DSP multiply	2	3	1
branch	3	3	1
float ALU	2	3	1
integer/float mul	2	3	1
float compare	1	1	1
float sqrt./divide	1	17	16

Registers	128 (32-bit width)
Special Multimedia/ DSP Operations	**total** 32 ops

MEMORY SYSTEM

Speed	66/80/100/133 MHz
CPU/Memory Speed Ratios	programmable; 1:1, 5:4, 4:3, 3:2, and 2:1
Memory Size	512 KB to 64 MB (up to four ranks)
Supported Types	16-Mbit SDRAM (x4, x8, x16); SGRAM (x32); 64-Mbit SDRAM (x32)
Width	32-bit bus
Max. Bandwidth	532 MB/sec (at 133 MHz)
Interface	glueless up to 4 16-Mbit or 2 64-Mbit chips at 133 MHz; more chips with slower clock and/or external buffers
Signal Levels	3.3 V LVTTL

CACHES

Access	**data** 8-, 16-, 32-bit word **instruction** 64 bytes
Associativity	8-way set-associative with LRU replacement
Block Size	64 bytes
Size	**data** 16 KB **instruction** 32 KB

INTERNAL DATA HIGHWAY

Protocol	64-byte block-transfer separate 32-bit data and 32-bit address buses

PCI INTERFACE

Speed	33 MHz
Bus Width	32-bit
Address Space	32 bits (4 GB)
Voltage	drive and receive at 3.3V or 5V
Standard Compliance	PCI Local Bus Specification 2.1

VIDEO IN

Supported Signals	CCIR 601/656 8-bit video up to 19 Mpix/sec raw 8-10-bit data (messages) up to 38 MB/sec
Image Sizes	all sizes, subject to sample rate
Functions	programmable on-the-fly 2X horizontal resolution subsampling

ENHANCED VIDEO OUT

Image Sizes	flexible, including CCIR601; maximum 4K x 4K pixels (subject to 80 MB/sec data rate)
Input Formats	YUV 4:2:2, YUV 4:2:0
Output Formats	CCIR601/656 8-bit video, PAL or NTSC
Clock Rates	programmable (4-80 MHz), typically 27 MB/sec (13.5 Mpixels/sec for NTSC, PAL)
Transfer Speeds	80 MB/sec in data-streaming and message-passing modes; 40 Mpix/sec in YUV 4:2:2 mode
Functions	full 129-level alpha blending, genlock mode, frame synchronization, chroma key, programmable YUV color clipping

AUDIO IN / AUDIO OUT

Number of Channels	2 input; 8 output
Sample Size	8- or 16-bit samples per channel
Sample Rates	1 Hz to 100 KHz programmable with 0.001 Hz resolution
Data Formats	8-bit mono and stereo; 16-bit mono and stereo PC standard memory data format
External Interface	4 pins each: 1 programmable clock output, 3 flexible serial input (AI) or output (AO) interface
Clock Source	internal or external
Native Protocol	I^2S and other serial 3-wire protocols

Multimedia application development entirely in C and C++

By enabling development of multimedia applications entirely in the C and C++ programming languages, the SDE dramatically lowers development costs, reduces time-to-market, and ensures code portability to next generation architecture.

ROBUST SOFTWARE DEVELOPMENT ENVIRONMENT

The TriMedia software development environment (SDE) includes a full suite of system software tools to compile and debug code, analyze and optimize performance, and simulate execution for the TM-1100 processor. By enabling development of multimedia applications entirely in the C and C++ programming languages, the SDE dramatically lowers development costs, reduces time-to-market, and ensures code portability to next generation architecture.

TRIMEDIA REAL-TIME OPERATING SYSTEM KERNELS

For multimedia applications requiring system resource and task management, the TM-1100 media processor supports the pSOS+™ embedded real-time operating system kernels. Developed by Integrated Systems, Inc. (ISI), the pSOS+ kernels are optimized to deliver the deterministic response essential for multimedia applications.

internal I/O requirements of its target applications, the TM-1100 couples substantial on-chip caches with a glueless memory interface.

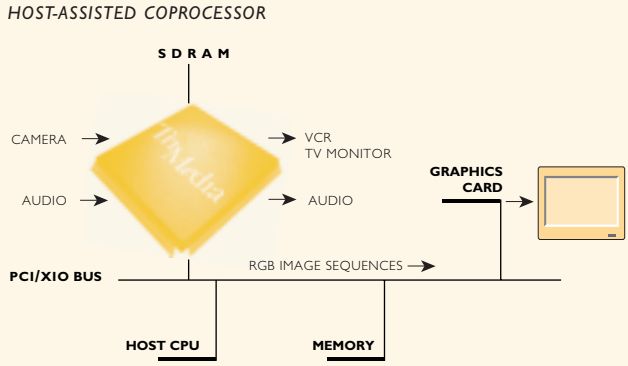
Dedicated instruction and data cache — TM-1100's CPU is supported by separate, dedicated on-chip data and instruction caches. Even without a second-level cache structure, TriMedia caches deliver media performance an order of magnitude greater than x86 processors.

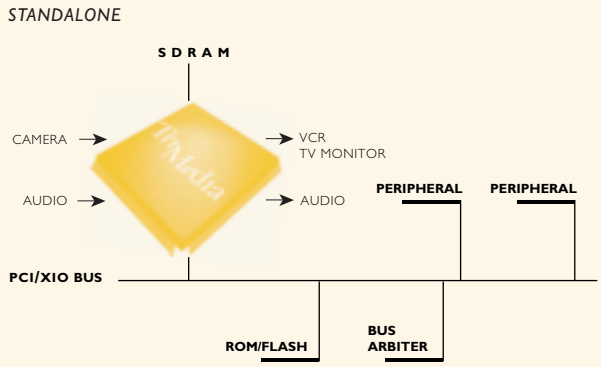
The dual-ported data cache allows two simultaneous accesses. It is non-blocking, thus cache misses and CPU cache accesses can be handled simultaneously. Early restart techniques reduce read-miss latency. Background copyback reduces CPU stalls.

To reduce internal bus bandwidth requirements, instructions in main memory and cache use a compressed format. The compressed instruction format improves the cache hit rate and reduces bus bandwidth. Instructions are compressed during compilation and decompressed in the instruction cache before being processed by the CPU.

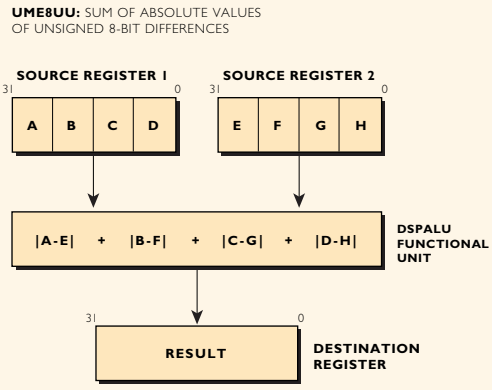
To improve cache behavior and thus performance, both caches have a locking mechanism. Cache coherency is maintained by software.

Glueless memory system interface — TM-1100's glueless main memory interface couples the on-chip caches and multimedia peripheral units to main memory (SDRAM). It acts as the SDRAM controller and programmable central arbiter that allocates SDRAM memory bandwidth for on-chip peripheral unit activities. Higher bandwidth SDRAM permits TM-1100 to use a narrower and simpler interface than would be required to achieve similar performance with standard DRAM.





TM-1100 is designed for use as a coprocessor in a PC-hosted environment or as the sole CPU in standalone systems.



SPECIAL MULTIMEDIA OPERATIONS
The ume8uu operation, commonly used for motion estimation in video compression, implements 11 simple operations in one TriMedia special op.

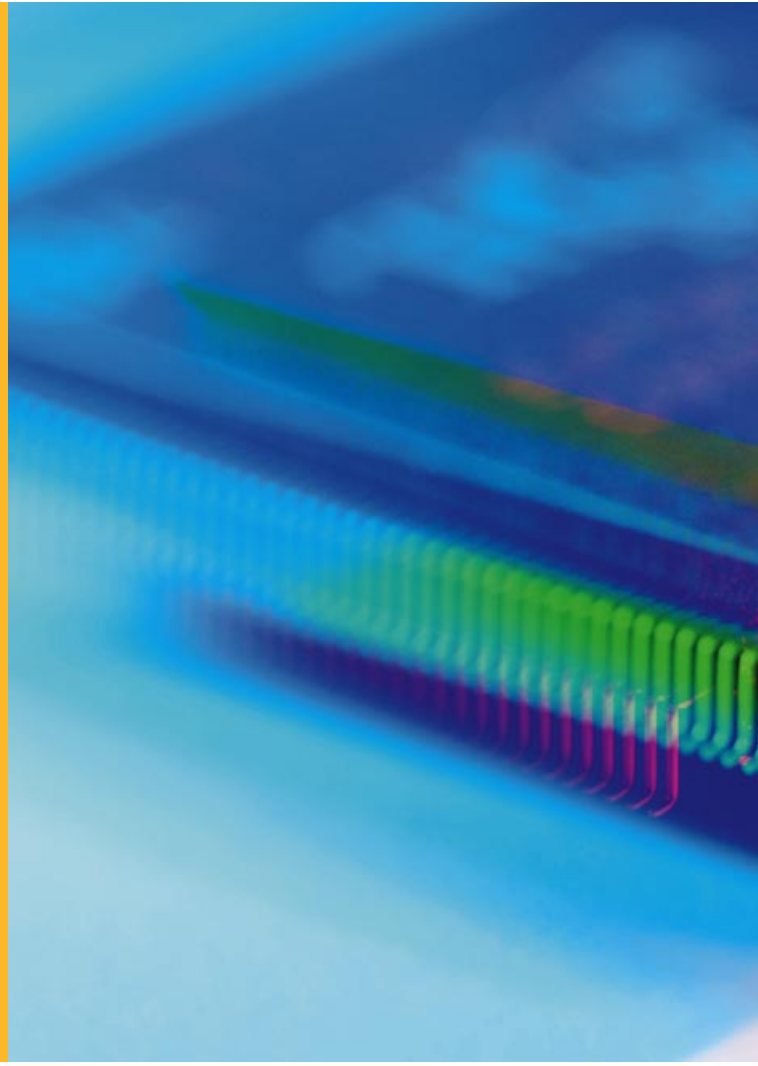
The TM-1100 memory interface provides sufficient capacity to drive a memory system consisting of up to 133-MHz, 8-MB (four 2Mx8) or 16-MB (two 2Mx32) SDRAMs. Larger memories can be implemented by using lower memory system clock frequencies or external buffers. Programmable speed ratios allow SDRAM to have a different clock speed than the TM-1100 CPU. Support for a variety of memory types, speeds, bus widths, and off-chip bank sizes allow a range of TM-1100-based systems to be configured.

HIGH-SPEED INTERNAL BUS (DATA HIGHWAY)

The memory system interface also mediates bandwidth allocation of the TM-1100's on-chip central data highway. A high-speed internal bus consisting of separate 32-bit address and data buses, the data highway connects the CPU and all on-chip I/O and coprocessing units to external SDRAM (through the memory interface) and to an off-chip PCI or XIO bus (through the PCI/XIO interface). Programmable bandwidth enables the data highway to deliver real-time responsiveness in a variety of multimedia applications.

On-chip multimedia I/O & coprocessing units

To streamline data throughput, TM-1100's independent DMA-driven peripheral units manage I/O, format video, audio, graphics, and communications datastreams, and perform operations specific to key multimedia algorithms.



MULTIMEDIA I/O AND COPROCESSING UNITS

Video input — The video input (VI) unit reads digital video datastreams from an off-chip source into main memory. The VI unit accepts input from CCIR656-compliant devices that output 8-bit parallel, 4:2:2 YUV time-multiplexed video data, such as digital video cameras, digital video decoders, or devices connected through ECL-level converters to the standard D1 parallel interface. After input, YUV data is demultiplexed, subsampled as needed, and written to SDRAM.

The VI unit can be programmed to perform on-the-fly 2X horizontal resolution subsampling. This enables high-resolution images (640- or 720-pixels/line) to be captured and converted to 320- or 360-pixels/line without burdening the CPU. When lower resolution video is eventually desirable, performing subsampling during data capture reduces initial storage and bus bandwidth requirements. The VI unit can receive raw data and unidirectional messages from another TM-1100's video out port.

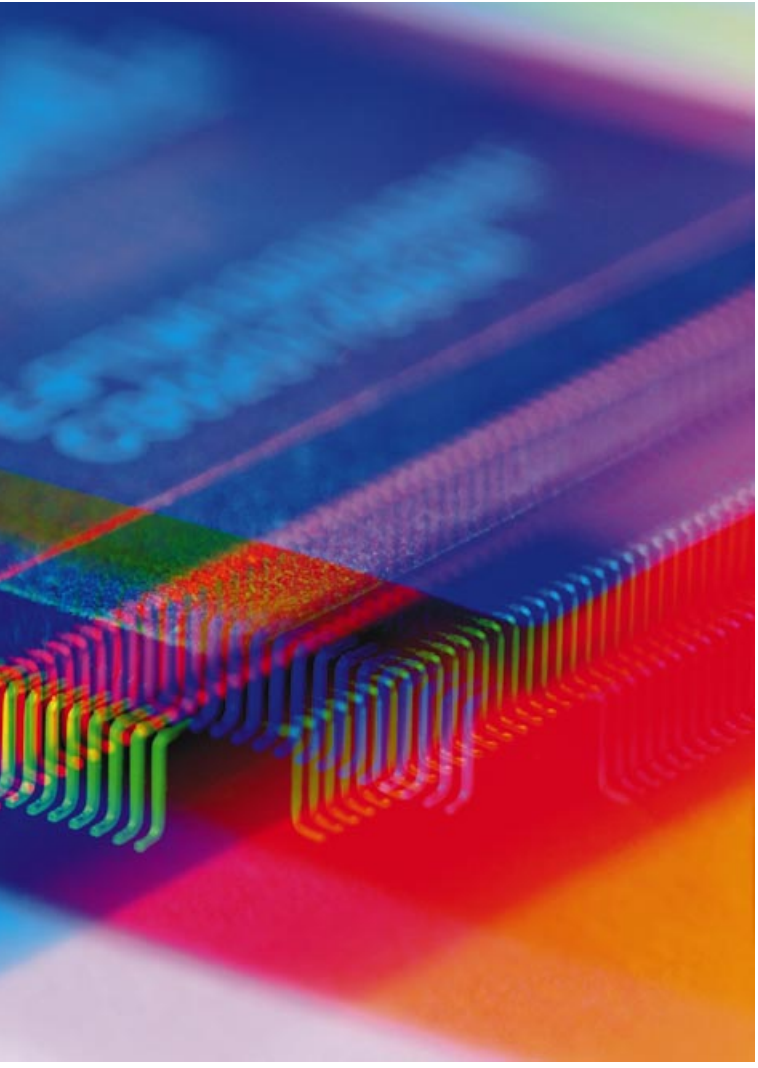
Enhanced video output — The enhanced video out (EVO) unit outputs a digital YUV datastream to off-chip video subsystems such as a digital video encoder chip, digital video recorder, or other CCIR656-compatible device. The output signal is generated by gathering bits from the separate Y, U, and V data structures in SDRAM.

The EVO unit can either supply or receive video clock and/or synchronizing signals from the external interface. Clock and timing registers can be precisely controlled through programmable registers. Programmable interrupts and dual buffers facilitate continuous data streaming by allowing the CPU to set up a buffer while another is being emptied by the EVO unit.

While generating the multiplexed stream, the EVO unit can perform programmed tasks, including optional horizontal 2X upscaling to convert from CIF/SIF to CCIR 601 resolution. For simultaneous display of graphics and live video, the EVO unit can perform 129-level alpha blending to generate sophisticated graphics overlays of arbitrary size and position within the output image. Chroma keying, genlock frame synchronization, and programmable YUV output clipping are also supported. The EVO unit can also pass raw data and unidirectional messages to another TriMedia processor.

Audio input and audio output — Together the audio input (AI) and audio output (AO) units provide all signals needed to interface to most high-quality, low-cost serial audio D/A and A/D converters. Both audio units are highly programmable, providing tremendous flexibility in developing custom datastream handling, adapting to custom protocols, and upgrading to support future audio standards.

The audio peripheral units connect to off-chip stereo converters through flexible bit-serial interfaces. The AI unit supports one or two channels of audio input; the AO unit delivers up to eight channels of



output. Eight-bit mono and stereo and 16-bit mono and stereo PC standard memory data formats are supported. The AO unit can be used to control highly integrated PC codecs.

Driven by TM-1100, the programmable audio sampling clock supports rates from 1 Hz to 100 KHz. High resolution of .001 Hz gives programmers subtle control over sampling frequency enabling audio and video synchronization in even the most complex configurations.

Image coprocessor — The image coprocessor (ICP) offloads the TriMedia CPU of several image processing and manipulation tasks such as copying an image from SDRAM to a host's video frame buffer. The ICP can operate as either a memory-to-memory or a memory-to-PCI coprocessor device. In memory-to-memory mode, the ICP can perform horizontal or vertical image filtering and scaling. In memory-to-PCI modes, it can perform horizontal scaling and filtering followed by YUV to RGB color-space conversion for screen display.

The ICP also provides display support for live video in overlapping windows. The number and sizes of windows processed are limited only by available bandwidth. The final resampled and converted image pixels are transmitted over the PCI/XIO bus to an optional off-chip graphics card/frame buffer.

Variable length decoder — TM-1100's variable length decoder (VLD) unit offloads the CPU of decoding Huffman-encoded video datastreams such as MPEG-1 and MPEG-2. It reads video streams from SDRAM and outputs a decoded stream optimized for MPEG-2 decompression software. This minimizes communications with the CPU where other portions of MPEG processing are performed.

DVD descrambler — The TM-1100 processor's digital versatile disc descrambler unit provides DVD authentication and descrambling functions internally. These features enables developers to add low-cost, flexible DVD-video playback functions in PC and standalone applications with a minimum of effort.

I2C interface — TM-1100's I^2C interface unit provides an external I^2C or compatible interface for use in hardware or software mode. In hardware mode, it can be used to connect and control a variety of I^2C multimedia devices. This allows TM-1100 to configure and inspect status of peripheral video devices such as digital decoders and encoders, digital cameras, parallel I/O expanders and more.

I^2C software operation mode enables full control of the I^2C interface through software. The I^2C interface is also used to read the boot program from an off-chip EEPROM.

Synchronous serial interface — TM-1100's synchronous serial interface (SSI) unit provides serial access for a variety of multimedia applications, such as video phones or videoconferencing, and for general data communications in PC-based systems. The SSI unit contains all the buffers and logic necessary to interface with simple analog modem front ends. When used with the TriMedia V.34 software library, the SSI unit provides fully V.34-compliant modem capability. Alternatively, it can be connected to an ISDN interface chip to provide advanced digital modem capabilities.

Timers — The TM-1100 provides four general purpose timers useful for counting/timing events such as CPU clock cycles, data /instruction breakpoints, cache tracing, audio/video clocks, and more. Three timers are available to programmers, the fourth is reserved for system software. Each timer has a value that can be continuously inspected as needed for an application and an associated modulus that can be used to generate an interrupt when the timer's value reaches the modulus.

High-speed PCI/XIO bus interface — TM-1100's PCI/XIO interface unit connects the CPU and on-chip I/O and coprocessing units to a PCI/XIO bus. In embedded applications where TM-1100 is the main processor, this interface enables the TM-1100 to access off-chip devices that implement functions not provided by on-chip peripherals. In PC-based applications, the PCI/XIO interface connects TM-1100 to a standard PCI bus, allowing it to be placed directly on the PC mainboard or on a plug-in card. For low-cost standalone systems, XIO allows glueless connection of 8-bit x86 or 68K peripheral devices such as ROM, Flash, EEPROM, UARTs, etc.

TM-1100 Specifications

IMAGE COPROCESSOR

Functions	horizontal or vertical scaling and filtering of individual Y, U, or V horizontal scaling and filtering with color conversion and overlay: - YUV to RGB - RGB overlay and alpha blending - bit mask blanking
Scaling	programmable scale factor (0.2X to 10X)
Filtering	32-polyphase, each instance 5-tap, fully programmable filter coefficients
Performance	horizontal scaling and filtering: 80 MB/sec vertical scaling and filtering: 30 MB/sec horizontal scaling and filtering with color conversion: 33 Mpixels/sec peak for RGB output; 50 Mpixels/sec peak for YUV 4:2:2 output

VLD

Function	parses MPEG-1 and MPEG-2 elementary bitstreams generating run-level pairs and filling in macroblock header
External Interface	none

DVD DESCRAMBLER

Functions	authentication; descrambling
External Interface	none

I²C INTERFACE

Supported Modes	single master only
Addressing	7- and 10-bit
Rates	up to 400 kbps
External Interface	2 pins: 1 serial data, 1 clock

SYNCHRONOUS SERIAL INTERFACE

Data Formats	variable slots/frame
Frame Sync	external or internal
Clock Source	separate transmit, receive, frame sync transmit/receive clocks external source automatic frame sync error detection settable edge polarity for transmit, receive, and frame sync
External Interface	6 pins (2 can be used for tip and ring for phone connections); compatible with a majority of telecom devices can be configured with multiple chips

TIMERS

Number	4
Width	32-bits
Sources	external clock, (prescaled) CPU clock, data or instruction breakpoints, cache events, video in/out clocks, audio in/out word strobe, V.34 receive/transmit frame sync

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