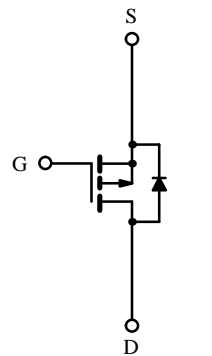
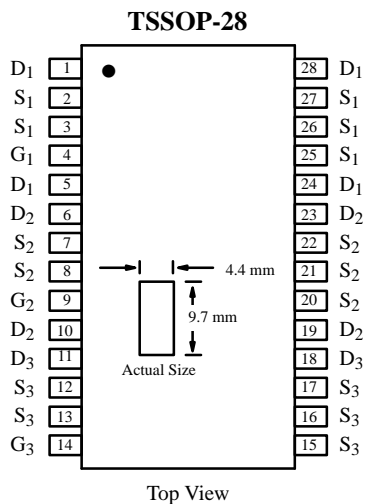


Triple P-Channel Enhancement-Mode MOSFET

Product Summary

V_{DS} (V)	$r_{DS(on)}$ (Ω)	I_D (A)
-30	0.040 @ $V_{GS} = -10$ V	± 4.5
	0.070 @ $V_{GS} = -4.5$ V	± 3.4

TrenchFET™
Power MOSFETs



*Source Pins 2, 3, 25, 26, and 27 must be tied common.

Source Pins 7, 8, 20, 21, and 22 must be tied common.

Source Pins 12, 13, 15, 16, and 17 must be tied common.

Absolute Maximum Ratings ($T_A = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Limit	Unit
Drain-Source Voltage	V_{DS}	-30	V
Gate-Source Voltage	V_{GS}	± 20	
Continuous Drain Current ($T_J = 150^\circ\text{C}$) ^a	I_D	$T_A = 25^\circ\text{C}$	± 4.5
		$T_A = 70^\circ\text{C}$	± 3.6
Pulsed Drain Current	I_{DM}	± 30	A
Continuous Source Current (Diode Conduction) ^a	I_S	-1.25	
Maximum Power Dissipation ^a	P_D	$T_A = 25^\circ\text{C}$	1.5
		$T_A = 70^\circ\text{C}$	1.0
Operating Junction and Storage Temperature Range	T_J, T_{stg}	-55 to 150	$^\circ\text{C}$

Thermal Resistance Ratings

Parameter	Symbol	Limit	Unit
Maximum Junction-to-Ambient ^a	R_{thJA}	83	$^\circ\text{C}/\text{W}$

Notes

a. Surface Mounted on FR4 Board, $t \leq 10$ sec.

Updates to this data sheet may be obtained via facsimile by calling Siliconix FaxBack, 1-408-970-5600. Please request FaxBack document #1817. A SPICE Model data sheet is available for this product (FaxBack document #5159).

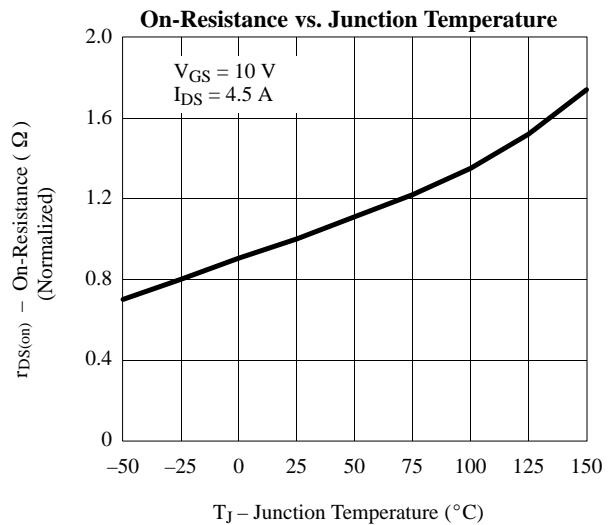
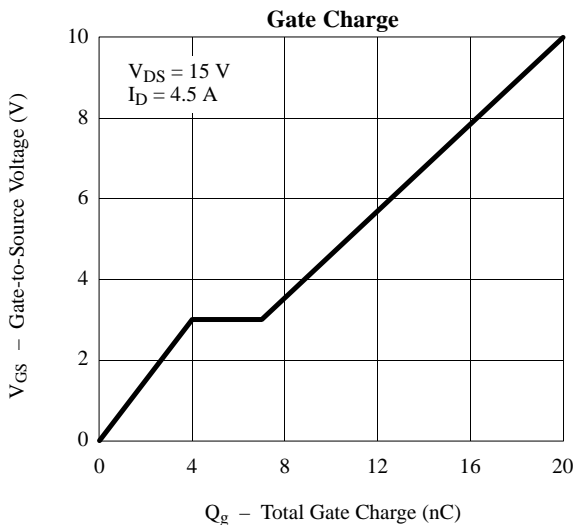
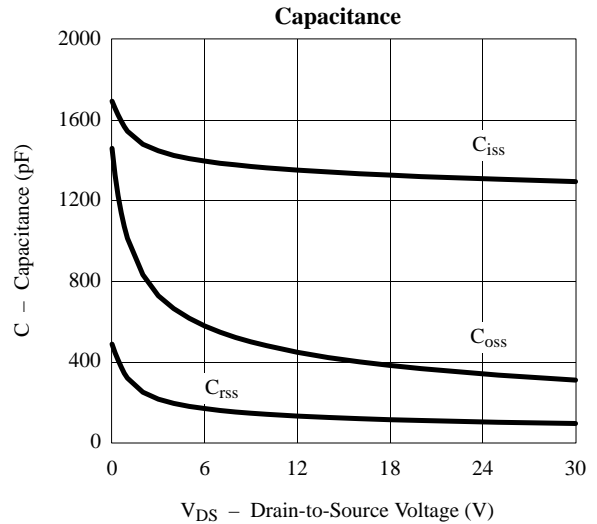
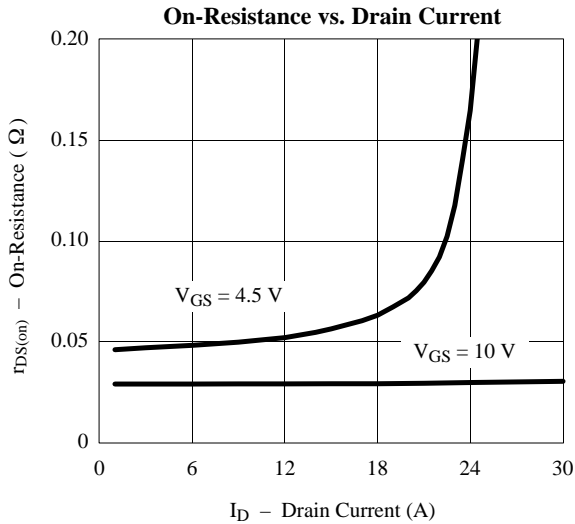
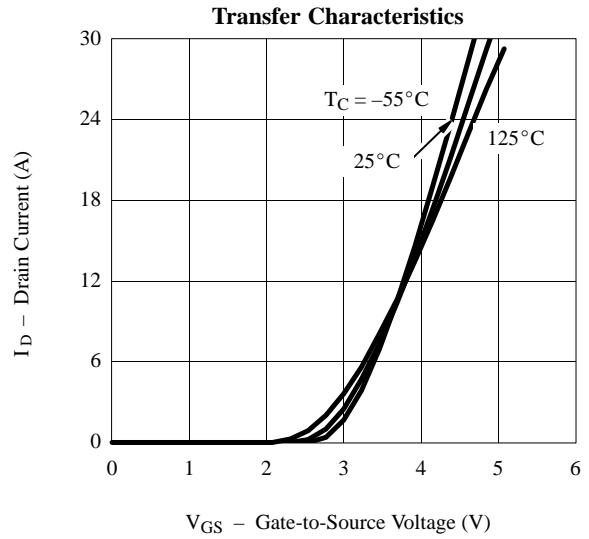
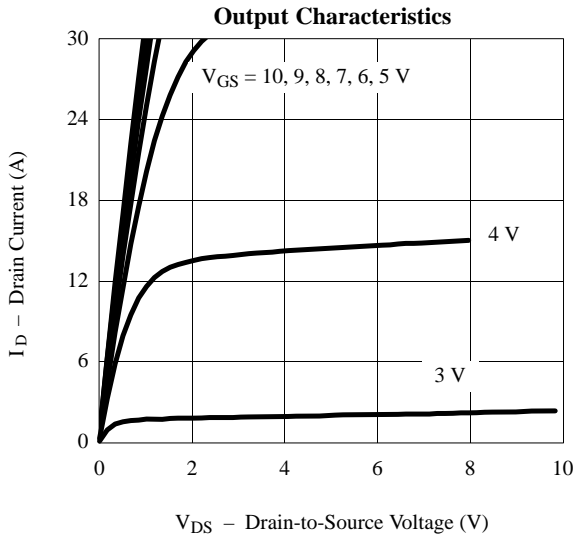
Specifications ($T_J = 25^\circ\text{C}$ Unless Otherwise Noted)

Parameter	Symbol	Test Condition	Min	Typ	Max	Unit
Static						
Gate Threshold Voltage	$V_{GS(th)}$	$V_{DS} = V_{GS}, I_D = -250 \mu\text{A}$	-1			V
Gate-Body Leakage	I_{GSS}	$V_{DS} = 0 \text{ V}, V_{GS} = \pm 20 \text{ V}$			± 100	nA
Zero Gate Voltage Drain Current	I_{DSS}	$V_{DS} = -30 \text{ V}, V_{GS} = 0 \text{ V}$			-1	μA
		$V_{DS} = -30 \text{ V}, V_{GS} = 0 \text{ V}, T_J = 55^\circ\text{C}$			-25	
On-State Drain Current ^a	$I_{D(on)}$	$V_{DS} = -5 \text{ V}, V_{GS} = -10 \text{ V}$	-20			A
Drain-Source On-State Resistance ^a	$r_{DS(on)}$	$V_{GS} = -10 \text{ V}, I_D = -4.5 \text{ A}$		0.029	0.040	Ω
		$V_{GS} = -4.5 \text{ V}, I_D = -3.5 \text{ A}$		0.045	0.070	
Forward Transconductance ^a	g_{fs}	$V_{DS} = -15 \text{ V}, I_D = -4.5 \text{ A}$		9.0		S
Diode Forward Voltage ^a	V_{SD}	$I_S = -1.25 \text{ A}, V_{GS} = 0 \text{ V}$		-0.8	-1.2	V
Dynamic^b						
Total Gate Charge	Q_g	$V_{DS} = -15 \text{ V}, V_{GS} = -10 \text{ V}, I_D = -4.5 \text{ A}$		20	35	nC
Gate-Source Charge	Q_{gs}			4.0		
Gate-Drain Charge	Q_{gd}			3.3		
Turn-On Delay Time	$t_{d(on)}$	$V_{DD} = -15 \text{ V}, R_L = 15 \Omega$ $I_D \cong -1 \text{ A}, V_{GEN} = -10 \text{ V}, R_G = 6 \Omega$		15	25	ns
Rise Time	t_r			14	25	
Turn-Off Delay Time	$t_{d(off)}$			40	65	
Fall Time	t_f			15	25	
Source-Drain Reverse Recovery Time	t_{rr}	$I_F = -1.25 \text{ A}, di/dt = 100 \text{ A}/\mu\text{s}$		50	80	

Notes

- a. Pulse test; pulse width $\leq 300 \mu\text{s}$, duty cycle $\leq 2\%$.
 b. Guaranteed by design, not subject to production testing.

Typical Characteristics (25°C Unless Noted)



Typical Characteristics (25°C Unless Noted)

