TS-850S

DESCRIPTION OF COMPONENTS

RF UNIT (X44-3120-00)

Ref. No.	Use/Function	Operation/Condition/Compatibility
Q1	RX RF amplifier	22~30MHz
Q2,3	RX RF amplifier	22MHz or less
Q4	DC switch	K4 control
Q5	TX RF amplifier	Drive output
Q6,7	DC switch	
Q8~11	RX 1st mixer	f_{RX} → 73.05MHz
Q12	Ripple filter	
Q13	IF amplifier	73.05MHz
Q14	Buffer	
Q15	Mixer	73.05MHz → 8.83MHz for monitor
Q16,17	RX 2nd mixer	73.05MHz → 8.83MHz
Q18	RF amplifier	NB RF output
Q19	DC switch	NB gate
Q20	TX IF amplifier	8.83MHz
Q21	RF amplifier	For monitor, 8.83MHz
Q22	DC switch	
Q23,24	TX 2nd mixer	8.83MHz → 73.05MHz
Q26,27	TX 3rd mixer	73.05MHz → f_{TX}
Q28	RF amplifier	1st local amplifier
Q29	DC LPF	ACL keying
Q30,31	DC switch	On when ARPD or PT or TPD are "H"
Q32	DC switch	On when S1 is on or BPD is "H" and Q30 is off
Q33	DC switch	On when PDE is "L"
Q34	DC switch	On when Q31 is on
Q35	DC switch	On when TPD is on
Q36~38	DC amplifier	ALC amplifier
Q39	DC amplifier	SWR protection
Q40,41	DC amplifier	ALC amplifier
Q42	DC switch	
Q43	DC switch	TXB → RL
Q45~48	DC switch	
Q49	RF switch	OPn when TX
Q50	DC switch	On when PDE is "L"
Q51	DC switch	On when Q50 is on
Q52	DC switch	On when Q45 is on and Q51 is off
Q501	AF switch	On when VOB is "H"
Q502	DC switch	On when VOB is "H"
Q503	AF switch	On when VOA is "H" and VOB is "L"
Q601~603	RF amplifier	8.83MHz NB
Q604	DC amplifier	NB AGC
Q605	DC switch	On at noise pulse (NB1, NB2)
Q606	DC switch	On at noise pulse (NB2)
Q607	DC switch	On at noise pulse (NB1, NB2)
Q608	DC switch	On at noise pulse (NB2)
Q609	AF amplifier	FM microphone amplifier
Q610	AF switch	FM microphone mute
Q611	DC switch	On when Q612 is on
Q612	DC switch	On when Q613 is off
Q613	DC switch	On when NFB is "H"

DESCRIPTION OF COMPONENTS

Ref. No.	Use/Function	Operation/Condition/Compatibility
IC1,2	BCD Æ decimal	RF BPF selection
IC3	Serial data → decimal	8.83MHz and 455kHz IF filter selection
IC4	RF detection	TX monitor
IC5	Meter amplifier	VSF, VSR, ALC processor
IC601	Delay	Noise cycle discrimination
IC602	NAND	Noise cycle discrimination
IC603	Analog switch	NFM changeover
D1,2	Spike absorption	
D3	RF switch	On when RX
D4~27	RF switch	BPF switch
D28	DC switch	
D29	DC switch	On when 22~30MHz BPF is selected
D30	Zener diode	4.7V, VCC of IC1 and IC2
D31	RF switch	On whe TX
D32	Reverse current prevention	
D33,34	RF switch	On when AIP is on
D35,36	RF switch	On when 22MHz or more RF amplifier is selected
D37,38	RF switch	On when 22MHz or less RF amplifier is selected
D39	Reverse current prevention	
D40~43	RF switch	Off when NB blanking
D44	RF switch	On when RX
D45~56	RF switch	8.83MHz filter changeover
D57	RF switch	On when RX
D58	RF switch	ON when TX
D59	Zener diode	4.7V, VCC of IC3
D60	RF switch	On when TX
D61,62	Reverse current prevention	
D63	LED	Constant voltage source
D64	RF switch	On when RX
D65,66	RF switch	On when TX
D67~71	Reverse current prevention	
D73	Zener diode	Lowers the output power during reduced voltage
D74	LED	Constant voltage source
D75	Zener diode	3.6V voltage shift
D76	Reverse current prevention	
D77	Zener diode	12V external ALC voltage shift
D78	Reverse current prevention	
D79	Spike absorption	
D80~85	Reverse current prevention	
D86	RF switch	LO2 TX/RX changeover
D87,88	Reverse current prevention	
D89	CAR level adjustment	
D90	Spike absorption	
D91,92	Reverse current prevention	
D93,94	Voltage limiter	
D601	Detection	
D602~604	Reverse current prevention	
D605	Zener diode	-6.2V

TS-850S

DESCRIPTION OF COMPONENTS

FINAL UNIT (X45-1470-02)

Ref. No.	Use/Function	Operation/Condition/Compatibility
Q1	Pre-drive amplifier	Wide-band amplification of HF band
Q2,3	Drive amplifier	Push-pull wide-band amplification of HF band
Q4,5	Final amplifier	Push-pull wide-band amplification of HF band
Q6	Supply of bias for drive	Temperature compensation of drive
Q7	Supply of bias for final	Temperature compensation of final
Q8	Switching	
Q9	Temperature detection	1/2 : Power down 2/2 : Fan motor operation
D1	Temperature compensation	Temperature sensing of pre-drive
D2	Temperature compensation	Temperature sensing of drive
D3	Temperature compensation	Temperature sensing of final
D4	Absorption of surge voltage	For fan motor

DIGITAL UNIT (X46-308X-XX) 0-11 : K,K2,P,P2 0-21 : M,M2 0-22 : M3,M4 0-71 : X,X2 2-71 : E,E2 2-72 : E3,E4

Ref. No.	Use/Function	Operation/Condition/Compatibility
Q1	Signal switch	TU-8 control
Q2	Signal switch	Mode signal (FM, AM)
Q3	Signal switch	Mode signal (SSB, FSK)
Q4	Signal switch	Mode signal (CW), TX indication signal (TXI)
Q5,6	Signal switch	RX band signal (RB0~RB3)
Q7,8	Signal switch	Power down signal (BPD, TPD, ATPD)
Q9	Signal switch	AIP signal
Q10,11	Signal switch	TX band signal (TB0~TB3)
Q12,13	Signal switch	AT-300 control, input (TS, TT)
Q14,15	Signal switch	AT-300 control, output (TS, TT)
Q16	Signal switch	Transmission control (SS line)
Q19~21	Signal switch	AT control (PR11, PR12, PR21, PR22, APRE, SPED)
Q22	Signal switch	AT relay control (ATA)
Q23	Signal switch	Transmission control (KEY line)
Q24,25	Signal switch	Select control of signal channel (RDC, TDC)
Q26	Signal switch	DRU-1 control (STBY)
IC1,3	I/O port	8 bit x 3 x 2
IC2	I/O port	8 bit x 4, 4 bit x 1
IC4	Multiplexer	A/D data switching
IC5	A/D converter	8 bit, 8 channel
IC6	CPU	8 bit microprocessor
IC10	Address latch	Latches multiplexer address/data
IC11	Address decoder	Converts the address signal into a chip select signal for each IC
IC12	Chip select decode	Chip select combination for RAM
IC13	RAM	8 bit x 8192 (8 K byte)
IC14	Encoder gate array	Pulse count of encoder
IC15,16	Schmitt trigger	Encoder chattering absorption
IC17	Inverter	Buffer for personal computer interface input/output
IC18	ROM	8 bit x 32768 (32 K byte)
IC20	NAND gate	Electronic keyer speed oscillator
IC21	CPU	Electronic keyer control 4 bit microcomputer
IC22	EEPROM	Electronic keyer message memory EEPROM (1 bit x 2048)
IC23	Select system reset back up	Generate reset signal, select back up power of the IC13 RAM
IC24	Inverter	Reverse reset logic
IC25	Regulator	14V → 8V
IC26	Regulator	8V → 5V
IC601,602	Regulator	14V → 8V

DESCRIPTION OF COMPONENTS

Ref. No.	Use/Function	Operation/Condition/Compatibility
D1	Protective diode	Protection from SEMI/FULL switch
D2	Protective diode	Protection from AT START switch
D3,4	Protective diode	Protection from MIC DOWN/UP switch
D5	Protective diode	Protection from SS line
D6~12	Switching	Destination selection
D14	Protective diode	Protection from AT THRU/AUTO switch
D17	protective diode	AT THRU/AUTO switch line overshoot protection
D18,19	Protective diode	Protection from DASH/DOT switch
D20	Protective diode	Protection from KEY line
D22	Protective diode	Protection from DBC line
D601	Protective diode	Reverse power connection prevention
D602	Surge absorption	For final fan motor
D603	Voltage stability	Voltage effect prevention during fan starting

IF UNIT (X48-3080-00)

Ref. No.	Use/Function	Operation/Condition/Compatibility
Q1,2	3rd receiving mixer	Conversion of 8.83MHz to 455kHz
Q3	Gain down for 28MHz	
Q4	Receiving IF amplifier	
Q5	LO3 amplifier	8.375MHz
Q6,7	1st transmission mixer	Conversion of 455kHz to 8.83MHz
Q8	Speech processor amplifier	
Q9	Transmission IF buffer	455kHz
Q10,11	Differential amplifier for notch	
Q12	Buffer for notch	
Q13~15	Receiving IF amplifier	455kHz
Q16	Receiving IF buffer	AM detection, AGC, and squelch
Q17	Buffer for AM detection	
Q18	AGC amplifier	
Q19~21	Squelch amplifier	
Q22	FM detection output low-pass filter	De-emphasis
Q23,24	FM S-meter amplifier	
Q25	CAR buffer	455kHz
Q26	Drive amplifier for modulation	
Q27	Squelch gate	
Q28	Monitor muting	
Q29~31	Side-tone switching	
Q32	Data amplifier	Amplifier for rear input
Q33	VOX amplifier	VOX gain
Q34	Keying	On at key down during CW mode
Q35	Switching	Stand-by for packet
Q36	Switching	RXB during other than FM mode, changeover of 455kHz filter
Q37	Switching	RXB during FM mode, changeover of 455kHz filter
Q38	Switching	When TDC is low, TDB is 8V
Q39	Switching	8V except transmission FM mode, muter signal of FM MIC amplifier
Q40	Switching	Voltage for RF gain except FM mode
Q41	Switching	Switching when AF AGC off
Q42	Switching	Changeover of HI BST
Q43	Switching	Squelch switching for packet
Q44	Switching	Keying when CW mode, key down except CW mode
Q45	Switching	Switching of RYB and SSBB
Q46	Switching	Switching of AMB and FMB

DESCRIPTION OF COMPONENTS

Ref. No.	Use/Function	Operation/Condition/Compatibility
Q47	Switching	8V when FM narrow mode
Q48	Switching	Switching of CWB
Q49,50	Switching	
Q51	Switching	Output of VOX module
Q52	Switching	Power source for muting of microphone when PKS is low
Q53-55	Switching	Inversion of FMB
Q56	Switching	Switching of squelch
Q57	Switching	For AGC on/off
Q58	Switching	Muting of reception
Q59	Switching	Switching when FM AGC off
Q60	Switching	Inversion of FMB
Q61	Switching	Inversion of RDB
Q62	Switching	Switching of IC5
Q63	Switching	Gain down when Am mode
Q64	Switching	
Q65	Switching	Inversion of SSBB and RYB
Q66	Switching	Stop carrier when receiving or when transmitting for DSP use
Q67	Switching	Switching of HI BST
Q68	Switching	VOX off when CW or FSK mode
Q69	Switching	Muting of input of FM IC when receiving
Q70	Active low-pass filter	Low-pass filter of IF output for DSP-100
Q71,72	Switching	Prevents transmission when power is on
Q73	Switching	RDB is 8V when RDC is low
Q74	Switching	Prevents transmission during mode changeover
IC1	Limiter	For speech processor
IC2	FM IF stage and DET	
IC3	Balanced modulator	
IC4	Product detector	
IC5	Receive audio muting	
IC6	Audio power amplifier	
IC7	Audio pre-amplifier	For monitor
IC8	Receive audio pre-amplifier	For monitor
IC9	Voltage select for RF gain	FM and the other
IC10	Time constant select of AGC	
IC11	Selector	For each mode of receiving audio signal
IC12	Selector	For DSP IN/OUT and through of receiving audio signal
D1	Switching	Changeover of tansmission/reception of LO3
D2	Switching	Changeover of transmission/reception of 455kHz IF filter (reception side)
D3,4	Switching	Changeover of 455kHz IF filter
D5,6	Switching	Changeover of transmission/reception of 455kHz IF filter (except FM reception)
D6-9	Switching	Changeover of 455kHz IF filter
D10	Switching	Changeover of transmission/reception of 455kHz IF filter (FM reception)
D11,12	Switching	Changeover 455kHz IF filter
D13,14	Switching	Changeover of transmission/reception of 455kHz IF filter (transmission side)
D15,16	Switching	Bypass of speech processor
D17	Switching	When speech processor is on
D18,19	Switching	Through circuit for transmission of 455kHz IF filter
D20	For notch tuning	
D23	Switching	Changeover of squelch SSB and FM
D24	Detection	FM S-meter detection
D27	Reverse current prevention	Upsets carrier balance during AM mode
D28	pin diode	Carrier level adjustment
D29	Reverse current prevention	SSBB and carrier volume

DESCRIPTION OF COMPONENTS

Ref. No.	Use/Function	Operation/Condition/Compatibility
D30	Reverse current prevention	Threshold squelch
D31	Detection	AGC squelch detection
D32	Detection	AM detection
D33	Reverse current prevention	Matching of AGO and FMB for AGC circuit off
D34	Reverse current prevention	CWB, RYB matching Æ RCB
D35	Reverse current prevention	CWB, RSB matching Æ CRSB
D36	Reverse current prevention	RYB, SSBB matching Æ RSB
D37	Reverse current prevention	Matching with inverse of MONS and RSB
D38	Reverse current prevention	Matching of RCB and TDB
D39	Reverse current prevention	Matching of VOX output and BK-SW output
D40	Reverse current prevention	Key lowering when key is not inserted
D41	Reverse current prevention	Matching of RBC and TXB
D42	Reverse current prevention	Stops operation of VOX when CW and FSK mode
D43	Reverse current prevention	Side-tone keying
D44	Reverse current prevention	Matching of RXB and TDB
D46	Switching	Changeover of analog modulator output and modulated output of DSP-100
D47	Reverse current prevention	Side-tone keying
D48	Detection	FM squelch detection
D49	Reverse current prevention	Matching of RXB and 8V other than FM mode
D50	Reverse current prevention	Squelch gate switching
D51	Reverse current prevention	Key line
D52	Reverse current prevention	Switching of monitor mute (RXB)
D53	Reverse current prevention	Matching of 45A selection and FM narrow switching
D54,55	Reverse current prevention	
D57	Switching	Switching of transmission carrier
D58	Switching	During transmission
D59	Limiter	Limiter for FM S-meter output
D60	Reverse current prevention	Noise sound countermeasures when power is on
D61,62	Reverse current prevention	Momentary transmission countermeasure when power is on
D63	Constant voltage	Stabilization of power of FM IC

PLL UNIT (X50-3130-00)

Ref. No.	Use/Function	Operation/Condition/Compatibility
Q1	VCO1-A	73.08~88.05MHz
Q2	VCO1-B	80.55~87.55MHz
Q3	VCO1-C	87.55~94.55MHz
Q4	VCO1-D	94.55~103.55MHz
Q5	Switching	VCO1-A changeover
Q6	Switching	VCO1-B changeover
Q7	Switching	VCO1-C changeover
Q8	Switching	VCO1-D changeover
Q9	Active LPF	Comparison : 500kHz
Q10,11	Active LPF	
Q12	Buffer	VCO1-A~D output, 73.08~103.05MHz
Q13	Buffer	IC6 mixer input, 73.08~103.05MHz
Q14	Buffer	LO1 output, 73.08~103.05MHz
Q15	Buffer	PLL IC3 input, 18.03~48.00MHz
Q16	Amplifier	PLL IC3 input, 18.03~48.00MHz
Q17	Amplifier	LO2 output, 64.22MHz
Q18~22	Active LPF	Comparison : 20kHz (5kHz when FM mode)
Q21	Reference oscillator	Reference signal : 20MHz
Q22	Buffer	Reference oscillator

DESCRIPTION OF COMPONENTS

Ref. No.	Use/Function	Operation/Condition/Compatibility
Q23	Amplifier	Reference output
Q24	Tripled circuit	10MHz x 3 = 60MHz
Q25	Amplifier	Frequency divider input
Q26	Active LPF	10kHz reference output
Q27	Switching	Low when unlock output
Q28	Switching	Power for TU-8
IC1	Mixer	1 : 55.05~55.55MHz output 2 : 60MHz input 5 : 4.45~4.49MHz input
IC2	AVR	+9V low drop-out
IC3	PLL	2,3,4 : Frequency division ratio input 5 : 10MHz input 7 : Lock voltage output 8 : Unlock output, Unlock : "H" 12 : 64.22MHz input
IC4	PLL	2,3,4 : Frequency division ratio input 5 : 10MHz input 7 : Lock voltage output 8 : Unlock output, Unlock : "H" 12 : 18.03~48.00MHz input
IC5	AVR	+5V
IC6	Mixer	5 : 73.08~103.05MHz input 11 : 55.05~55.55MHz input 13 : 18.03~48.00MHz output
IC7,8	Frequency divider	1/2 x 2, 1/5 x 2
D1	Vari-cap diode	VCO1-A
D2	Switching	VCO1-A output
D3	Vari-cap diode	VCO1-B
D4	Switching	VCO1-B output
D5	Vari-cap diode	VCO1-C
D6	Switching	VCO1-C output
D7	Vari-cap diode	VCO1-D
D8	Switching	VCO1-D output
D9	Switching	Unlock signal

CAR UNIT (X50-3140-00)

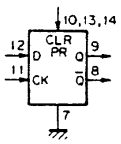
Ref. No.	Use/Function	Operation/Condition/Compatibility
Q1	Buffer	D/A buffer
Q2	Buffer	DLO1 buffer
Q3	Amplifier	20MHz fSTD
Q4	Buffer	D/A buffer
Q5,6	Switching	Chopper
Q7	Buffer	Output buffer for chopper
Q8,9	Amplifier	LO3
Q10	Buffer	D/A buffer
Q11,12	Switching	Chopper
Q13	Buffer	Output buffer for chopper
Q14,15	Amplifier	MCAR
Q16	Buffer	STON
Q17	Buffer	D/A buffer
Q18	Buffer	CAR
Q19	Level conversion	RTK
IC1	DDS	DLO1
IC2	DDS	LO3 sub-tone modulation
IC3	DDS	MCAR, STON, sub-tone generation
IC4	DDS	CAR, FSK modulation
IC5	Division	20MHz → 4MHz
IC6	Mixer	0.95~0.45MHz → 4.95~4.45MHz
IC7,8	Regulator	+5V
IC9	Buffer	20MHz fSTD

DESCRIPTION OF COMPONENTS

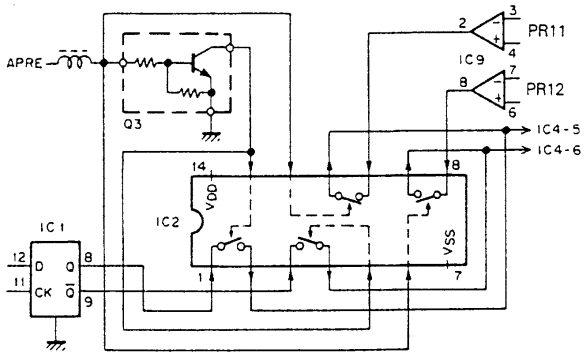
FILTER UNIT (X51-3100-00)

Ref. No.	Use/Function	Operation/Condition/Compatibility
Q1	Relay driver	10F relay
IC1	Band data decoder	
IC2	Relay driver	
D1	High-frequency rectification	Reflected wave rectification
D2	High-frequency rectification	Forward wave rectification
D3	Voltage stabilization	5V stabilization
D4,5	LPF changeover	18/21MHz common use
D6,7	LPF changeover	24/28MHz common use
D8	Relay surge absorption	1.6~2.0MHz LPF relay
D9	Relay surge absorption	2.0~4.0MHz LPF relay
D10	Relay surge absorption	4.0~7.5MHz LPF relay
D11	Relay surge absorption	7.5~10.5MHz LPF relay
D12	Relay surge absorption	10.5~14.5MHz LPF relay
D13	Relay surge absorption	14.5~21.5MHz LPF relay
D14	Relay surge absorption	21.5~30MHz LPF relay
D15	Relay surge absorption	Transmission/reception changeover relay
D16	Lightning surge protection	
D17,18	RF limiter	

AT UNIT (X53-3340-00)

Ref. No.	Use/Function	Operation/Condition/Compatibility
Q1,2	Amplifier	Waveform shaping
Q3	Switching	On when APRE is "H"
Q4,5	Switching	Motor speed control pulse
IC1	DFF	Phase difference detection  Function table

INPUTS		OUTPUTS	
CLOCK	D	Q	$\overline{Q}$
↑	L	L	H
L	X	Qo	$\overline{Qo}$

IC2	Analog switch	For control changeover motor 1 

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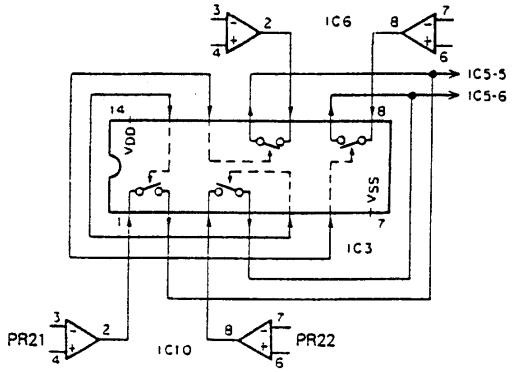
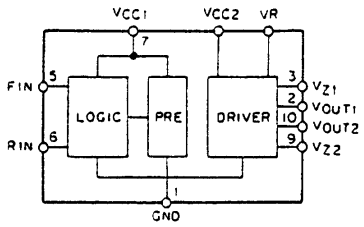
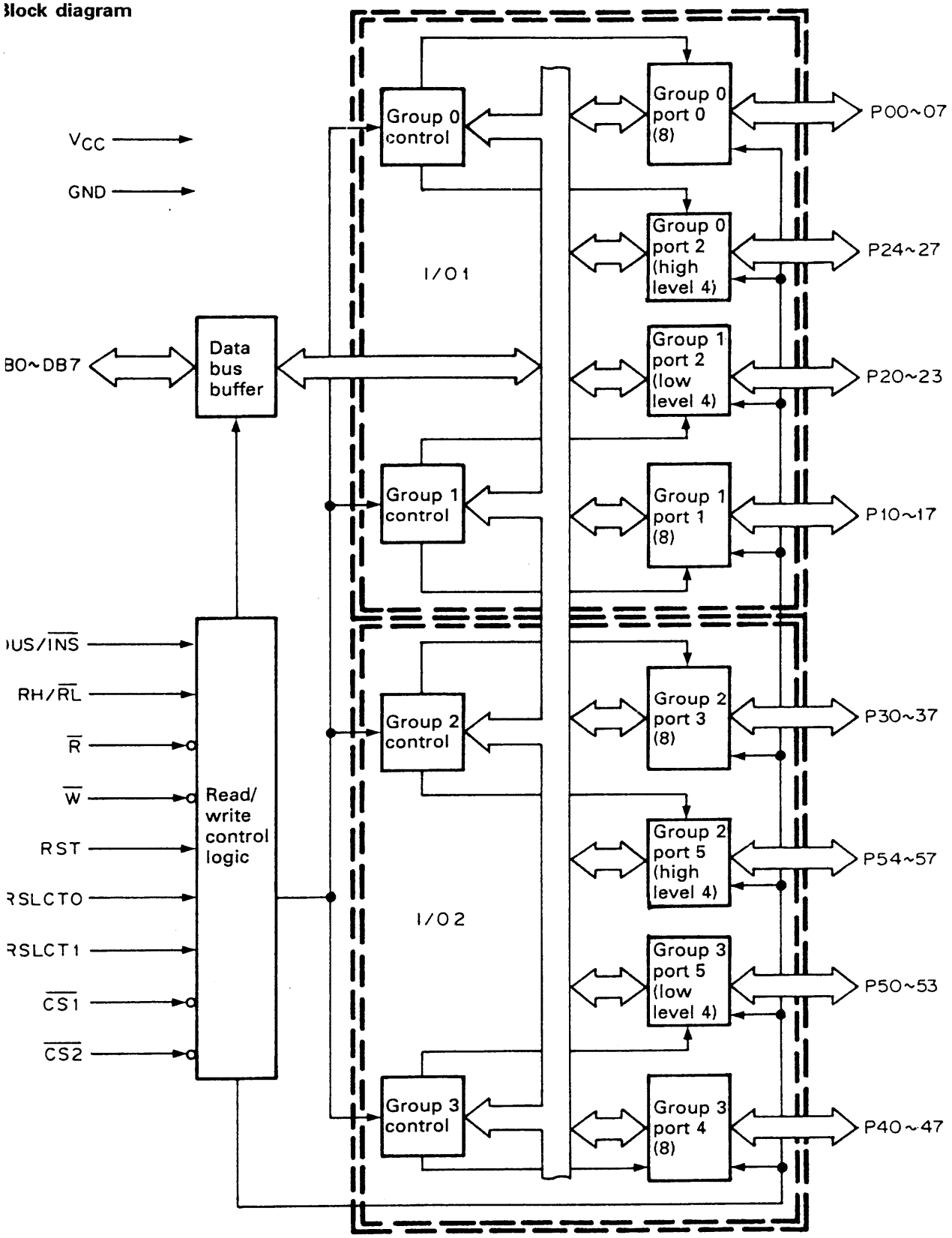
DESCRIPTION OF COMPONENTS

Ref. No.	Use/Function	Operation/Condition/Compatibility
IC3	Analog switch	For control changeover motor 2 
IC4	Motor drive	For motor 1 
IC5	Motor drive	For motor 2
IC6	Comparator	Amplification difference detection
IC7	AVR	+5V
D1	Detection	Current component amplification detection
D2	Detection	Voltage component amplification detection
D3~8	Switching	Clipper
D10	Switching	Spike absorption
D101~103	Switching	Spike absorption
D105~108	Switching	Spike absorption
D109,110	Switching	Band information

SEMICONDUCTOR DATA

) Port : MB89363B (Digital unit IC1, 3)

Block diagram



SEMICONDUCTOR DATA

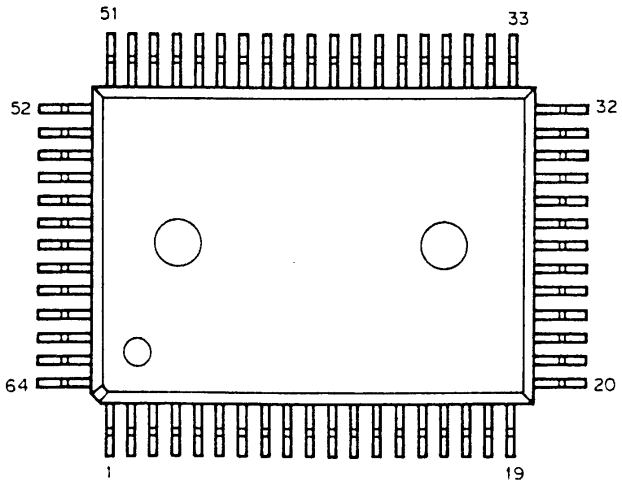
- **Terminal function**

Pin No.	Pin name	Name	I/O	Function
1~4 77~80	P30~P37	Port 3 all bits	I/O	Eight-bit general-purpose input/output port. These terminals are included in group 2. Three operation modes can be selected by setting the control parameter by software.
5	$\overline{W}$	Write	I	The control parameter and port output data item can be written using a low-level signal. The parameter and port data can be distinguished and selected using the $\overline{CS1}$, $\overline{CS2}$, RSLCT0, and RSLCT1 signals.
6	RST	Initial setting reset	I	Input terminal. The MB89363B is set to the initial mode using a reset signal, and initial value 9B (hexadecimal) is automatically set for two control parameters. The initial mode indicates that all ports are in the input state of mode 0. All port terminals stay high in the initial mode. The active signal level is selected using an RH/$\overline{RL}$ signal. RH/$\overline{RL}$ = 0 : $\overline{RST}$ (active low) RH/$\overline{RL}$ = 1 : RST (active high)
9	RH/$\overline{RL}$	Reset active level selection	I	The RST terminal is set to active high or active low. RH/$\overline{RL}$ = 0 : $\overline{RST}$ (active low) RH/$\overline{RL}$ = 1 : RST (active high) The RH/$\overline{RL}$ terminal is fixed at either Vcc ot GND at all times.
11	OUS/$\overline{INS}$	Port 0 and 3 read value selection	I	This terminal indicates the output state of ports 0 and 3. It also selects whether the external terminal value of ports 0 and 3 is read directly or whether the output latch value of ports 0 and 3 is read directly when reading the value of ports 0 and 3. OUS/$\overline{INS}$ = 0 : The output latch value of ports 0 and 3 is read. OUS/$\overline{INS}$ = 1 : The external terminal value of ports 0 and 3 is read.
12~19	DB0~DB7	Bidirectional data bus	I/O	Eight-bit, bidirectional data bus. These terminals are used for data communication with the MPU. The bus signal making and breaking and data direction are controlled using the $\overline{CS1}$, $\overline{CS2}$, $\overline{R}$ and $\overline{W}$ signals.
20~23 25~28	P00~P07	Port 0 all bits	I/O	Eight-bit, general-purpose input/output port. These terminals are included in group 0. Three operation modes can be selected by setting the control parameter by software.
29 75	$\overline{CS1}$ $\overline{CS2}$	Device selection	I	When a low-level signal is input to this terminal, signals DB0 through DB7 are released and data communication with the MPU takes place. At that time, the control parameter is written, and data is written into or read from each port. $\overline{CS1}$ = 0 : I/O1 $\overline{CS2}$ = 0 : I/O2 Simultaneous selection of $\overline{CS1}$ = 0 and $\overline{CS2}$ = 0 is inhibited.
30, 74	GND	Ground terminal	I	0V.
31 32	RSLCT0 RSLCT1	Access selection	I	When data is sent to the MPU, the parameter and port are distinguished and selected using the $\overline{CS1}$, $\overline{CS2}$, RSLCT0, and RSLCT1 signals.
34~40 43	P20~P27	Port 2 all bits	I/O	These terminals are used as a general-purpose input/output port, handshaking control terminals, and status data bit input/output terminals in accordance with the operation functions and modes of groups 0 and 1.
44~51	P10~P17	Port 1 all bits	I/O	Eight-bit, general-purpose input/output port. These terminals are included in group 1. Two operation modes can be selected by setting the control parameter by software.
53	Vcc			+5V power.
54~61	P40~P47	Port 4 all bits	I/O	Eight-bit, general-purpose input/output port. These terminals are included in group 3. Two operation modes can be selected by setting the control parameter by software.
62 65~71	P50~P57	Port 5 all bits	I/O	These terminals are used as a general-purpose input/output port, handshaking control terminals, and status data bit input/output terminals.
76	$\overline{R}$	Read	I	Data from each port is read using a low-level signal. The port type is selected using the $\overline{CS1}$, $\overline{CS2}$, RSLCT0, and RSLCT1 signals.
7,8,10,24 33,41,42 52,63,64 72,73	NC	-	-	Connection to the NC terminal is inhibited.

SEMICONDUCTOR DATA

I/O Port : CXD1095Q (Digital unit IC2)

- **Terminal connection**



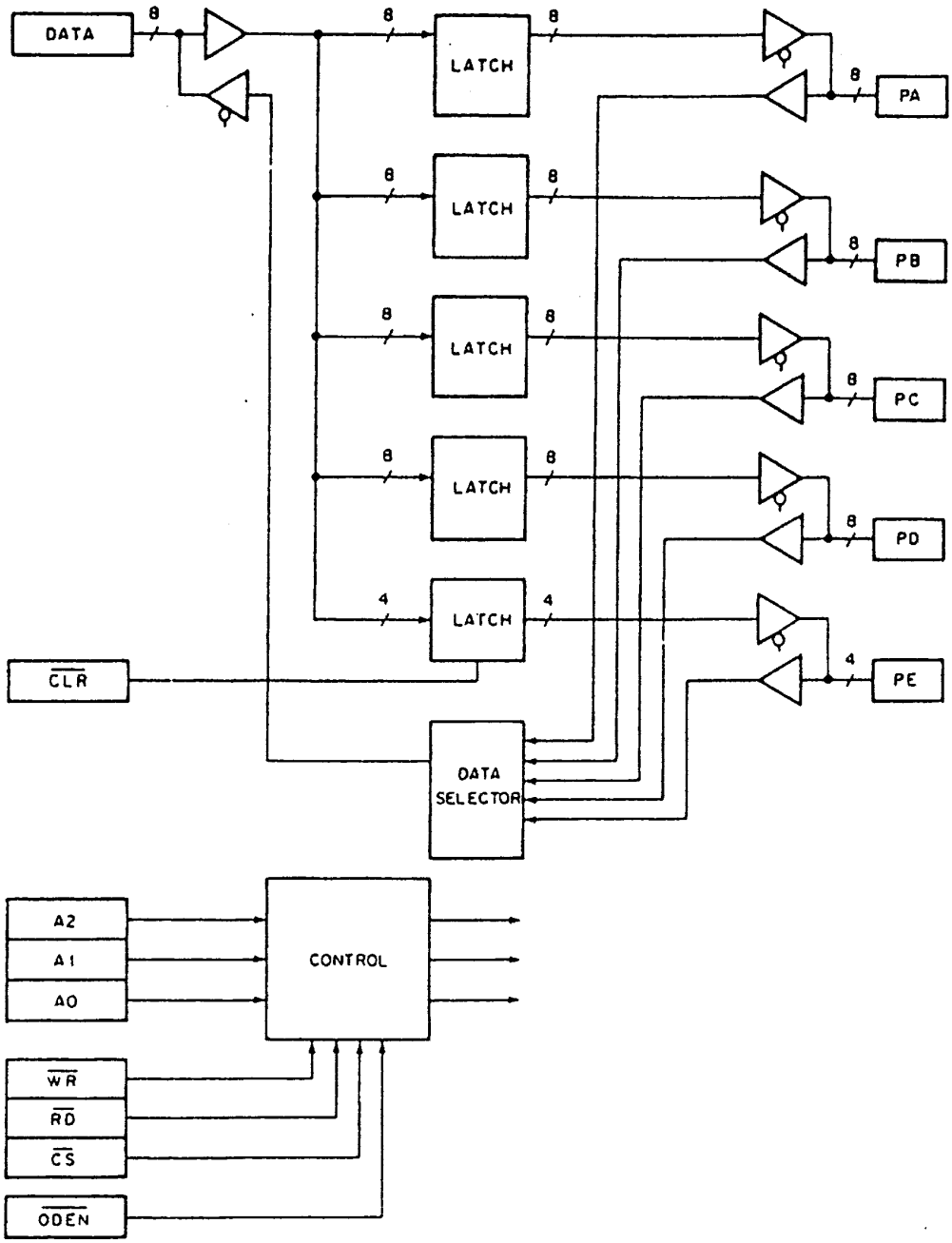
- **Terminal function**

Pin No.	Pin name	I/O	Function
1, 2	NC	–	Not connected.
3~9	PB1~PB7	I/O	Port B input/output terminals.
10	Vss	–	Connected to ground.
11~18	PC0~PC7	I/O	Port C input/output terminals.
19	NC	–	Not connected.
20~24	PD0~PD4	I/O	Port D input/output terminals.
25	Vss	–	Connected to ground.
26	VDD	–	Connected to +5V.
27~29	PD5~PD7	I/O	Port D input/output terminals.
30~32	D0~D2	I/O	Eight bit, tristate, bidirectional data bus. Data can be sent by connecting these terminals to the data bus of a microcomputer system. Goes active when $\overline{CS}$ = 0 and $\overline{RD}$ = 0 or $\overline{WR}$ = 0.
33, 34	NC	–	Not connected.
35~39	D3~D7	I/O	Eight bit, tristate, bidirectional data bus. Data can be sent by connecting these terminals to the data bus of a microcomputer system. Goes active when $\overline{CS}$ = 0 and $\overline{RD}$ = 0 or $\overline{WR}$ = 0.
40	$\overline{CLR}$	I	The register output of port E (4-bit port) is cleared (becomes zero) when $\overline{CLR}$ = 0.
41	$\overline{ODEN}$	I	All ports enter the input state (high-impedance state) when $\overline{ODEN}$ = 0. No output data register or control register is set.
42	Vss	–	Connected to ground.
43	$\overline{WR}$	I	Data is written into CXD1095Q when $\overline{WR}$ = 0. Data bus information is written on the leading edge of the $\overline{WR}$ signal (0 to 1).
44	$\overline{RD}$	I	Data is read from CXD1095Q when $\overline{RD}$ = 0.
45	$\overline{CS}$	I	CXD1095Q is selected when $\overline{CS}$ = 0 and enters the non-selection mode when $\overline{CS}$ = 1. Data lines D7 through D0 enter the high-impedance state.
46~48	A0~A2	I	Five ports and control registers are selected by addressing.
49, 50	PE0, PE1	I/O	Port E input/output terminals.
51	NC	–	Not connected.
52, 53	PE2, PE3	I/O	Port E input/output terminals.
54~56	PA0~PA2	I/O	Port A input/output terminals.
57	Vss	–	Connected to ground.
58	VDD	–	Connected to +5V.
59~63	PA3~PA7	I/O	Port A input/output terminals.
64	PB0	I/O	Port B input/output terminals.

Note : The $\overline{CS}$, $\overline{RD}$, $\overline{WR}$, $\overline{ODEN}$, and $\overline{CLR}$ signals are pulled up to Vcc in the IC.

SEMICONDUCTOR DATA

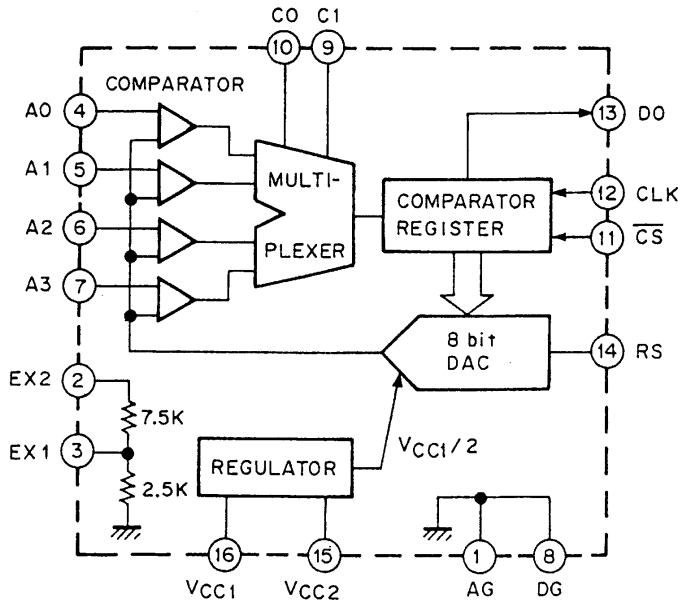
Block diagram



SEMICONDUCTOR DATA

A/D Converter : MB4052 (Digital unit IC5)

- **Block diagram**



- **Terminal function**

Pin No.	Pin Name	Symbol	Function
2	Range expander input	EX2	Analog input pin for expanding the range.
3	Range expander output	EX1	Analog output pin for expanding the range. Connect to any pin from A0 to A3. By using EX1 and EX2, the range is expanded to the x4 range.
4~7	Analog entrance	A0~A3	4-ch analog input pin. Channel 1 is selected by channel select input C0 and C1.
9	Channel select input	C0	The input to designate the analog input channel for A/D converter.
10		C1	This signal is latched at the trailing edge of $\overline{CS}$.
11	Chip select input	$\overline{CS}$	This is the chip select input pin. When $\overline{CS}$ is inverted from "1" to "0", A/D converting starts and data output is enabled. After A/D converting is over or when an interrupt is required, set the $\overline{CS}$ back to "1".
12	A/D conversion clock	ADC CLK	This is the clock input pin for A/D conversion input to the comparator register sequentially. Conversion speed is determined by the clock speed. In the case of 8-bit, approx. 10 clocks will be needed. However, it is not necessary that the clock period by fixed.
13	Data output	DATA OUT	This is the open collector to output the result of A/D conversion. The data is output in the order of the start bit, most significant bit, 2nd significant bit, ... least significant bit, and the stop bit, synchronized with ADC CLK.
14	Range select input	RS	This is the input pin for selecting the voltage range of analog input. The VFS = $V_{CC1}/8$ range is selected at "0", and the range of FVS = $V_{CC1}/2$ is selected at "1". During conversion, hold this pin to "0" or "1".
1	Analog ground	AG	Ground terminal.
8	Digital ground	DG	
15	Power supply pin 2	V_{CC2}	When driving with 3.5 to 6.0V of power, connect V_{CC1} and V_{CC2} to each other, and apply the power voltage to them. When driving 8 to 18V of power, apply the power voltage to V_{CC2}. At this time, the 5V stabilized voltage is output to V_{CC1}, and approx. 10mA current can be supplied externally to the IC. When either 3.5 to 6.0V or 8 to 18V power is used, V_{CC1} is the reference voltage for A/D conversion.
16	Power supply pin 1	V_{CC1}	

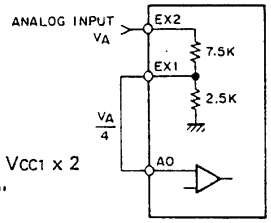
- **Channel select**

C1	C0	Selected CH
0	0	A0
0	1	A1
1	0	A2
1	1	A3

- **Range select**

RS	Conversion voltage range
0	0 ~ $V_{CC1}/8$
1	0 ~ $V_{CC1}/2$

- **Wiring example when expanding the range**



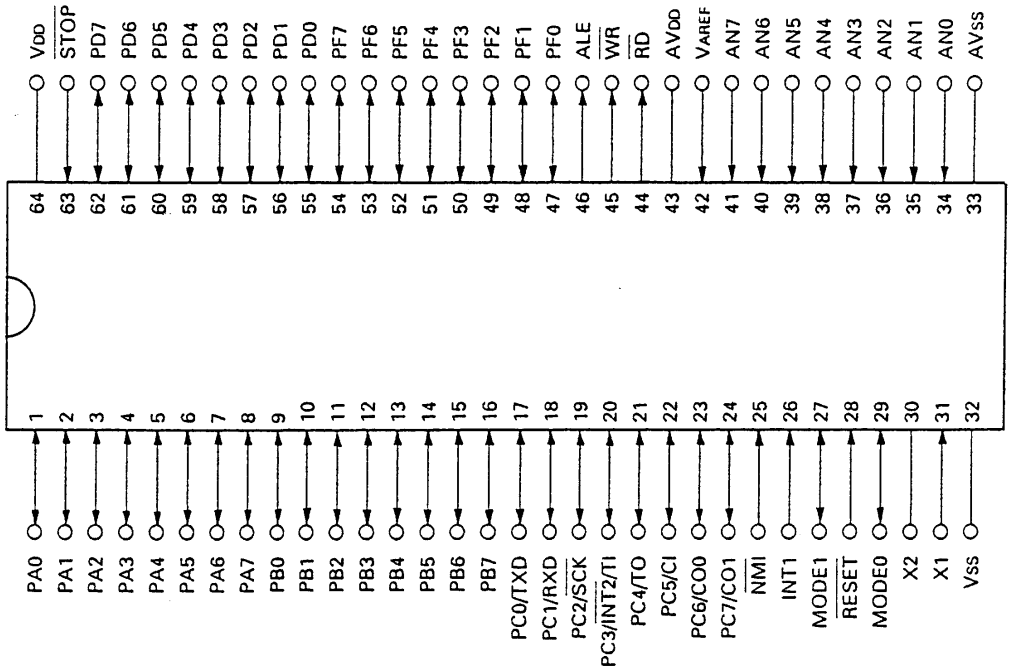
V_A : 0 ~ V_{CC1} x 2
RS : "1"

TS-850S

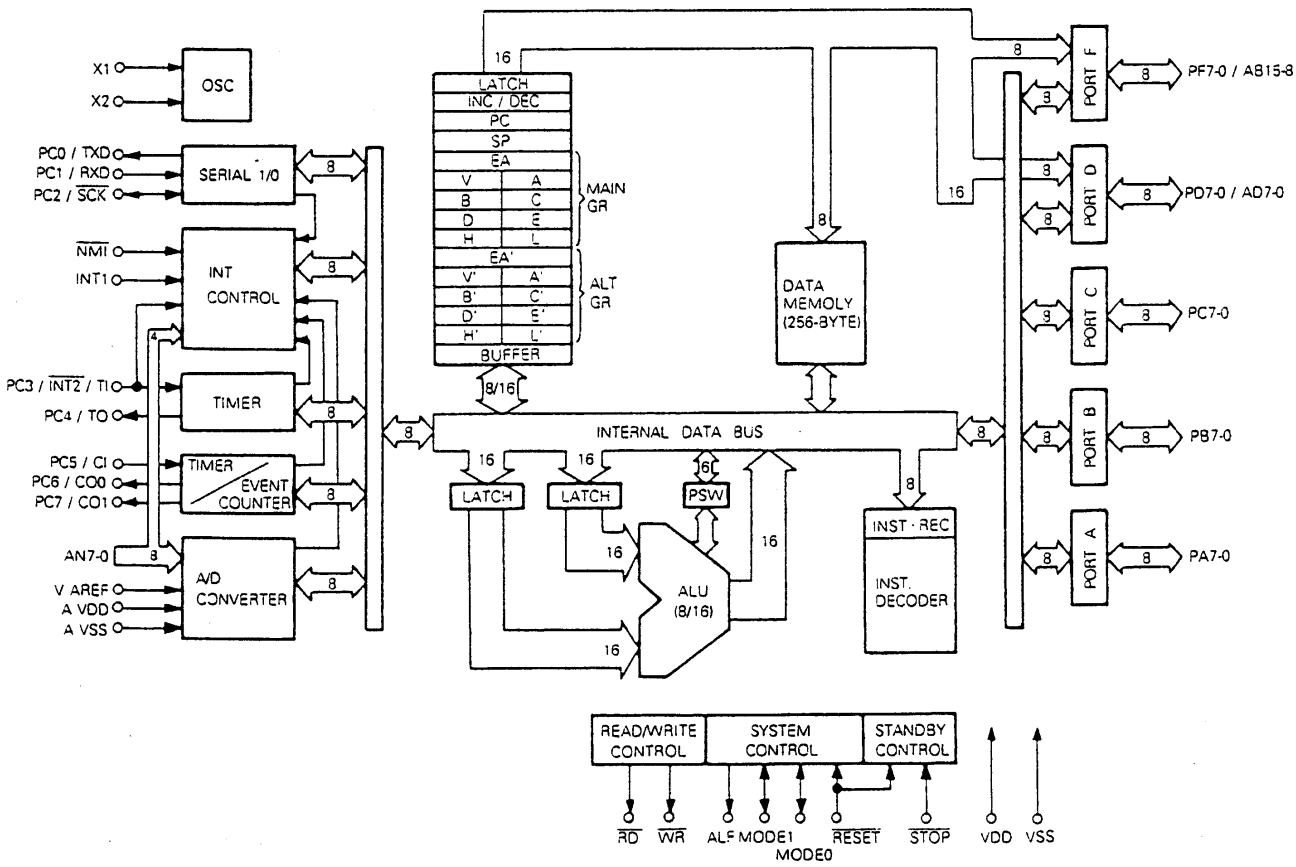
SEMICONDUCTOR DATA

CPU : μPD78C10G-36 (Digital unit IC6)

- **Terminal connection**



- **Block diagram**



SEMICONDUCTOR DATA

• Terminal function

Pin No.	Pin Name	I/O	Functions
1~8	PA7~PA0 (Port A)	I/O	8-bit input/output ports that allows designation of input and output in bit units.
9~16	PB7~PB0 (Port B)	I/O	8-bit input/output ports that allows designation of input and output in bit units.
17	PC0 (Port C)	I/O	8-bit input/output ports that allows designation of input and output in bit units.
	TXD (Transmit data)	O	The output terminal for serial data.
18	PC1 (Port C)	I/O	8-bit input/output ports that allows designation of input and output in bit units.
	RXD (Receive data)	I	The input terminal for serial data.
19	PC2 (Port C)	I/O	8-bit input/output ports that allows designation of input and output in bit units.
	$\overline{SCK}$ (Serial clock)	I/O	The input/output terminal of the serial clock. The terminal functions as an output terminal when using the internal clock and as an input terminal when using an external clock.
20	PC3 (Port C)	I/O	8-bit input/output ports that allows designation of input and output in bit units.
	$\overline{INT2}$ (Interrupt request)	I	The maskable interruption input terminal for the edge trigger (falling edge).
	TI (Timer input)	I	This can also be used as a zero detection terminal of an AC input.
21	PC4 (Port C)	I/O	8-bit input/output ports that allows designation of input and output in bit units.
	TO (Timer output)	O	The square wave is output for the amount of the time counted on the timer taking a half cycle for 1 cycle of the internal clock.
22	PC5 (Port C)	I/O	8-bit input/output ports that allows designation of input and output in bit units.
	CI (Counter input)	I	The input terminal of external pulse for the timer/event counter.
23,24	PC6, PC7 (Port C)	I/O	8-bit input/output ports that allows designation of input and output in bit units.
	CO0,CO1 (Counter output 0, 1)	O	The output of the programmable rectangular wave in accordance with the timer/event count.
25	$\overline{NMI}$ (Non-maskable interrupt)	I	The non-maskable interruption input terminal for the edge trigger (falling edge).
26	INT1 (Interrupt request)	I	The maskable interruption input terminal for the edge trigger (rising edge). This can also be used as a zero cross detection terminal of an AC input.
27,29	MODE0, MODE1 (Mode)	I/O	The μPD78C10G is installed externally in accordance with the specifications of the MODE0, MODE1 terminal. Memory size of 4kB, 16KB or 64KB can be selected. MODE0 | MODE1 | External memory 0 | 0 | 4KB 1 | 0 | 16kB 1 | 1 | 64KB In addition, when the MODE0, MODE1 terminal is set to "1" (*1), a control signal is output in synchronization with ALE.
28	$\overline{RESET}$ (Reset)	I	The system reset input of low level active.
30,31	X1, X2 (Crystal)		The crystal connection terminal for oscillation of the system clock. This is input to X1 when a clock is supplied from outside.
32	Vss		GND terminal.
33	AVss (Analog Vss)		GND terminal of A/D converter.
34~41	AN0~AN7 (Analog input)	I	The 8-bit analog input to the A/D converter. The AN7 to AN4 can be used as an edge detection (falling edge) input.
42	VAREF (Reference voltage)	I	This serves as both the reference voltage input terminal of the A/D converter as well as control terminal of operation for the A/D converter.
43	AVDD (Analog VDD)		The power terminal of the A/D converter.
44	$\overline{RD}$ (Read strobe)	O	The output strobe signal for the reading operation of external memory. This is at the high level except for the read machine cycle of external memory. When the $\overline{RESET}$ signal is at the low level and during the hardware STOP mode, the output becomes a high impedance output.
45	$\overline{WR}$ (Write strobe)	O	The output strobe signal for the writing operation of external memory. This is at the high level except for the write machine cycle of external memory. When the $\overline{RESET}$ signal is at the low level and during the hardware STOP mode, the output becomes a high impedance output.
46	ALE (Address latch enable)	O	The PD7~PD0 pin output strobe signal for latch outside that output lower address data for the access external memory. When the $\overline{RESET}$ signal is at the low level and during the hardware STOP mode, the output becomes a high impedance output.
47~54	PF7~PF0 (Port F)	I/O	8-bit input/output ports that allows designation of input and output in bit units.
	AB15~AB8 (Address bus)	O	This serves as address data bus when using external memory.
55~62	PD7~PD0 (Port D)	I/O	
	AD7~AD0 (Address/data bus)	I/O	This serves as multiplexed address/data bus when using external memory.
63	$\overline{STOP}$ (Stop)	I	The control signal input terminal of the hardware STOP mode. When a low level signal is input, oscillation of the oscillator is discontinued.
64	VDD		Positive power supply terminal.

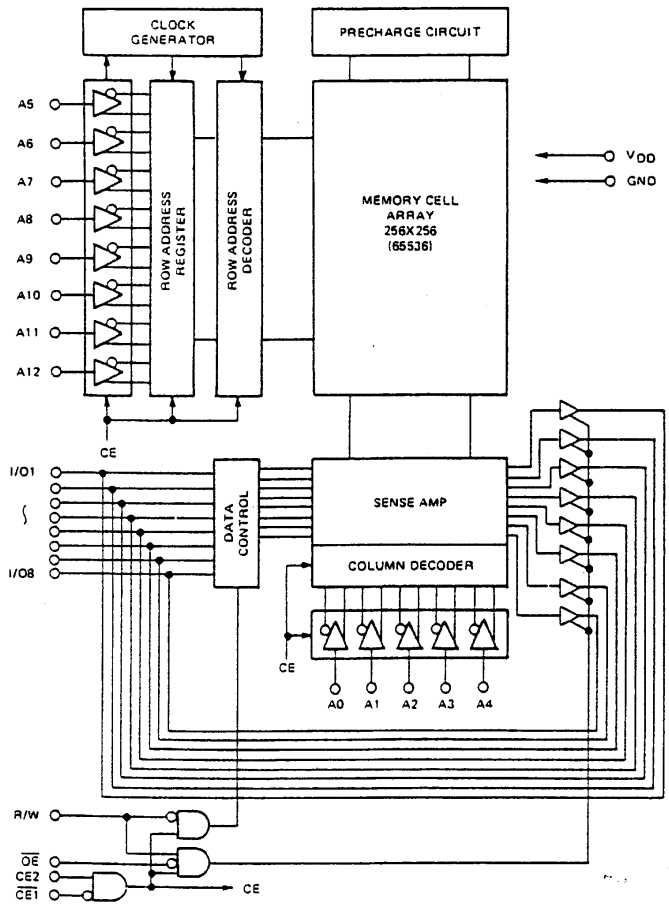
*1 : The pull-up resistance R is $4 \leq R \leq 0.4tcyc$ (KΩ). tcyc is in ns units

TS-850S

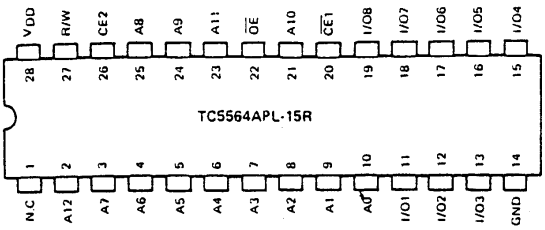
SEMICONDUCTOR DATA

RAM : TC5564APL-15 (Digital unit IC13)

• **Block diagram**



• **Terminal connection**



• **Operation mode**

Operation mode	$\overline{CE1}$	CE2	$\overline{OE}$	R/W	I/O1 ~ I/O8	Power
Read	L	H	L	H	D OUT	IDDO
Write	L	H	*	L	D IN	IDDO
Output disable	*	*	H	*	High-Z	IDDO
Standby	H	*	*	*	High-Z	IDDS
	*	L	*	*	High-Z	IDDS

• **Description of terminals**

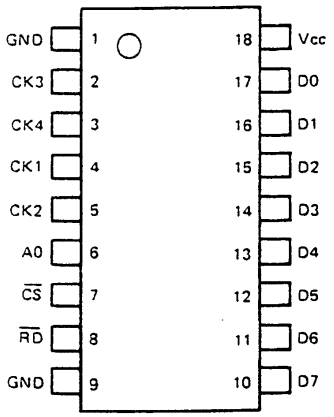
Name	Description
A0 ~ A12	Address input
R/W	Read/write control input
$\overline{OE}$	Output enable input
$\overline{CE1}$, CE2	Chip enable input
I/O1 ~ I/O8	Data input/output
VDD	Power supply terminal (+5V)
GND	Ground
NC	Not used

• **Access time (MAX)**

Item	Time
Access time	150ns
CE1 access time	150ns
CE2 access time	150ns
OE access time	70ns

Encoder Gate Array : LZ92K37 (Digital unit IC14)

• **Terminal connection**



• **Terminal function**

Pin No.	I/O	Signal name	Pin No.	I/O	Signal name
1	–	GND	10	TO	D7
2	Icu	CK3	11	TO	D6
3	Icu	CK4	12	TO	D5
4	Icu	CK1	13	TO	D4
5	Icu	CK2	14	TO	D3
6	Ic	A0	15	TO	D2
7	Ic	CS	16	TO	D1
8	Ic	RD	17	TO	D0
9	–	GND	18	–	Vcc

Ic : C-MOS level input buffer
Icu : Input buffer with C-MOS level pull-up resistance
TO : Tristate output buffer

• **Terminal function**

Terminal name	Terminal function
CK1, 2	Rotary encoder pulse input
CK3, 4	Rotary encoder pulse input
A0	Output data selection input, 0 = CK1, 2 1 = CK3, 4
$\overline{CS}$	Chip select input
$\overline{RD}$	Read enable input
D0 ~ D7	Data bus output

i2