



Preliminary W9330F

CODE DIVISION SPREAD SPECTRUM TELEPHONE CHIP

GENERAL DESCRIPTION

The Winbond W9330F is an integrated 900 MHz cordless telephone controller. It employs Code Division Spread Spectrum (CD/SS) technology optimized for low cost, consumer applications while providing the clarity, distance and security of digital spread spectrum communication.

Targeted as a single chip baseband solution, the W9330F incorporates all digital signal processing (DSP) and system control functions for the RF module, voice codec and key pad interface, thus freeing the MPU for other user oriented tasks. Using 1-bit analog to digital conversion (ADC) technique, signal processings are performed in an extended time domain transformation to allow for the use of low cost radio modules. Linear RF coding schemes such as FSK, BPSK and MSK are supported.

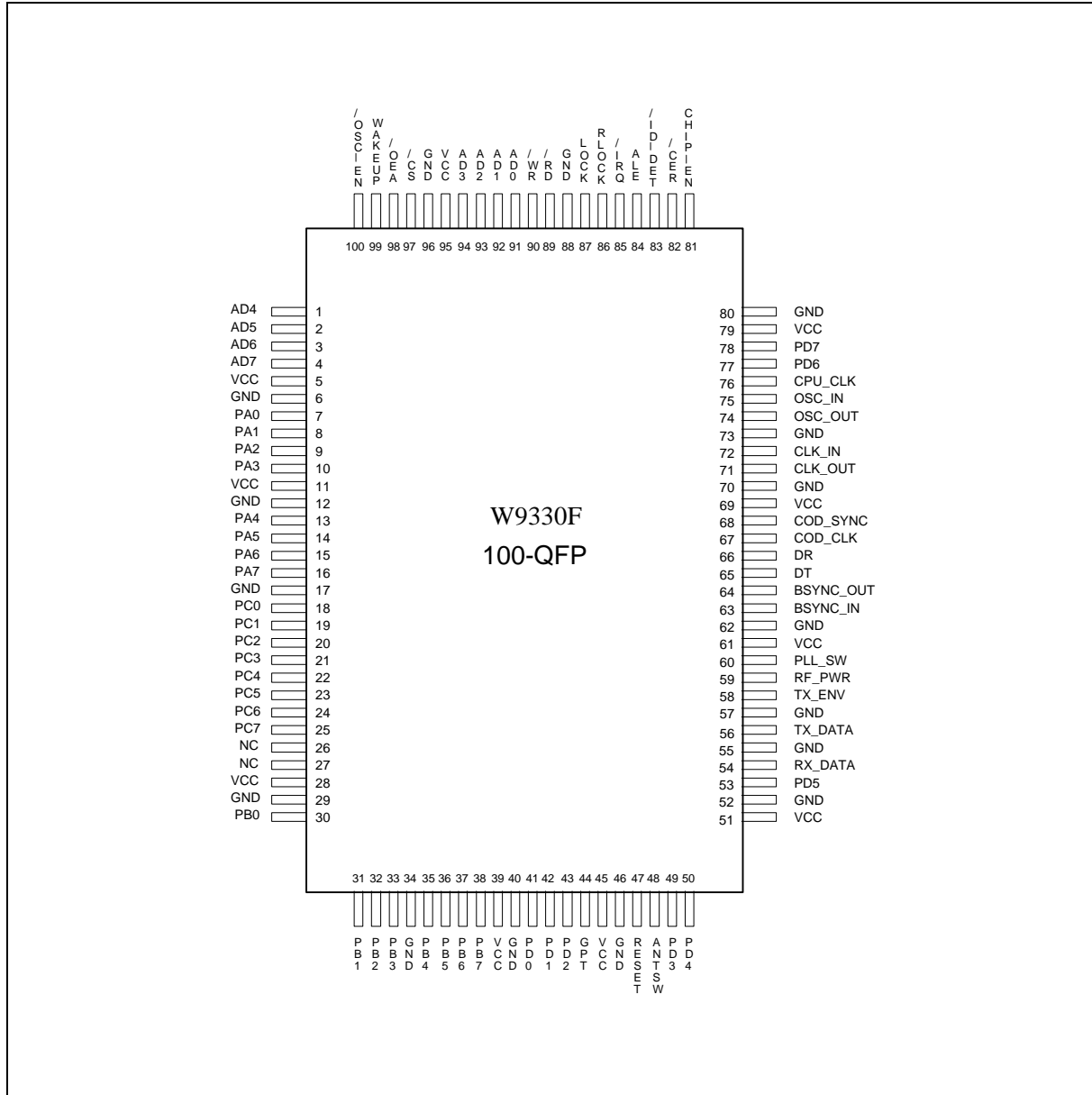
Advance built in features include acoustic echo minimization, data encryption, and diversity antenna control. A proprietary noise reduction scheme can be implemented to correct for low speed multipath fading found in consumer cordless and wireless local loop applications.

The W9330F is implemented in a low power 3V CMOS process technology. It is contained in a 100-pin PQFP package. A complete reference design is available for telephone manufacturers for quick turn development.

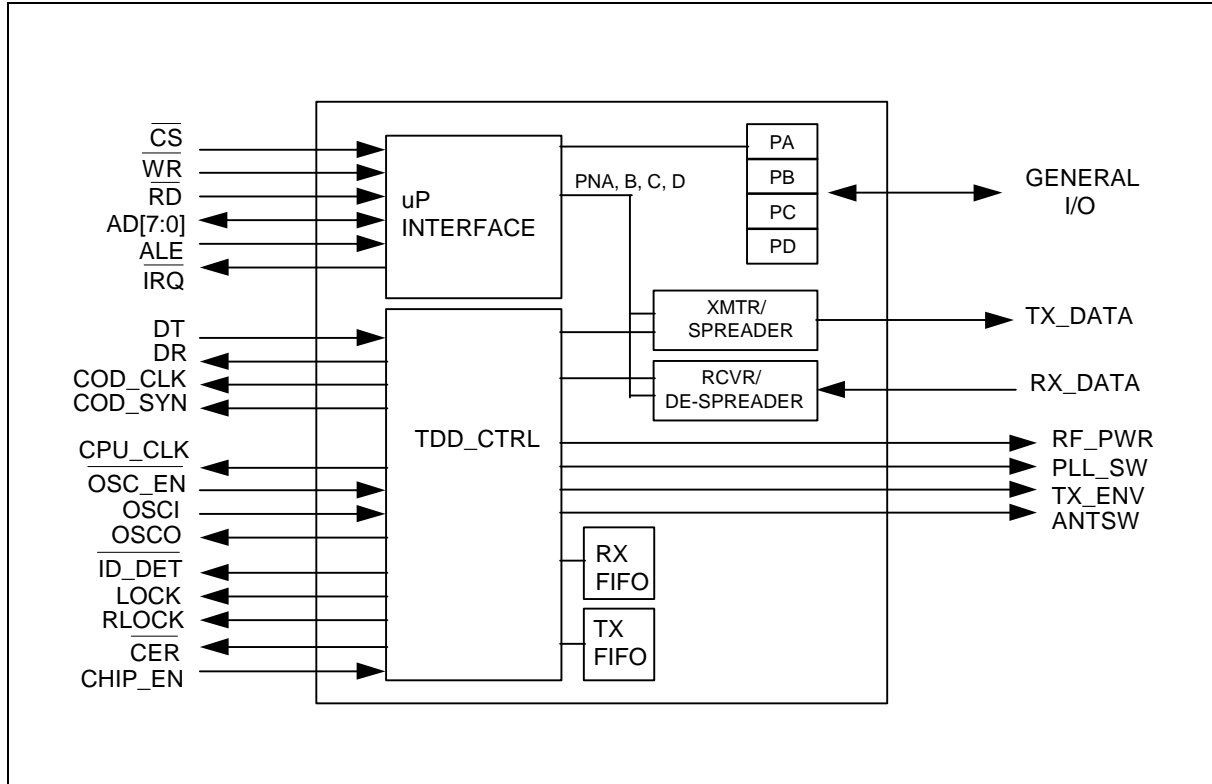
FEATURES

- Low Cost Single Chip Baseband Cordless Telephone Solution
- Advanced CD/SS digital signal processing architecture
- FCC part-15 compliant for unlicensed 900 MHz and 2.4 GHz band operation
- Optimized for low cost MPU and telephone components
- Low Acoustic Echo
- Support Multiple Handset Designs
- Separate Command and Data Fields
- 22-bit User Selectable ID with Automatic Hardware Authentication
- Audio Noise Reduction with Automatic Digital Noise Control
- On-chip PLL, RF module and Codec Interface
- Variable Rate CPU Clock Generation
- Integrated Power Management
- Hardware Supported Dual Antenna Design
- Multi Clock Synchronization for Wireless Local Loop Applications
- Built-in Data Encryption
- 3.0V Single Power Supply with 5.0V Tolerant I/O
- Packaged in 100-pin PQFP/TQFP

PIN CONFIGURATION



BLOCK DIAGRAM



PIN DESCRIPTIONS

The following table describes the external pins of the W9330F. The following conventions and abbreviations are used in the signal descriptions:

Signal Name: All active low signals are indicated by overscore; otherwise the signal is active high.

Signal Type:

IN = 3V TTL input

IN_D = 3V TTL input with built-in pull down resistor

IN_U = 3V TTL input with built-in pull up resistor

OUT = 3V TTL output

OD = Open-drain 3V TTL output

IO = Bi-directional 3V TTL signal

Table 1: Micro-controller Access Signals

| PARAMETER | PIN | TYPE | DESCRIPTIONS |
|-------------------------|----------------------------|------|--|
| AD[7:0] | 4, 3, 2, 1, 94, 93, 92, 91 | IO | Address and data bus. This is the multiplexed address and data bus used for micro-controller interface |
| ALE | 84 | IN | Address Latch Enable. Access address is latched at the falling edge of the ALE. The address specifies the on-chip register being accessed by the micro-controller. |
| $\overline{\text{CS}}$ | 97 | IN | Chip Select. This signal is asserted during a micro-controller access cycle. |
| $\overline{\text{IRQ}}$ | 85 | OUT | Interrupt Request. It is asserted by the W9330F to interrupt the system micro-controller at certain operation points. Interrupt is generated at the end of each transmit frame, the end of each receive frame, and when frame error is detected. |
| $\overline{\text{RD}}$ | 89 | IN | Read Control. When $\overline{\text{RD}}$ is asserted, read data is driven on to the AD[7:0] bus by the W9330F. |
| $\overline{\text{WR}}$ | 90 | IN | Write Control. When $\overline{\text{WR}}$ is asserted, write data on the AD[7:0] bus is sampled by the W9330F. |

Table 2: Codec Interface

| PARAMETER | PIN | TYPE | DESCRIPTIONS |
|-----------|-----|------|--|
| COD_CLK | 67 | OUT | Codec transmit and receive clock. It is used by the Codec chip to sample received data and generate transmit data. This signal is generated from the main operating frequency and is 600 KHz. |
| COD_SYNC | 68 | OUT | Codec Synchronization signal. This is a 8 KHz framing clock signal used by the Codec to synchronized transmit and receive data. COD_SYNC is synchronous with COD_CLK and is generated from the main operating frequency. |
| DR | 66 | OUT | Received Data. Voice data to be sampled by the Codec. It is sampled by the Codec chip at the falling edge of COD_CLK at the beginning of each frame. |
| DT | 65 | IN | Transmit data. Voice data generated by the Codec for transmission. It is generated by the Codec at the rising edge of COD_CLK. |

Table 3: RF Module Interface

| PARAMETER | PIN | TYPE | DESCRIPTIONS |
|-----------|-----|------|--|
| ANTSW | 48 | OUT | Antenna Switch. This signal can be used to switch between two available antenna in the system. The ANTSW signal changes state only at the beginning of the gap time between frames. |
| PLL_SW | 60 | OUT | Phase Lock Loop Switch. This signal switches the transceiver phase lock loop between transmit and receive mode. PLL_SW is high during transmission and the preceding gap time. It is low when receiving. |
| RF_PWR | 59 | OUT | RF Power. This signal switches the transmitter on and off during full duplex operation. It is high when transmitting and low when receiving. It is enveloped by TX_ENV to ensure the proper timing sequence when the RF module switches direction. |
| RX_DATA | 54 | IN | Received Data. PN data recovered from the RF module. Input to the de-spreader circuitry. |
| TX_DATA | 56 | OUT | Transmit Data. Output of the spreader circuitry to be transmitted by the RF module. TX_DATA is a high drive output but is not 5V tolerant. All other external pins are 5V tolerant. |
| TX_ENV | 58 | OUT | Transmitter Power. Switches the direction of the RF module. It is high when transmitting and low when receiving. It envelopes RF_PWR by 5.5 chip time in both edges. |

Table 4: System Interface

| PARAMETER | PIN | TYPE | DESCRIPTIONS |
|-----------|-----|------|--|
| BSYNC_IN | 63 | IN_D | Burst Synchronization Input. This signal is designed to use in a PBX setup where multiple master is located together. All the BSYNC_IN signals should be connected together so that all masters start transmission at the same time. |
| BSYNC_OUT | 64 | OUT | Burst Synchronization Output. This signal is designed to use in a PBX setup where multiple master is located together. The BSYNC_OUT of one master should be used as synchronization source and connected to the BSYNC_IN to all masters, including its own BSYNC_IN to synchronize transmission. If only one master issued, the BSYNC_OUT should be connected to the BSYNC_IN of the same device. |
| CHIP_EN | 81 | IN | Chip Enable. This signal controls the internal clocks of the device. When it is de-asserted, the internal clocks remain unchanged (time freeze). The CPU_CLK signal and internal timer are still operational while CHIP_EN is de-asserted. The device is in operation mode only when CHIP_EN is asserted. |

Table 4: System Interface, continued

| PARAMETER | PIN | TYPE | DESCRIPTIONS |
|-----------------------------|---|------|--|
| CLK_IN | 72 | IN | System clock input. It should be set at 19.2 MHz. |
| CLK_OUT | 71 | OUT | System clock output. This signal is generated by the oscillator circuit and should be connected to the CLK_IN input |
| CPU_CLK | 76 | OUT | CPU Clock. This is the clock input to the system micro-controller. After power up, this is the main operating clock divided by 8. It can be programmed to divided by 2 or by 4. |
| $\overline{\text{CER}}$ | 82 | OUT | Check sum Error. This signal is asserted at the end of each receive subframe to indicate that at least one single bit error has been detected. It is cleared with the status register is read. |
| GPT | 44 | OUT | General Purpose Timer. This signal is the output of the programmable general purpose timer. The cycle time of this output is programmable between 125 usec to 8.192 sec with 50% duty cycle. |
| $\overline{\text{ID_DET}}$ | 83 | OUT | ID detection. This signal is set during each receive frame after the ID field has been detected. It is clear at the end of the receive frame if the ID is not found. |
| LOCK | 87 | OUT | Lock. Indicates that the W9330F is in the LOCK state with the remote device. See functional description section for more detail. |
| NC | 26, 27 | | No connect. These pins must be left unconnected in the system. |
| $\overline{\text{OEA}}$ | 98 | IN_U | Output enable for port A output pins. |
| $\overline{\text{OSC_EN}}$ | 100 | IN | Crystal oscillator enable signal. The oscillator circuit is off when this signal is de-asserted. |
| OSC_IN | 75 | IN | Crystal input. |
| OSC_OUT | 74 | OUT | Crystal output |
| PA[7:0] | 16, 15, 14, 13, 10, 9, 8, 7 | OUT | General purpose output port. |
| PB[7:4] | 38, 37, 36, 35, 30, 31, 32, 33 | OD | General purpose output port. |
| PB[3:0] | | OUT | |
| PC[7:4] | 25, 24, 23, 22, 21, 20, 19, 18 | IN_U | General purpose input port. |
| PC[3:0] | | IN_D | |

Table 4: System Interface, continued

| PARAMETER | PIN | TYPE | DESCRIPTIONS |
|-----------|---|------|---|
| PD[7:0] | 78, 77, 53, 50, 49, 43, 42, 41 | IO | General purpose I/O port |
| RESET | 47 | IN | System reset. This is asynchronous reset signal. RESET must be asserted for at least ten clock cycles after initial power up. |
| RLOCK | 86 | OUT | Remote Lock. Indicates that W9330F is in the RLOCK state. see functional description section for more detail |
| WAKEUP | 99 | OUT | Combinational output of port C input pins. WAKEUP = PC0 PC1 PC2 PC3 ~PC4 ~PC5 ~PC6 ~PC7 |

FUNCTIONAL DESCRIPTION

The W9330F is an integrated baseband chip designed for digital cordless telephone applications. It employs direct sequence spread spectrum technology for secure and superior voice data transmission. All the telephone controller functions are provided including: time division duplex control, pseudo noise spreader and de-spreader, direct codec interface and I/O expansion ports.

1. Spreader and De-spreader

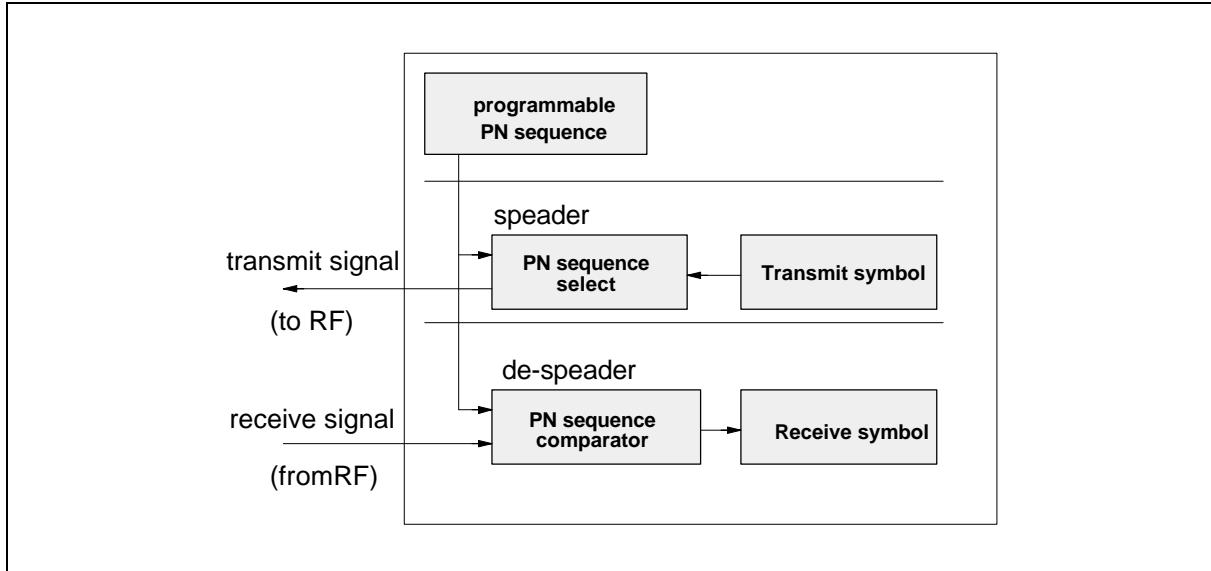
The function of the spreader is the key to any spread spectrum communication system. It encodes (spreads) the voice data into a multiple bit (chip) pseudo-noise (PN) sequence for transmission.

Four sets of PN sequences, 32 chips each, are programmable by the system controller. The four PN sequences and their opposite phase counterparts form eight possible PN combinations. Every three bits of the transmit data is grouped together to form a symbol. Each one of the eight possible symbol is assigned to one of the PN combination. With each PN sequence being 32-chip long and each symbol carries 3 bits of user data, the spread ratio is 10.667.

The de-spreader performs the reversed function of the spreader. The received signal (chip) is sampled by the de-spreader and compared with the eight possible PN sequence being sent. The user data is recovered based on the best-matched PN sequence.

The received signal is sampled by the de-spreader at twice the chip rate. This sampling rate is chosen to ensure that the transmitted signal can be sufficiently reconstructed after all the environmental distortion.

The following diagram shows the principal functions of the spreader and the de-spreader.



2. Time Division Duplex

The W9330F emulates full duplex communication on a half duplex link by using time division duplex (TDD). The two communication units, one designated as master and the other designated as slave, communicate with each other by using the TDD protocol.

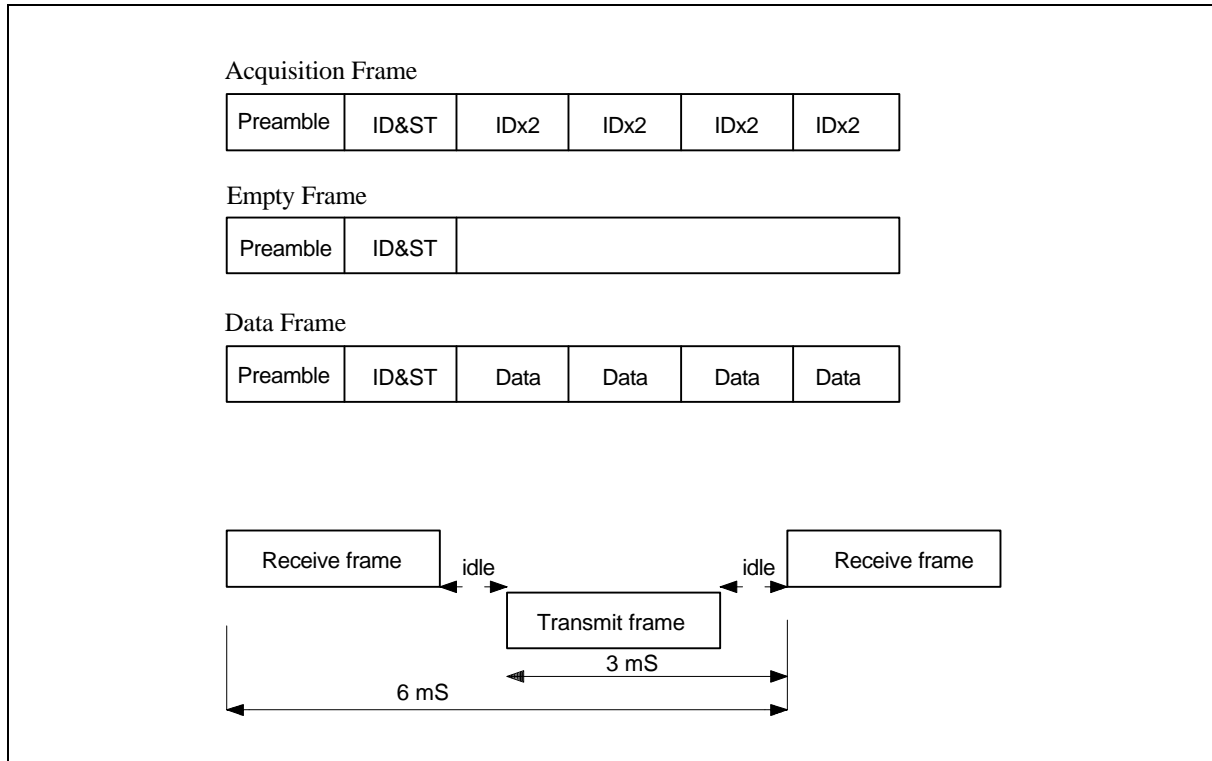
Within each time slot, only one device is transmitting and the other is in either idle or receiving mode. Three types of communication frames are used by the master and slave to establish communication link and transmit data. The frame structures are illustrated in the following diagram.

Each frame consists of 324 bits. It includes a 54-bit preamble and five sub-frames. Each sub-frame contains 48 bits of data and 6 bits of parity. The first subframe contains 24 bits of ID field which uniquely identifies the master-slave pair. Between transmitting and receiving of each frame, idle time equals to the transmission time of 60 bits is added for RF module switching and locking. At the chip rate of 1.365333 MHz and spread of 10.667, the transmission time of one frame including the idle time is exactly 3.000 mS. With 192 bits of user data transmitted per frame, the data bandwidth is 32 Kbps in each direction.

Communication is initiated by the master by sending the acquisition frame. When the slave acquires the acquisition frame and correctly matches the ID field, it responds by sending another acquisition frame to the master.

When the master receives the acquisition frame with the correct ID, it responds by sending the empty frame to the slave. The slave responds by sending another empty frame and the communication link is established.

Once the link is established, the master and the slave take turns in sending data frame. Each data frame contains the ID and status sub-frame to identify the intended receiver and the command/status information in addition to user data.



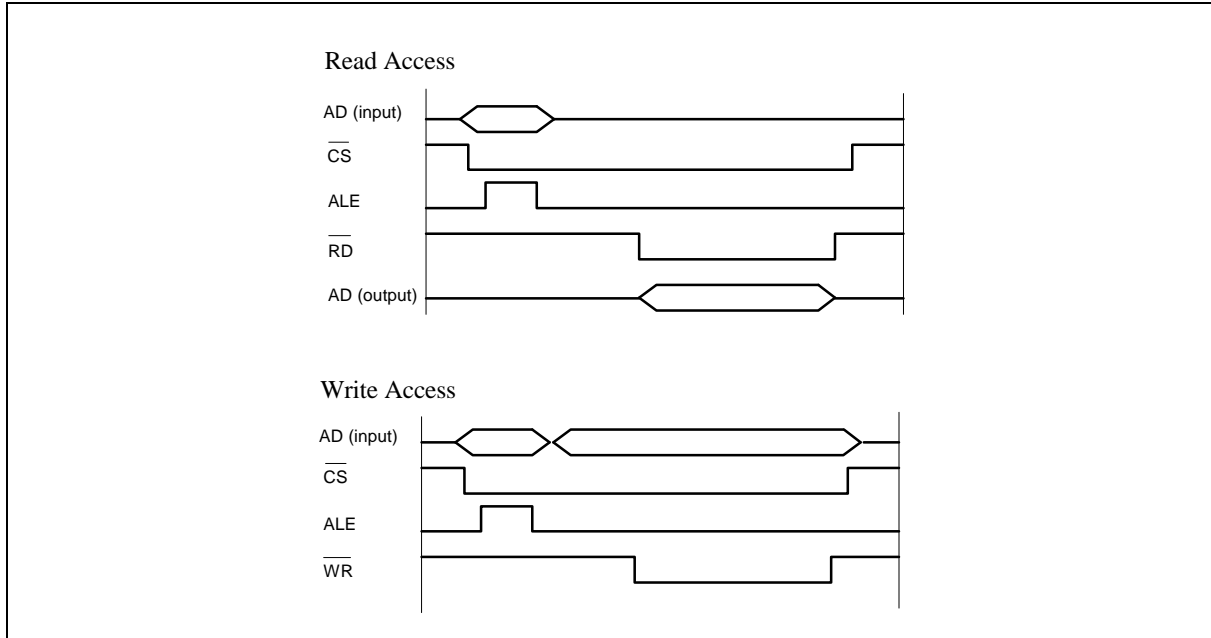
3. System Controller Interface

Interface to the system controller is through the on-chip registers, the interrupt pin and a group of auxiliary status signals.

3.1 Control register access

The control registers of the W9330F can be accessed by the system controller through a simple bus interface. The registers and the I/O expansion ports are uniquely identified by an 8-bit address. The following diagram illustrates the read and write access timing to the on-chip registers. Each access must be enclosed by the assertion of \overline{CS} . As soon as \overline{CS} is asserted, the access address can be specified at the AD bus with ALE asserted. The access address is latched by the falling edge of ALE. Once the address is latched, the access command can be specified by asserting the \overline{RD} or \overline{WR} signals. If \overline{RD} is asserted, the read data is driven by the W9330F on to the AD bus. The system controller must tri-state the AD bus before asserting \overline{RD} to avoid data contention.

If \overline{WR} is asserted, the data on the AD bus is written into the register specified during ALE. The valid data must be driven on the AD bus before \overline{WR} is asserted. \overline{CS} gated write is not supported.



3.2 Interrupt

The W9330F can be programmed to generate system interrupt at the end of each transmit or receive frame or subframe.

If the TE bit in the command register is set, an interrupt is generated at the end of each transmit frame. If the SUBE bit in the command register is also set, interrupt is generated at the end of each transmit subframe in addition the end of frame. The RE bit in the command register has similar function but is applied to receive frame and subframe.

When interrupt, $\overline{\text{IRQ}}$, is asserted, it remains asserted until the status register is read by the controller. When the status register is read, some status bits and $\overline{\text{IRQ}}$ pin are cleared at the same time. If the status register is not read before the next interrupt arrives, the second interrupt may not be detected since $\overline{\text{IRQ}}$ remains asserted starting from the first interrupt.

3.3 Auxiliary status signals

The W9330F provides additional status signals to assist system design.

The LOCK signal is asserted after the device successfully receive an acquisition frame. It remains asserted until the communication link is broken.

The RLOCK signal is asserted after the device successfully receive an empty frame. It remains asserted until the communication link is broken.

$\overline{\text{ID_DET}}$ is asserted when the receiving device detects the correct system ID in the receive frame. It is asserted around the first subframe of the receive frame. Once asserted, it remains asserted until the end of the frame. The W9330F allows up to two symbol errors within the ID field. $\overline{\text{ID_DET}}$ is asserted if two or less symbol error is detected in the ID field.

$\overline{\text{CER}}$ is asserted when the parity error is detected in any subframe. It is cleared when the status register is read by the system controller.

4. Clock Generator

The W9330F operates with the system crystal or oscillator at 19.2 MHz.

The CLK_IN signal is the system clock input pin. All internal timing signals, including the chip rate and sampling rate, are generated from this main clock. The system clock can be supplied by an external source or can be generated through the on-chip oscillator circuit.

The on-chip oscillator circuit consists of four pins, OSC_IN, OSC_OUT, $\overline{\text{OSC_EN}}$ and CLK_OUT. The OSC_IN and OSC_OUT pins are connected to an external crystal. $\overline{\text{OSC_EN}}$ should be asserted (low) to enable the oscillator circuit. CLK_OUT is the buffered output of the oscillator which is capable of driving multiple external devices. If the on-chip oscillator is to be used to generate the system clock input, CLK_OUT and CLK_IN should be connected together externally. If the system clock is provided by external source other than the on-chip oscillator, the oscillator circuit can be turned off by de-asserting $\overline{\text{OSC_EN}}$. The external clock source should drive the CLK_IN input directly. In power down mode the $\overline{\text{OSC_EN}}$ signal can be de-asserted to stop the oscillator and the system clock to conserve power.

The W9330F contains a programmable clock generator to generate a divided-down CPU clock to the system controller. The CPU clock output from the W9330F can be programmed to run at 9.6 MHz, 4.8 MHz, 2.4 MHz (CLK_IN divided by 2, 4 or 8) or off. After system reset, the CPU clock runs at 2.4 MHz (divided by 8).

5. Codec Interface

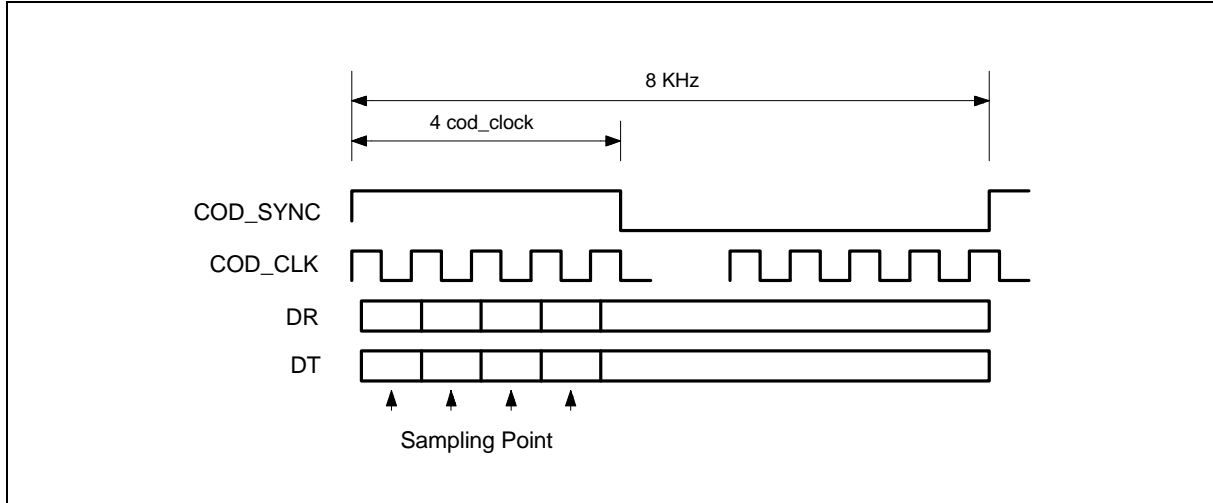
The W9330F supports all ADPCM Codec chips that are compatible with the CCITT G.721 recommendation and ANSI T1.301. Once the communication is established between the master and slave, the W9330F interfaces directly with the codec to retrieve transmit data and send out received data. It generates codec framing signal COD_SYNC and clocking signal COD_CLK.

The COD_SYNC signal is a 8 KHz signal generated from the system clock. The COD_CLK signal is 600 KHz, equivalent to 75X of COD_SYNC.

The rising edge of COD_SYNC defines a data frame for the codec chip. The COD_SYNC signal remains high for four COD_CLK cycles. The codec chip samples four bits of data at the falling edge of COD_CLK while COD_SYNC is high. User data recovered by the de-spreader of the W9330F is stored in on-chip FIFO and then outputted on DR to be sampled by the codec, synchronized with COD_SYNC and COD_CLK signals.

Data to be transmitted by the W9330F is generated by the codec at the first four rising edge of COD_CLK of each data frame. The transmit data, DT, is sampled by the W9330F at the falling edge of COD_CLK and stored in on-chip FIFO. During transmission time, data is read from the FIFO and sent out to the RF module through the spreader.

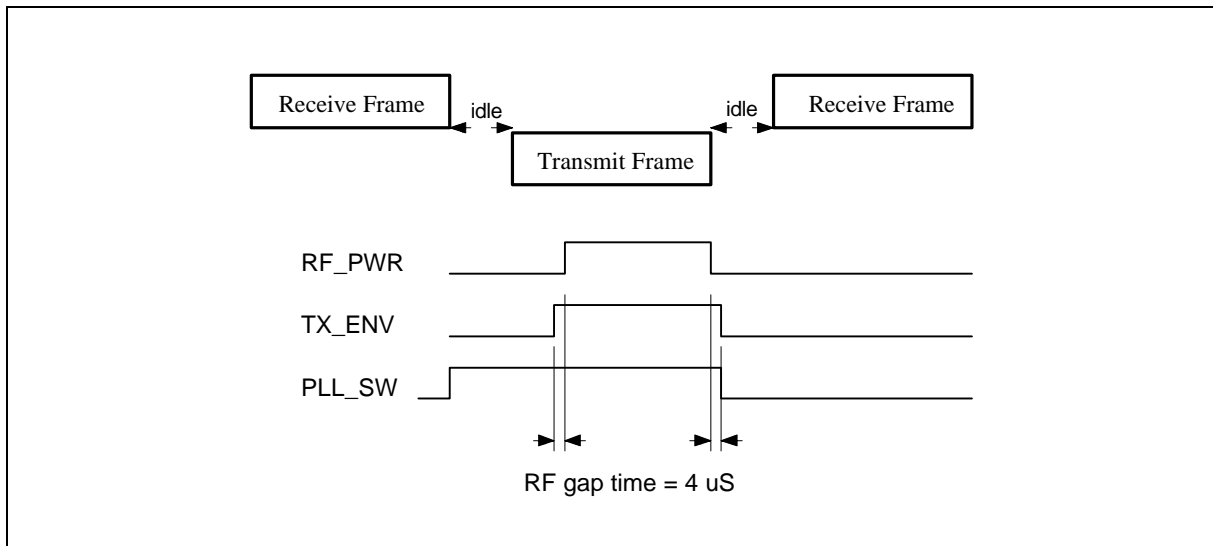
The following timing diagram illustrates the timing of the codec interface.



6. RF Interface

The RF module interface consists of the PLL_SW, RF_PWR, TX_ENV, TX_DATA, RX_DATA and ANTSW signals. The PLL_SW, RF_PWR and TX_ENV signals control the RF module to be in receive and transmit state. The ANTSW signals issued only in dual antenna design to select one of the two available antennas. The value of ANTSW follows the ANTSW bit in the control register. At the end of a transmit frame or receive frame, the value stored in the ANTSW bit is copied to the ANTSW output. During transmit or receive frame, ANTSW output remains unchanged.

The following timing diagram illustrates the RF control signals when switching between transmitting and receiving.



7. Reset

The W9330F can be reset through hardware or software. Hardware reset is when the RESET input is asserted with the system clock running. Software reset is done by writing "one" to the RST bit in the command register. Hardware reset and software reset are very similar except that some control registers return to their default values through hardware reset while some other control registers return to the default value through either reset. The register description section of this data sheet describes the conditions when each register returns to default value. It should be noted that some register values such as IO expansion ports are not affected by either reset. After system power-up, the RESET signal must be asserted for at least ten clock cycles before the system can function properly.

When the RESET signal is de-asserted, the W9330F enters the standby mode. During standby, all the control registers hold its current value and the system controller interface and I/O expansion blocks are fully functional. All control registers, including the command registers, should be programmed by the controller during standby mode. Once programming is completed, the STRT bit in the command register can be set to start operation.

8. Advanced Power Management

The W9330F has three power down modes: sleep, freeze and standby.

Sleep mode has the lowest level of power consumption. The device enters sleep mode when $\overline{\text{OSC_EN}}$ is de-asserted. If the system clock, CLK_IN, is supplied by an external source, it should also stop toggling. Most of the function of the W9330F, including CPU_CLK, general purpose timer, CODEC interface, are stopped in sleep mode. The controller interface and I/O ports are still operational. All control registers and IO ports retain their values and control register can still be accessed through the controller interface. However, read the status register would not clear the $\overline{\text{IRQ}}$ signal. In order to conserve power, controller bus activity and register access should be keep to the minimum.

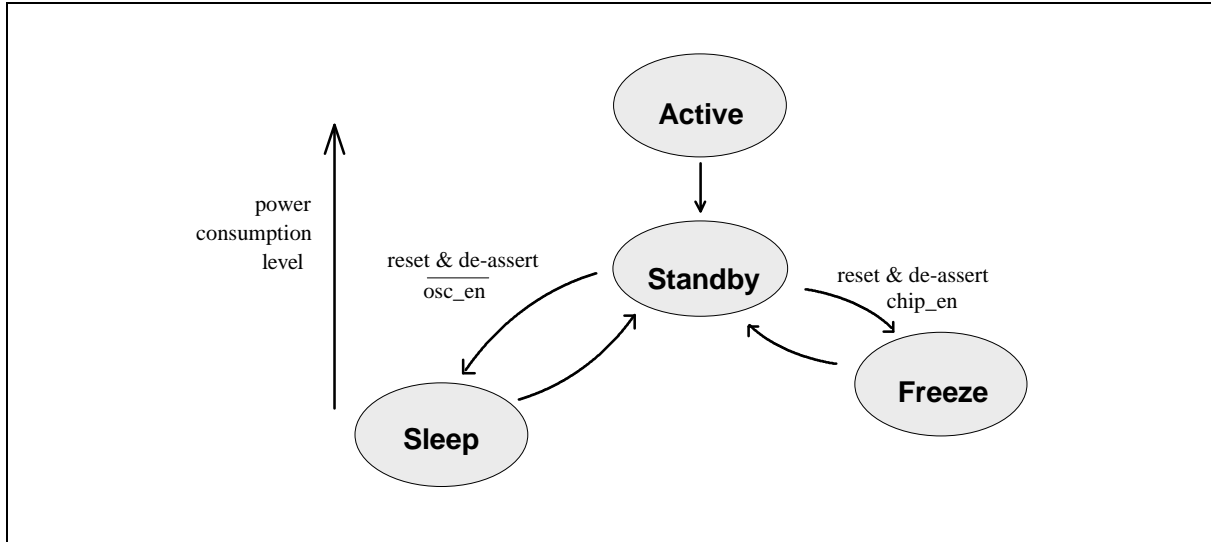
To exit from sleep mode, the device must go through the standby mode. The device must first be reset through hardware reset or software reset. While reset is on, $\overline{\text{OSC_EN}}$ or external clock can be re-asserted. The hardware or software reset can then be removed and the device is now in standby mode.

Freeze mode is the second lowest level of power saving. The device enters freeze mode when the CHIP_EN input is de-asserted. It is similar to sleep mode except that since the system clock is still toggling, the CPU_CLK and general purpose timer functions are still operational. Exit from freeze mode is similar to exit from sleep mode.

Standby mode is entered by executing a hardware or software reset while system clock is running. In standby mode, the device is operational except that communication protocol is not running. When the STRT bit in the command register is set, the device enters active mode and becomes fully operational. The device receives and transmits data only in active mode.

In order to ensure that the device enters sleep or freeze mode with all output pins at the proper setting, the device must be first reset through hardware or software before entering either sleep or freeze modes.

If the on-chip oscillator is not used and the system clock is supplied by an external source, the $\overline{\text{OSC_EN}}$ pin must be de-asserted at all time to avoid any device switching noise and to minimize power consumption.



9. Noise Reduction Control

During voice communication, audible noise can occur in the system through two mechanisms: (1) data underflow/overflow or (2) communication link broken.

Data underflow or overflow is caused by the frequency mis-match between master and slave. The rate of underflow or overflow is proportional to the mis-match. It can be shown that if the operating frequencies between the master and slave differs by 25 ppm, an overflow or underflow occurs every 10 second. In the event of data overflow, the receiver receives data at a rate faster than it sends out to the ADPCM codec. When enough data is accumulated within the W9330F receiving FIFO, it drops 8 bits of ADPCM aligned data each time it occurs. Overflow is not audible because every 8-bit segment of ADPCM data has a play time of only 250 usec and it occurs so infrequently that virtually no information is lost.

Data underflow occurs when the receiver receives data at a rate slower than the 32 Kbps required by the ADPCM codec. When it occurs, the W9330F adds an 8-bit quiet code into the codec bit stream. The quiet code holds the audio output steady for 250 usec until the next data arrives. The occurrence of such event is not audible to human ear due to its short duration. The value of the quiet code is programmable by the user so that different codec devices can be supported.

Communication link is broken when the receiver cannot acquire the receive data frame. This event is signaled to the controller as frame error and the communication link must be re-established. The W9330F is programmable in handling of frame error. If the STKY bit in the command register is cleared, the W9330F will immediately declare lose lock on frame error. The LOCK and RLOCK bits will be dropped and it will try to re-establish the link by sending and receiving acquisition frame. If the STKY bit in the command register is set, the W9330F continues to transmit its data frame on frame error for a few times. If it receive a correct data frame during this time, the communication link remains intact. It declares lose lock only when it cannot receive the correct data frame after several attempts. The number of attempts it continues to transmit on frame error is also programmable by the user through one of the control registers.

During the time when no data is received, the W9330F sends the quiet code to the codec. This eliminates the need for audio signal muting by the controller during frame error.

10. Data Encryption

Data transmission using code division spread spectrum technology is inherently secure due to the use of PN code. The W9330F adds another level of data security by allowing the user to encrypt the transmit data on a frame-by-frame basis. The transmit data can be encoded by a random sequence generated on-chip. Only receivers programmed with the same random sequence can decipher the transmit frame.

The random sequence is generated by the following polynomial $f(X)$: $f(X) = 1 + X^2 + X^3 + X^5 + X^{11}$

Unique random sequence is defined by the user by initializing the value of X^0 to X^7 through one of the control registers.

11. Error Detection

Error detection is built-in to the W9330F. Every 8 bits of the transmit data is accompanied by a parity bit. Parity generation and detection is automatically performed. The CER bit in the status register and $\overline{\text{CER}}$ output pin signals when parity error is detected. They are set within each subframe when parity is detected and are cleared when the status register is read.

12. Signal Strength Indicator

Code division spread spectrum (CD/SS) devices receive data by matching the received signal with the expected PN code. The signal strength indicator indicates how well the received signal correlates with the expected PN code. The indicator is the accumulative value of the correlation factor of each received data starting from the beginning of each frame. If the subframe interrupt bit, SUBE, is turned on and the signal strength indicator is read on each subframe and frame end interrupt, the value is always increasing from the first interrupt until the last interrupt of the receive frame. This value provides a very good indication of how clean the communication link is as seen by the W9330F.

The signal strength indicator is a relative value. Higher value indicates stronger PN code correlation. Value of 5F(Hex) can be expected at frame end when strong signal is received. When frame error is detected on the receive frame, the signal strength indicator does not carry any meaningful value.

13. I/O Expansion Ports

The W9330F contains four I/O expansion ports to facilitate system design. Port A and port B are output ports with PA7: 0 and PB7: 0 as the corresponding output pins. Port A can be tri-stated by de-asserting the $\overline{\text{OE}}$ input pin. Port B is divided into two halves, the lower half, PB3: 0, has regular output buffers and is always enabled. The upper half, PB7: 4, has open drain outputs. Both port A and port B are bit address-able as well as byte address-able.

Port C is an input port with pins PC7:0. It can be read through the control register and also feeds to a combinational output signal. The output signal, WAKEUP, is defined with the following logical function:

$$\text{WAKEUP} = \text{PC0} \mid \text{PC1} \mid \text{PC2} \mid \text{PC3} \mid \sim\text{PC4} \mid \sim\text{PC5} \mid \sim\text{PC6} \mid \sim\text{PC7}$$

Port D is a general purpose I/O port. It functions as an output port when the IO control bit in register 44(Hex) is cleared. If the IO control bit is set, the output buffers on pins PD7: 0 are tri-stated and the input value can be read.

The internal registers holding the value of all ports are static registers and are not affected by software reset or power management functions. All ports can be written or read even when the system clock is turned off. Upon hardware reset, port D becomes an input port and the registers holding the output values are set. Port B is also set by hardware reset.

14. General Purpose Timer

A general purpose timer is included in the W9330F. It can be used by the system designer for various functions such as watch dog timer or tone generator. The output signal GPT is a 50% duty cycle signal and the cycle time is programmable between 125 usec to 8.2 sec. The cycle time is controlled by the register 46(Hex) and 47(Hex) with 47(Hex) being the upper byte and 46(Hex) being the lower byte. Together they form a 16-bit value which becomes the multiplying factor for the cycle time with 125 usec being the basic time unit. When the two registers are programmed with all zero, the GPT output stops toggle.

CONTROL REGISTERS

The control registers of the W9330F can be accessed through the system controller interface. This section describes each control register in detail.

The following table lists all the control registers. The register types are: R/W = Read and write-able, W = write only register, R = read only register.

| REGISTER | TYPE | ADDRESS | HARDWARE RESET VALUE |
|-----------------------------------|------|---------|----------------------|
| Command 1/Status | R/W | 00 | 00000000 |
| Command 2 | W | 01 | 00000000 |
| Quiet Code | W | 03 | 10000000 |
| Transmit ST field | W | 04 - 06 | - |
| Received ST field | R | 08 - 0A | - |
| System ID | W | 0C - 0E | - |
| CPU Clock divider | W | 10 | 00000011 |
| Preamble threshold | W | 12 | 00001000 |
| Signal strength | R | 14 | - |
| Preamble count | W | 15 | 00110111 |
| Scrambler | W | 1E | 00000000 |
| Sticky count | W | 1F | 00000011 |
| PN code, symbol zero | W | 20 - 23 | - |
| PN code, symbol one | W | 24 - 27 | - |
| PN code, symbol two | W | 28 - 2B | - |
| PN code, symbol three | W | 2C - 2F | - |
| I/O expansion port, PA, bit wise | W | 30 - 37 | - |
| I/O expansion port, PB, bit wise | W | 38 - 3F | - |
| I/O expansion port, PA, byte wise | W | 40 | - |
| I/O expansion port, PB, byte wise | W | 41 | 11111111 |
| I/O expansion port, PC | R | 42 | - |
| I/O expansion port, PD | R/W | 43 | 11111111 |
| PD I/O control | W | 44 | 11111111 |
| GPT timer, lower byte | W | 46 | 00000000 |
| GPT timer, upper byte | W | 47 | 00000000 |
| Reserved | | Others | - |

Address 00: Command 1 / Status

Both the Command 1 register and Status register are mapped to register address 00. When this address is written, the input data is written into Command 1 register in the following format.

| | | | | | | | |
|---|---|-----|---|-------|-----|------|------|
| 0 | 0 | REC | 0 | ANTSW | RST | STRT | STKY |
|---|---|-----|---|-------|-----|------|------|

Bit 7, 6 and 4 must be written as zero.

Bit 5: Receive only bit. If this bit is set and the device operates in slave mode, it does not transmit any response frame even when a valid acquisition burst frame is detected.

Bit 3: Antenna switch bit. The output signal ANTSW reflects the value of ANTSW bit. When the value of ANTSW bit changes, the output signal ANTSW will change state only when the PLL_SW output change state.

Bit 2: Soft reset bit. Setting this bit would have similar effect as asserting the RESET external input pin(hardware reset). The RST bit is cleared when the external RESET pin is asserted. Write one to this bit to enter soft reset state and write zero to exit soft reset.

Bit 1: Start bit. The device starts normal operation when this bit is set.

Bit 0: STICKY bit. this bit enables the sticky count register (1FH) when it is set. See description of the sticky count register for more detail.

Reset value: bit 7 to 3 are cleared by hardware reset and not affected by software reset.

bit 2 is cleared by hardware reset.

bit 1 to 0 are cleared by both hardware and software reset.

When register location 00 is read, the status register value outputted with the following format.

| | | | | | | | |
|----|-----|-------|------|-----|-----|-----|-----|
| LK | RLK | ANTSW | SUBF | FER | CER | TND | RND |
|----|-----|-------|------|-----|-----|-----|-----|

This register should read by the system controller at each interrupt. Bit 4 to 0 and the interrupt request pin, \overline{IRQ} , are cleared after each read.

Bit 7: Lock bit. This bit is set whenever an acquisition frame has been received by the device. Once set, this bit remains set unless the communication link is broken.

Bit 6: Rlock bit. This bit is set whenever an empty frame has been received by the device. Once set, this bit remains set unless the communication link is broken.

Bit 5: Has the same value as the ANTSW output pin.

Bit 4: Sub-frame end. This bit is set whenever an interrupt is generated at the end of a subframe. When interrupt is generated at the end of a complete data frame, this bit is cleared. The bit have valid information only when FER bit is cleared.

Bit 3: Frame Error. This bit is set when the device fail to detect the frame preamble or when system ID mis-match. When this bit is set, bit 4, 2, 1 and 0 does not hold valid information.

Bit 2: This bit is set if parity error is detected in any subframe. This bit is cleared every time this register is read.

Bit 1: Transmit End. This bit is set at the end of a transmit frame or subframe.

Bit 0: Received End. This bit is set at the end of a received frame or subframe.

Address 01: Command 2, write only. default: 00000000

| | | | | | | | |
|---|---------|---------|------|----|----|-----|-----|
| 0 | FLIP_TX | FLIP_RX | SUBE | TE | RE | M/S | T/N |
|---|---------|---------|------|----|----|-----|-----|

Bit 7: Reserved. Must be zero when writing to this register.

Bit 6: When this bit is set, the TX_DATA output pin has reversed polarity.

Bit 5: When this bit is set, the RX_DATA input pin is interpreted with reversed polarity.

Bit 4: Subframe enable. If SUBE and either TE or RE is set, an interrupt is generated at the end of each transmit or receive subframe, depending on TE and RE. If SUBE is clear while either TE or RE is set, an interrupt is generated only at the end of each full data frame.

Bit 3: Transmit-end enable bit. Setting this bit would enable an interrupt to be generated at the end of each transmit frame or subframe.

Bit 2: Receive-end enable bit. Setting this bit would enable an interrupt to be generated at the end of each receive frame or subframe.

Bit 1 is the Master/Slave select bit. The device functions as a master if this bit is set. It functions as a slave if this bit is cleared.

Bit 0 is the Test/Normal mode select bit. This bit must be cleared for normal operation.

Bit 7 to 0 are cleared on hardware or software reset.

Address 03: Quiet Code, write only. default: 10000000

| |
|------------|
| Quiet Code |
|------------|

This register controls the output value of the receive data FIFO when data underflow occurs. The value equal to the quiet code of the CODEC should be written into this register. When data underflow occurs, value of this register is outputted to the CODEC.

This register is set to the default value on hardware reset and it is unaffected by software reset.

Address 04 - 06: transmit status, write only, no default value

| |
|------------|
| STO[7:0] |
| STO[15:8] |
| STO[23:16] |

The transmit status field is sent by the W9330F during all transmission frame. Value of the STO field is defined by the system controller and is not interpreted by the W9330F.

The value of these registers are unaffected by hardware and software reset. They are undefined after system power up.

Address 08 - 0A: received status, read only

| |
|------------|
| STI[7:0] |
| STI[15:8] |
| STI[23:16] |

The received status field stores the status value received from each receive frame. These registers are updated at the beginning of each receive frame after the status is received. Value of the STI field is defined by the system controller and is not interpreted by the W9330F.

Address 0C - 0E: system ID, write only, no default value

| | | | | | | | |
|----------|---|-----------|--|--|--|--|--|
| ID[7:0] | | | | | | | |
| ID[15:8] | | | | | | | |
| 1 | 0 | ID[21:16] | | | | | |

These registers contain the system ID. Address 0C contains the least significant bits and 0E contains the most significant bits. The first two bits of register 0E are hard-wired to 10 and they become the two most significant bits of the ID when a frame is transmitted. Both the master and the slave should be programmed to the same ID value.

The value of these registers are unaffected by hardware and software reset. They are undefined after system power up.

Address 10: CPU CLK, write only. default: 00000011

| | | | | | | | |
|---|---|---|---|---|---|-----|-----|
| 0 | 0 | 0 | 0 | 0 | 0 | CU1 | CU0 |
|---|---|---|---|---|---|-----|-----|

Bit 1 to 0 defines the CPU clock divider. If bit[1:0] = 11, CPU_CLK output equivalent to OSC_IN divided by 8. If bit[1:0] = 10, CPU_CLK is divided by 4. If bit[1:0] = 01, CPU_CLK is divided by 2. If bit[1:0] = 00, CPU_CLK output is always low.

This register is set to the default value at hardware reset. It is not affected by software reset.

Address 12: Threshold, write only. default: 00001000

| | | | | |
|---|---|---|---|-----|
| 0 | 0 | 0 | 0 | TH1 |
|---|---|---|---|-----|

The 4 least significant bits of this register define the threshold value of the de-spreader in recognizing preamble symbol. Each acquired symbol has a signal strength value between 0 to 15. A preamble symbol must have signal strength above TH1 in order for it to be recognized.

TH1 is set to "1000" at hardware reset and it is not affected by software reset.

Address 14: Signal Strength, read only.

| |
|-----------------|
| Signal Strength |
|-----------------|

This register is a relative strength indicator of the received signal. FF(Hex) indicates the strongest signal and 0x00 indicates the weakest signal. This register should be read at the end of each receive frame to determine signal strength. This register can be used to assist the system software to adjust signal level or to select antenna in multi-antenna design.

Address 15: Preamble count, write only. default: 00110111

| | |
|------|------|
| CNT1 | CNT2 |
|------|------|

This register contains the preamble symbol count during preamble acquisition. Preamble acquisition is divided into two stages. The first stage is completed when the number of preamble symbol equals to CNT1 is acquired. The second stage is completed when the number of preamble symbol equals to CNT2 is acquired. CNT2 must always be larger than CNT1.

This register is set to the default value during hardware reset and it is not affected by software reset.

Address 1E: Encryption register, write only. default: 00000000

| |
|----------------|
| Encryption key |
|----------------|

This register contains the encryption key used for all transmit and receive data. Both the master and the slave must be programmed to the same value in order to communicate.

This register is set to the default value during hardware reset and it is not affected by software reset.

Address 1F: Sticky count, write only. default: 00000011

| | | | | |
|---|---|---|---|--------------|
| 0 | 0 | 0 | 0 | Sticky count |
|---|---|---|---|--------------|

The 4 least significant bits of this register determine the sticky count. The sticky count is the number of error data frame the device allowed before it would re-establish communication link through the acquisition burst frame protocol. If the STKY bit of the Command 1 register is cleared, the sticky count register is ignored and the communication link must be re-established on every data frame error.

This register is set to the default value during hardware reset and it is not affected by software reset.

Address 20 - 23: PN code, write only, no default value

| |
|-----------------|
| CODEZERO[7:0] |
| CODEZERO[15:8] |
| CODEZERO[23:16] |
| CODEZERO[31:24] |

These registers contain the PN sequence for symbol "000" and "111". PN code registers are not affected by hardware or software reset.

Address 24 - 27: PN code, write only, no default value

| |
|----------------|
| CODEONE[7:0] |
| CODEONE[15:8] |
| CODEONE[23:16] |
| CODEONE[31:24] |

These registers contain the PN sequence for symbol "001" and "110". PN code registers are not affected by hardware or software reset.

Address 28 - 2B: PN code, write only, no default value

| |
|----------------|
| CODETWO[7:0] |
| CODETWO[15:8] |
| CODETWO[23:16] |
| CODETWO[31:24] |

These registers contain the PN sequence for symbol "010" and "101". PN code registers are not affected by hardware or software reset.

Address 2C - 2F: PN code, write only, no default value

| |
|------------------|
| CODETHREE[7:0] |
| CODETHREE[15:8] |
| CODETHREE[23:16] |
| CODETHREE[31:24] |

These registers contain the PN sequence for symbol "011" and "100". PN code registers are not affected by hardware or software reset.

Address 30 - 37: I/O expansion port A, write only

Address 30 to 37 are the bit-wise address of bit 0 to 7 of I/O expansion port A. The data bit position of each bit in the AD bus is the same as if the bit is addressed through the byte-wise address, i.e. bit 7 is access through AD7 and bit 0 is through AD0.

Address 38 - 3F: I/O expansion port B, write only

Bit-wise address of port B. Access method is the same as port A.

Address 40: I/O expansion port A, write only

This is the byte-wise address of port A. When address 40 is written, all 8 bits of port A are updated at the same time. This port is not affected by hardware or software reset.

Address 41: I/O expansion port B, write only. default: 11111111

This is the byte-wise address of port B. When address 41 is written, all 8 bits of port B are updated at the same time. This port is set by hardware reset and is not affected by software reset.

Address 42: I/O expansion port C, read only

Bit 7 to 0 of this register is mapped to the input port PC[7:0]. This port is not affected by hardware or software reset.

Address 43: I/O expansion port D, read and write. default: 11111111

Bit 7 to 0 of this register is mapped to the I/O port PD[7:0]. When this port is in output mode, write to this register sets the value of PD pins. When this port is in input mode, the value of PD pins are read from this location. This port is set by hardware reset and is not affected by software reset.

Address 44: I/O control, port D, write only. default: 11111111

Bit 1 of this register is the I/O control of port D. When it is one, port D is an input port. When it is zero, port D is an output port and the PD pins are driven by the device. Other bits of this register are reserved. This register is set by hardware reset and it is not affected by software reset.

Address 46 and 47: General purpose timer, write only. default: 00000000

Register 46 and 47 together form a 16-bit number, GPT_CNT. Register 47 is the upper byte and register 46 is the lower byte. GPT_CNT determines the cycle time of the GPT output pin in units of 2400 CLK_IN cycle time. If the device operates at 19.2 MHz, GPT cycle time ranges from 125 μ S to 8.192 sec. GPT always has 50% duty cycle. When GPT_CNT is zero, the GPT output does not toggle. These registers are cleared by hardware reset and are not affected by software reset.

ELECTRICAL CHARACTERISTICS

Absolute Maximum Ratings

| PARAMETER | RATING | UNIT |
|---------------------------------|---|------|
| Storage Temperature | -40 to +125 | °C |
| Power Supply Voltage | -0.3 to +4.5 | V |
| Voltage to 5V Tolerant Pins | -0.3 to +5.5 ⁽¹⁾ | V |
| Voltage to Non-5V Tolerant Pins | -0.3 to V _{DD} +0.3 ⁽¹⁾ | V |

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC Characteristics

V_{DD} = 3.0V ±10%, T_A = 0° to 70° C

| PARAMETER | SYMBOL | MIN. | MAX. | UNIT | TEST CONDITIONS |
|--------------------------------------|------------------|------|------|------|---|
| Supply Voltage | V _{DD} | 2.7 | 3.3 | V | |
| Input High Voltage | V _{IH} | 2.0 | | V | |
| Input Low Voltage | V _{IL} | | 0.8 | V | |
| Input Current, Normal Buffer | I _{I1} | -10 | 10 | μA | |
| Input Current, Buffer with Pull-up | I _{I2} | -200 | 10 | μA | |
| Input Current, Buffer with Pull-down | I _{I3} | -10 | 200 | μA | |
| Tri-state Leakage Current | I _{OZ} | -10 | 10 | μA | |
| Output High Voltage | V _{OH1} | 2.4 | | V | I _{OH} = -2 mA ⁽²⁾ |
| Output High Voltage | V _{OH2} | 2.4 | | V | I _{OH} = -3 mA ^(2, 3) |
| Output High Voltage | V _{OH3} | 2.4 | | V | I _{OH} = -8 mA ⁽²⁾ |
| Output Low Voltage | V _{OL1} | | 0.4 | V | I _{OL} = 2 mA ⁽²⁾ |
| Output Low Voltage | V _{OL2} | | 0.4 | V | I _{OL} = 2 mA ⁽²⁾ |
| Output Low Voltage | V _{OL3} | | 0.4 | V | I _{OL} = 8 mA ⁽²⁾ |
| Sleep Mode Current | I _{DD1} | | | mA | TBD |
| Freeze Mode Current | I _{DD2} | | | mA | TBD |
| Standby Current | I _{DD3} | | | mA | TBD |
| Active Current | I _{DD4} | | | mA | TBD |

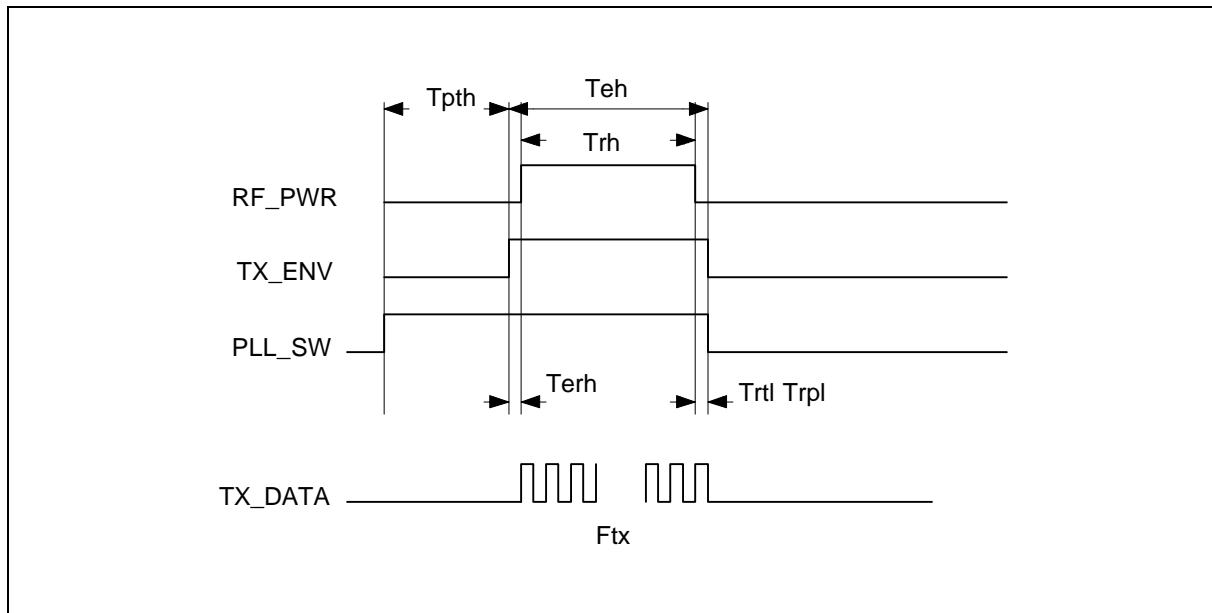
Notes:

- TX_DATA is not 5V Tolerant
- V_{OL1}, V_{OH1} = BSYN_C_OUT, CER, COD_CLK, COD_SYNC, CPU_CLK, DR, ID_DET, IRQ, LOCK, PA, PD, PLL_SW, RF_PWR, RLOCK, TX_ENV, WAKEUP
V_{OL2}, V_{OH2} = AD, ANT_SW, CLK_OUT, GPT, PB
V_{OL3}, V_{OH3} = TX_DATA
- PB[7:4] are open-drain outputs and V_{OH} does not apply.

TIMING WAVEFORMS

RF Module Timing Specifications

| PARAMETER | SYMBOL | VALUE | UNITS | NOTE |
|----------------------------|--------|-------|---------|------|
| TX_ENV High Time | TEH | 2532 | μ S | * |
| TX_ENV High to RF_PWR High | TERH | 4 | μ S | * |
| PLL_SW High to TX_ENV High | TPTH | 470 | μ S | * |
| RF_PWR High Time | TRH | 2524 | μ S | * |
| RF_PWR Low to TX_ENV Low | TRTL | 4 | μ S | * |
| RF_PWR Low to PLL_SW Low | TRPL | 4 | μ S | * |
| TX_DATA Rate | FTX | 1.365 | Mbps | * |

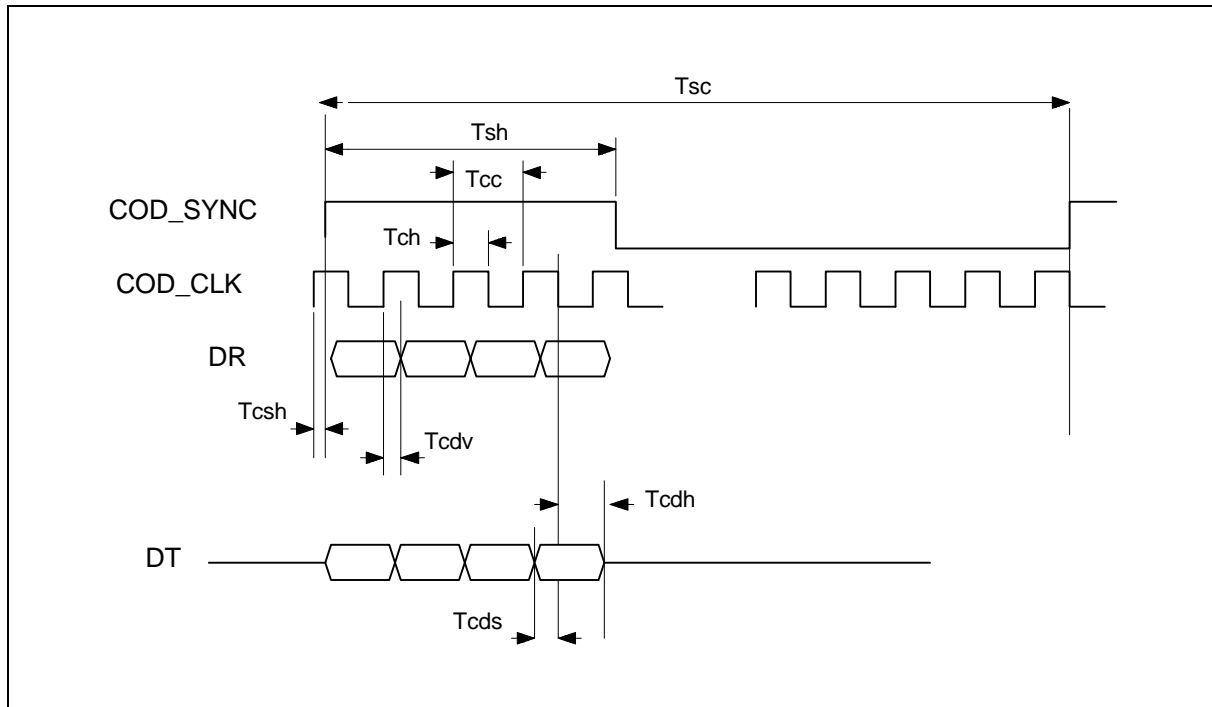


Note *: All RF timing values are linear proportional to CLK_IN frequency. Value assumes CLK_IN at 19.2 MHz

Timing Waveforms, continued

CODEC Interface Timing Specifications

| PARAMETER | SYMBOL | VALUE | UNITS | NOTE |
|-------------------------------|--------|-------|---------|------|
| CLK_IN Frequency | FCLK | 19.2 | MHz | |
| COD_SYNC High Time | TSH | 6.71 | μ S | @ |
| COD_SYNC Cycle Time | TSC | 125 | μ S | @ |
| COD_CLK High Time | TCH | 0.83 | μ S | @ |
| COD_CLK Cycle Time | TCC | 1.67 | μ S | @ |
| COD_CLK High to COD_SYNC High | TCSH | 0.05 | μ S | @ |
| COD_CLK High to DR Valid | TCDV | 0.05 | μ S | |
| DT to COD_CLK Low Setup Time | FCDS | 0.05 | μ S | |
| DT to COD_CLK Low Hold Time | FCDH | 0.05 | μ S | |

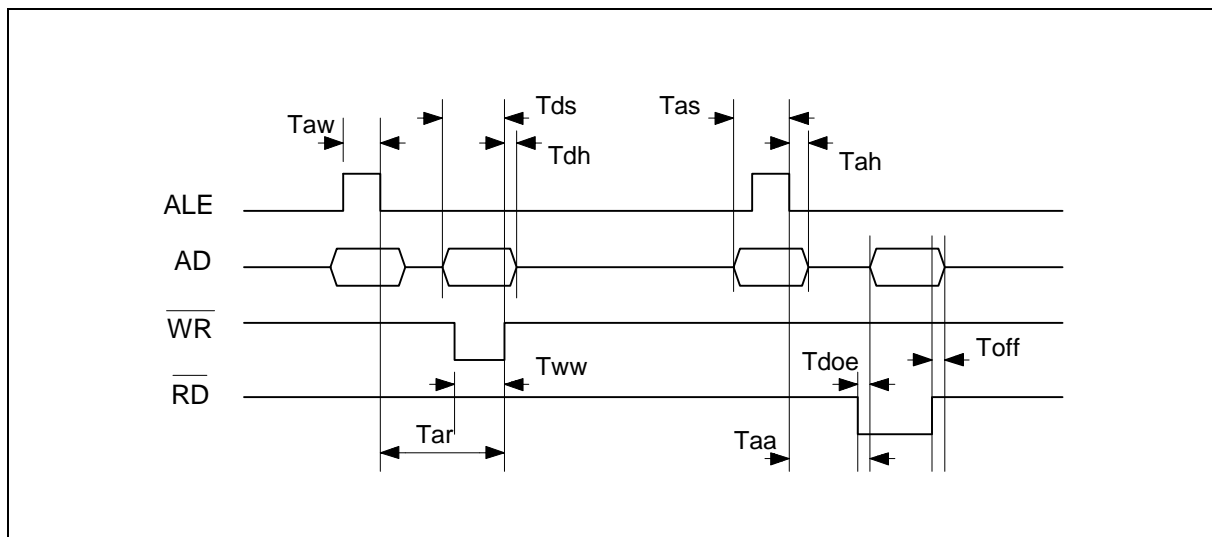


Note @: All timing values are linear proportional to CLK_IN frequency. Value assumes CLK_IN at 19.2 MHz

Timing Waveforms, continued

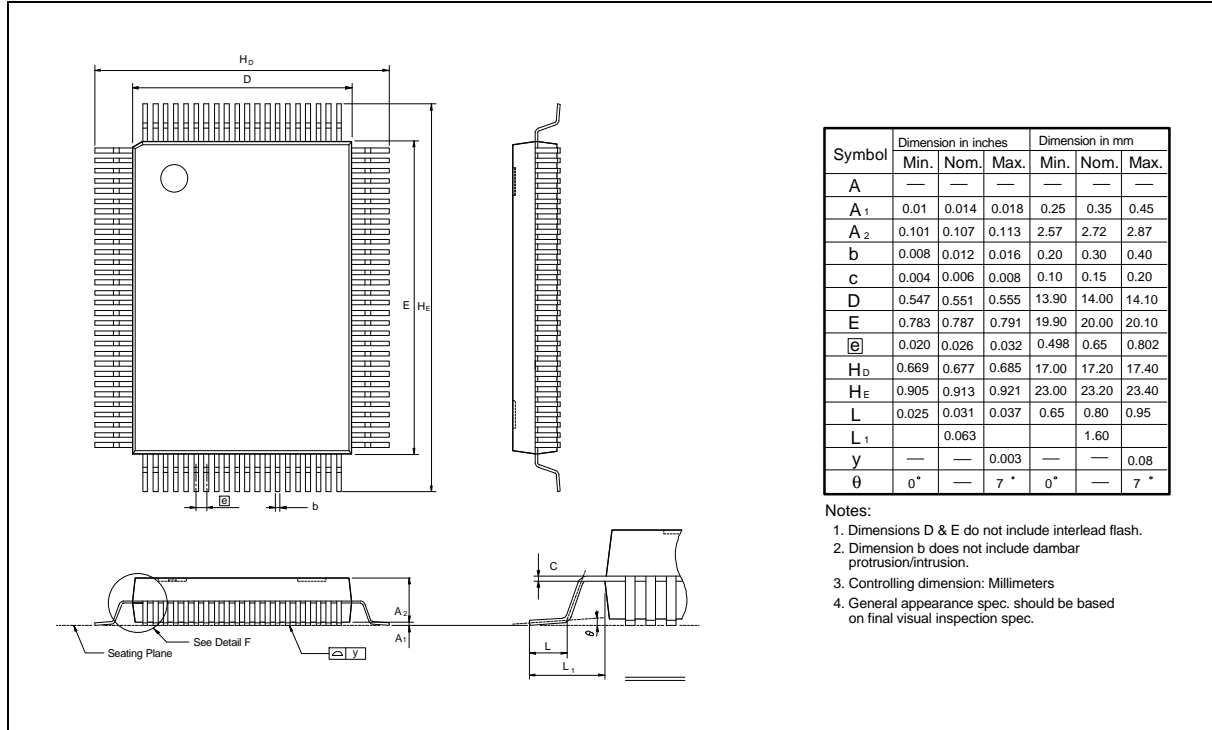
CPU Interface Timing Specifications

| PARAMETER | SYMBOL | MIN. | MAX. | UNITS | NOTE |
|---|--------|------|------|-------|------|
| Address to ALE Setup Time | TAS | 30 | | nS | |
| Address to ALE Hold Time | TAH | 10 | | nS | |
| Data to $\overline{\text{WR}}$ Setup Time | TDS | 30 | | nS | |
| Data to $\overline{\text{WR}}$ Hold Time | TDH | 10 | | nS | |
| $\overline{\text{RD}}$ to Data Output Enable | TDOE | | 20 | nS | |
| $\overline{\text{RD}}$ to Data Output Disable | TOFF | | 15 | nS | |
| ALE Pulse Width | TAW | 40 | | nS | |
| $\overline{\text{WR}}$ Pulse Width | TWW | 40 | | nS | |
| ALE Low to Data Output Valid | TAA | | 45 | nS | |
| ALE Low to $\overline{\text{WR}}$ High | TAR | 40 | | nS | |



PACKAGE DIMENSIONS

100-pin QFP



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Note: All data and specifications are subject to change without notice.

Note: CD/SS technology used in W9330F is developed by Lanwave Components, Inc.