

W91330N SERIES



TONE/PULSE DIALER WITH HANDFREE LOCK AND KEY TONE FUNCTIONS

GENERAL DESCRIPTION

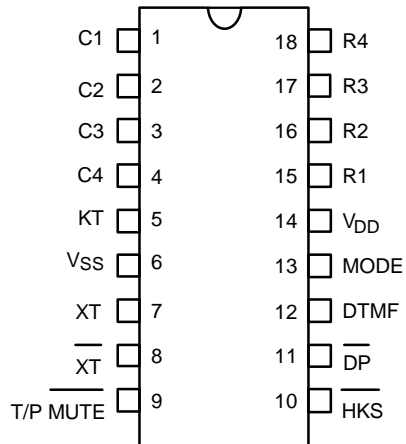
The W91330N series are Si-gate CMOS ICs that provide the necessary signals for tone or pulse dialing. They feature one-key redial, handfree dialing, key tone, redial, and lock functions.

FEATURES

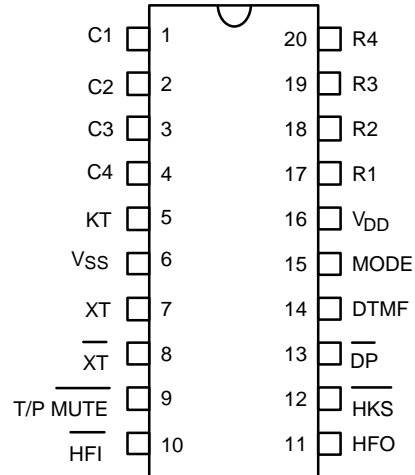
- DTMF/pulse switchable dialer
- 32-digit redial memory
- Pulse-to-tone (*T) keypad for long distance call operation
- Uses 5×4 keyboard
- Easy operation with redial, flash, pause, and */T keypads
- Pause, pulse-to-tone (*T) can be stored as a digit in memory
- 0 or 9 dialing inhibition pin for PABX system or long distance dialing lock out
- Off-hook delay 300 mS in lock mode (\overline{DP} will keep low for 300 mS low while off hook)
- First key-in delay 300 mS output in lock mode
- Dialing rate (10, 20 ppS) selected by bonding option
- Minimum tone output duration: 93 msec.
- Minimum intertone pause: 93 msec.
- Flash break time (73, 100, 300, 600 msec.) selectable by keypad; pause time is 1.0 sec.
- On-chip power-on reset
- Uses 3.579545 MHz crystal or ceramic resonator
- Packaged in 18 or 20-pin plastic DIP
- The different dialers in the W91330N series are shown in the following table:

TYPE NO.	REPLACEMENT TYPE NO.	PULSE (ppS)	FLASH (mS)	M/B	KEY TONE	HANDFREE DIALING	LOCK	PACKAGE (PINS)
W91330N	W91330	10	600/100/300/73	Pin	Yes	-	-	18
W91331N	W91331	20	600/100/300/73	Pin	Yes	-	-	18
W91330AN	W91330A	10	600/100/300/73	Pin	Yes	Yes	-	20
W91331AN	W91331A	20	600/100/300/73	Pin	Yes	Yes	-	20
W91330LN	W91330L	10	600/100/300/73	Pin	-	-	Yes	20
W91330ALN	W91330AL	10	600/100/300/73	Pin	-	Yes	Yes	20

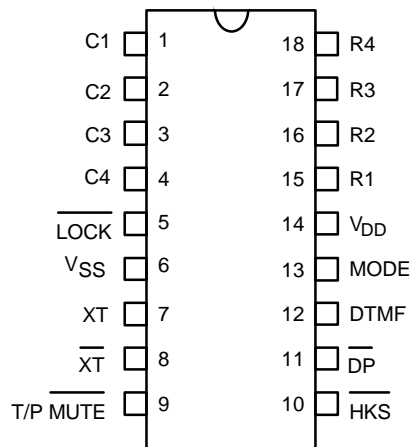
PIN CONFIGURATIONS



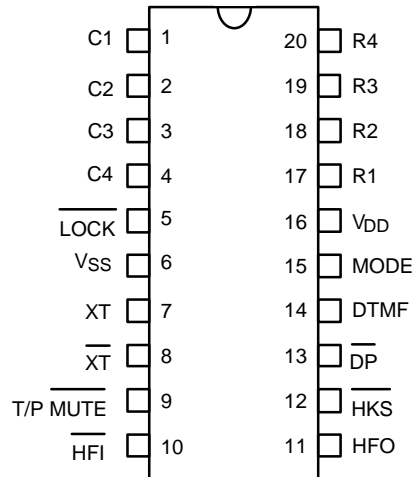
W91330N/W91331N



W91330AN/W91331AN



W91330LN



W91330ALN

PIN DESCRIPTION

SYMBOL	18-PIN	20-PIN	I/O	FUNCTION
Column- Row Inputs	1–4 & 15–18	1–4 & 17–20	I	The keyboard inputs may be used with either the standard 5×4 keyboard or the inexpensive single contact (Form A) keyboard. Electronic input from a μ C can also be used. A valid key-in is defined as a single row being connected to a single column.
XT, $\overline{\text{XT}}$	7, 8	7, 8	I, O	A built-in inverter provides oscillation with an inexpensive 3.579545 MHz crystal or ceramic resonator.
T/P $\overline{\text{MUTE}}$	9	9	O	The T/P $\overline{\text{MUTE}}$ is a conventional CMOS N-channel open drain output. The output transistor is switched on during dialing sequence, one-key redial break, and flash break time. Otherwise, it is switched off.
MODE	13	15	I	Pulling mode pin to Vss places the dialer in tone mode. Pulling mode pin to VDD places the dialer in pulse mode. (10 ppS; 20 ppS for W91331N/W91331AN, M/B = 40:60) Floating mode pin places the dialer in pulse mode. (10 ppS; 20 ppS for W91331N/W91331AN, M/B = 33.3:66.7).
$\overline{\text{HKS}}$	10	12	I	Hook switch input. $\overline{\text{HKS}} = \text{VDD}$: On-hook state. Chip in sleeping mode, no operation. $\overline{\text{HKS}} = \text{Vss}$: Off-hook state. Chip enabled for normal operation. $\overline{\text{HKS}}$ pin is pulled to VDD by internal resistor.
$\overline{\text{DP}}$	11	13	O	N-channel open drain dialing pulse output. Flash key will cause $\overline{\text{DP}}$ to be active in either tone mode or pulse mode. The timing diagram for pulse mode is shown in Figure 1(a, b, c, d).
VDD, VSS	14, 6	16, 6	I	Power input pins.

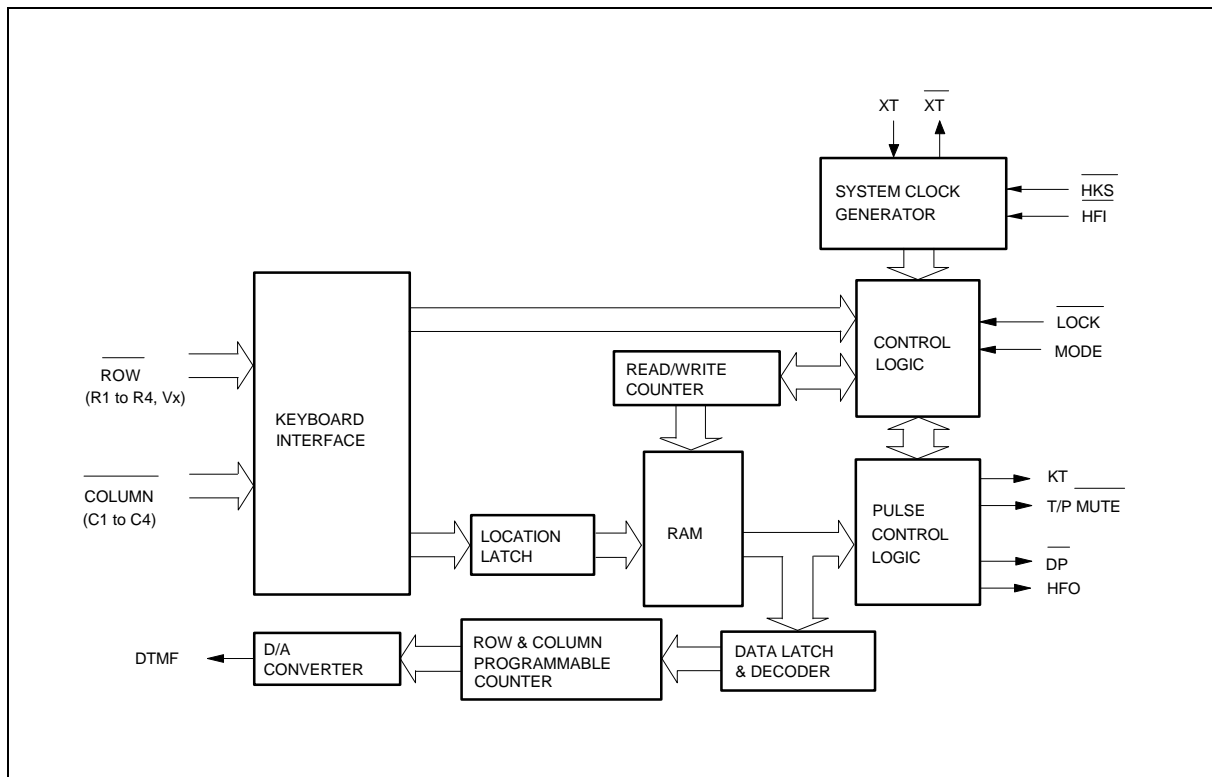
Pin Description, continued

SYMBOL	18-PIN	20-PIN	I/O	FUNCTION																																								
DTMF	12	14	O	<p>In pulse mode, this pin remains in low state at all times. In tone mode, it will output a dual or single tone. Detailed timing diagram for tone mode is shown in Figure 2(a, b, c, d).</p> <table><tr><th colspan="4">Output Frequency</th></tr><tr><th></th><th>Specified</th><th>Actual</th><th>Error %</th></tr><tr><td>R1</td><td>697</td><td>699</td><td>+0.28</td></tr><tr><td>R2</td><td>770</td><td>766</td><td>-0.52</td></tr><tr><td>R3</td><td>852</td><td>848</td><td>-0.47</td></tr><tr><td>R4</td><td>941</td><td>948</td><td>+0.74</td></tr><tr><td>C1</td><td>1209</td><td>1216</td><td>+0.57</td></tr><tr><td>C2</td><td>1336</td><td>1332</td><td>-0.30</td></tr><tr><td>C3</td><td>1477</td><td>1472</td><td>-0.34</td></tr></table>	Output Frequency					Specified	Actual	Error %	R1	697	699	+0.28	R2	770	766	-0.52	R3	852	848	-0.47	R4	941	948	+0.74	C1	1209	1216	+0.57	C2	1336	1332	-0.30	C3	1477	1472	-0.34				
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$\overline{\text{HFI}}$, HFO	-	10, 11	I, O	<p>Handfree control pins. The handfree control state is toggled on by a low pulse on the $\overline{\text{HFI}}$ input pin. The status of the handfree control state is described in the following table:</p> <table><tr><th colspan="2">CURRENT STATE</th><th colspan="3">NEXT STATE</th></tr><tr><th>Hook SW.</th><th>HFO</th><th>Input</th><th>HFO</th><th>Dialing</th></tr><tr><td>—</td><td>Low</td><td>$\overline{\text{HFI}} \downarrow$</td><td>High</td><td>Yes</td></tr><tr><td>On Hook</td><td>High</td><td>$\overline{\text{HFI}} \downarrow$</td><td>Low</td><td>No</td></tr><tr><td>Off Hook</td><td>High</td><td>$\overline{\text{HFI}} \downarrow$</td><td>Low</td><td>Yes</td></tr><tr><td>On Hook</td><td>—</td><td>Off Hook</td><td>Low</td><td>Yes</td></tr><tr><td>Off Hook</td><td>Low</td><td>On Hook</td><td>Low</td><td>No</td></tr><tr><td>Off Hook</td><td>High</td><td>On Hook</td><td>High</td><td>Yes</td></tr></table> <p>$\overline{\text{HFI}}$ pin is pulled to VDD by internal resistor.</p> <p>Detailed timing diagrams are shown in Figure 3.</p>	CURRENT STATE		NEXT STATE			Hook SW.	HFO	Input	HFO	Dialing	—	Low	$\overline{\text{HFI}} \downarrow$	High	Yes	On Hook	High	$\overline{\text{HFI}} \downarrow$	Low	No	Off Hook	High	$\overline{\text{HFI}} \downarrow$	Low	Yes	On Hook	—	Off Hook	Low	Yes	Off Hook	Low	On Hook	Low	No	Off Hook	High	On Hook	High	Yes
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Off Hook	High	On Hook	High	Yes																																								
KT	5 (except W91330LN)	5 (except W91330ALN)	O	<p>Key-tone signal output. The key tone is generated for all valid keys. Frequency is 600 Hz and duration is 35 mS.</p>																																								

Pin Description, continued

SYMBOL	18-PIN	20-PIN	I/O	FUNCTION								
<div>LOCK</div>	<div>5</div> <div>(W91330LN only)</div>	<div>5</div> <div>(W91330ALN only)</div>	<div>I</div>	<div>The function of this terminal is to prevent "0" dialing and "9" dialing under PABX system long distance call control. When the first key input after reset is 0 or 9, all key inputs, including the 0 or 9 key, become invalid and the chip generates no output. The telephone is reinitialized by a reset.</div> <table><tr><th>LOCK PIN</th><th>FUNCTION</th></tr><tr><td>Floating</td><td>Normal dialing mode</td></tr><tr><td>VDD</td><td>"0," "9" dialing inhibited</td></tr><tr><td>VSS</td><td>"0" dialing inhibited</td></tr></table>	LOCK PIN	FUNCTION	Floating	Normal dialing mode	VDD	"0," "9" dialing inhibited	VSS	"0" dialing inhibited
LOCK PIN	FUNCTION											
Floating	Normal dialing mode											
VDD	"0," "9" dialing inhibited											
VSS	"0" dialing inhibited											

BLOCK DIAGRAM





FUNCTIONAL DESCRIPTION

Keyboard Operation

C1	C2	C3	C4	
1	2	3		R1
4	5	6	F1	R2
7	8	9	F2	R3
*/T	0	#	R/P1	R4
R/P2	R	F3	F4	Vx

- R: One-key redial function
- R/P1, R/P2: Redial and pause function key, P1 is 3.6 sec. and P2 is 2.0 sec.
- */T: * in tone mode and P→T in pulse mode
- F1, ..., F4: Flash keys, F1 = 600 mS, F2 = 100 mS, F3 = 300 mS, F4 = 73 mS

Notes: D1, ..., Dn, D1', ..., Dn': 0, ..., 9, */T, #

R/P: R/P1 or R/P2.

Fn: F1, ..., F4

Normal Dialing

OFF HOOK (or ON HOOK & $\overline{\text{HFI}} \ \overline{\text{IO}}$), D1, D2, ..., Dn

1. D1, D2, ..., Dn will be dialed out.
2. Dialing length is unlimited, but redial is inhibited if length oversteps 32 digits in normal dialing.

Redialing

OFF HOOK (or ON HOOK & $\overline{\text{HFI}} \ \overline{\text{IO}}$), D1, D2, ..., Dn Busy,

Come ON HOOK, OFF HOOK (or ON HOOK & $\overline{\text{HFI}} \ \overline{\text{IO}}$), R/P

- The redial memory content will be dialed out.
- The R/P key can execute the redial function only as the first key-in after off-hook; otherwise, it executes pause function.

- If redialing length oversteps 32 digits, the redialing function will be inhibited.

OFF HOOK (or ON HOOK G $\overline{\text{HFI}}$ ☐ ☐ ☐ ☐ ☐



- If the pulses of the dialed digits $\boxed{D1}$ to \boxed{Dn} have not finished, \boxed{R} will be ignored.
- The redial function by \boxed{R} key has no break time (2.2 sec.) if it is the first key in after off-hook.
- The \boxed{R} key uses the same redial buffer as the redial function $\boxed{R/P1}$ or $\boxed{R/P2}$ key, and it is activated during normal dialing or repertory dialing.

Access Pause

$\boxed{\text{OFF HOOK}}$ (or $\boxed{\text{ON HOOK}}$ & $\boxed{\overline{\text{HFI}} \ \overline{\text{I}\hat{\text{O}}}}$), $\boxed{D1}$, $\boxed{D2}$, $\boxed{R/P}$, $\boxed{D3}$, ..., \boxed{Dn}

1. The pause function can be stored in memory.
2. The pause function is executed in normal dialing, redial dialing, or memory dialing.
3. The pause duration of 2.0 or 3.6 seconds per pause is selected by keypad.
4. The detailed timing diagram for the pause function is shown in Figure 5.
5. Only one pause function can be released to user.

Pulse-to-tone (*T)

$\boxed{\text{OFF HOOK}}$ (or $\boxed{\text{ON HOOK}}$ & $\boxed{\overline{\text{HFI}} \ \overline{\text{I}\hat{\text{O}}}}$), $\boxed{D1}$, $\boxed{D2}$, ..., \boxed{Dn} , $\boxed{*/T}$, $\boxed{D1'}$, $\boxed{D2'}$, ..., $\boxed{Dn'}$

1. If the mode switch is set to pulse mode, then the output signal will be:
 $D1, D2, \dots, Dn, \text{Pause (2.0 sec. or 3.6 sec.)}, D1', D2', \dots, Dn'$
(Pulse) (Tone)
If pause1 is excuted, the pause time of pulse-to-tone function is 3.6S. If pause2 is excuted, the pause time of the pulse-to-tone function is 2.0S.
2. If the mode switch is set to tone mode, then the output signal will be as follows:
 $D1, D2, \dots, Dn, *, D1', D2', \dots, Dn'$
(Tone) (Tone)
3. The dialer remains in tone mode when the digits have been dialed out and can be reset to pulse mode only by going on-hook.
4. The pulse-to-tone function timing diagram is shown in Figure 6.

Flash

$\boxed{\text{OFF HOOK}}$ (or $\boxed{\text{ON HOOK}}$ & $\boxed{\overline{\text{HFI}} \ \overline{\text{I}\hat{\text{O}}}}$), \boxed{Fn}

1. $Fn = F1, \dots, F4$
2. The dialer will execute flash break time of 600 mS (F1), 100 mS (F2), 300 mS (F3), or 73 mS (F4) before the next digit is dialed out. In each case, the pause time is 1.0 sec.

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- Flash key cannot be stored as a digit in memory. The flash key has the first priority among the keyboard functions.
- The system will return to the initial state after the flash pause time is finished.
- The flash function timing diagram is shown in Figure 7.

ABSOLUTE MAXIMUM RATINGS

PARAMETER	SYMBOL	RATING	UNIT
DC Supply Voltage	V _{DD} -V _{SS}	-0.3 to +7.0	V
Input/Output Voltage	V _{IL}	V _{SS} -0.3	V
	V _{IH}	V _{DD} +0.3	V
	V _{OL}	V _{SS} -0.3	V
	V _{OH}	V _{DD} + 0.3	V
Power Dissipation	P _D	120	mW
Operation Temperature	T _{OPR}	-20 to +70	°C
Storage Temperature	T _{STG}	-55 to +150	°C

Note: Exposure to conditions beyond those listed under Absolute Maximum Ratings may adversely affect the life and reliability of the device.

DC CHARACTERISTICS

(V_{DD}-V_{SS} = 2.5V, F_{osc} = 3.579545 MHz, T_A = 25° C, all outputs unloaded)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Operating Voltage	V _{DD}	-	2.0	-	5.5	V
Operating Current	I _{OP}	Tone, Unloaded	-	0.4	0.6	mA
		Pulse, Unloaded	-	0.2	0.4	
Standby Current	I _{SB}	$\overline{\text{HKS}} = \text{V}_{\text{SS}}$, No load & No key entry	-	-	15	μA
Memory Retention Current	I _{MR}	$\overline{\text{HKS}} = \text{V}_{\text{DD}}$, V _{DD} = 1.0V	-	-	0.2	μA
DTMF Output Voltage	V _{TO}	Row group, R _L = 5 KΩ	130	150	170	mVrms
Pre-emphasis		Col/Row, V _{DD} = 2.0 to 5.5V	1	2	3	dB
DTMF Distortion	THD	R _L = 5 KΩ, V _{DD} = 2.0 to 5.5V	-	-30	-23	dB

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DC Characteristics, continued

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
DTMF Output DC Level	VTDC	$R_L = 5\text{ K}\Omega$, $V_{DD} = 2.0\text{ to }5.5\text{V}$	1.0	-	3.0	V
DTMF Output Sink Current	ITL	$V_{TO} = 0.5\text{V}$	0.2	-	-	mA
$\overline{\text{DP}}$ Output Sink Current	IPL	$V_{PO} = 0.5\text{V}$	0.5	-	-	mA
T/P $\overline{\text{MUTE}}$ Output Sink Current	ITML	$V_{TMO} = 0.5\text{V}$	0.5	-	-	mA
Key Tone Output Current	IKTH	$V_{KTH} = 2.0\text{V}$	0.5	-	-	mA
	IKTL	$V_{KTL} = 0.5\text{V}$	0.5	-	-	mA
HFO Drive/Sink Current	IHFH	$V_{HFH} = 2.0\text{V}$	0.5	-	-	mA
	IHFL	$V_{HFL} = 0.5\text{V}$	0.5	-	-	mA
Keypad Input Drive Current	IKD	$V_I = 0.0\text{V}$	30	-	-	μA
Keypad Input Sink Current	IKS	$V_I = 2.5\text{V}$	200	400	-	μA
HKS I/P Pull-High Resistor	RHK	-	-	300	-	$\text{K}\Omega$
Keypad Resistance	RK	-	-	-	5	$\text{K}\Omega$

AC CHARACTERISTICS

($V_{DD} - V_{SS} = 2.5\text{V}$, $F_{osc} = 3.579545\text{ MHz}$, $T_A = 25^\circ\text{C}$, all outputs unloaded.)

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Key-in Debounce	TKID	-	-	20	-	mS
Key Release Debounce	TKRD	-	-	20	-	mS
Off-Hook Delay	TOFD	Lock only	-	300	-	mS
First Key-in Delay	TFKD	Lock only	-	300	-	mS
Pre-digit-pause1	TPDP1 10 ppS	Mode = V_{DD}	-	40	-	mS
		Mode = Floating	-	33.3	-	
Pre-digit-pause2	TPDP2 20 ppS	Mode = V_{DD}	-	20	-	mS
		Mode = Floating	-	16.7	-	
Interdigit Pause (Auto Dialing)	TIDP	10 ppS	-	800	-	mS
		20 ppS	-	500	-	

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Revision A2

AC Characteristics, continued

PARAMETER	SYMBOL	CONDITIONS	MIN.	TYP.	MAX.	UNIT
Make/Break Ratio	M:B	Mode = V _{DD}	-	40:60	-	%
		Mode = Floating	-	33.3:66.7	-	
Tone Output Duration	T _{TD}	Auto dialing	-	93	-	mS
Intertone Pause	T _{ITP}	Auto dialing	-	93	-	mS
Flash Break Time	T _{FB}	F1	-	600	-	mS
		F2	-	100	-	
		F3	-	300	-	
		F4	-	73	-	
Flash Pause Time	T _{FP}	F1, F2, F3, F4	-	1.0	-	S
Pause Time	T _P	R/P1	-	3.6	-	S
		R/P2	-	2.0	-	
Key Tone Frequency	F _{KT}	-	-	600	-	Hz
Key Tone Duration	T _{KTD}	-	-	35	-	mS
One-Key Redial Break Time	T _{RB}	-	-	2.2	-	S
One-Key Redial Pause Time	T _{RP}	-	-	0.6	-	S

Notes:

- Crystal parameters suggested for proper operation are R_s < 100 Ω, L_m = 96 mH, C_m = 0.02 pF, C_n = 5 pF, C_I = 18 pF, F_{osc.} = 3.579545 MHz ± 0.02%.
- Crystal oscillator accuracy directly affects these times.

TIMING WAVEFORMS

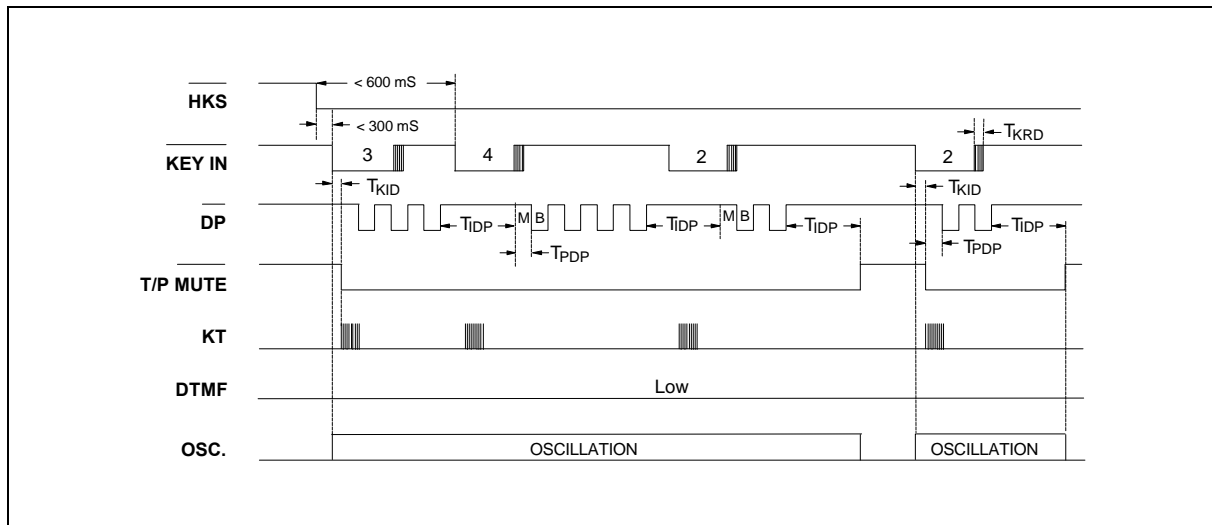


Figure 1(a). Normal Dialing Timing Diagram (Pulse Mode Without Lock Function)

Timing Waveforms, continued

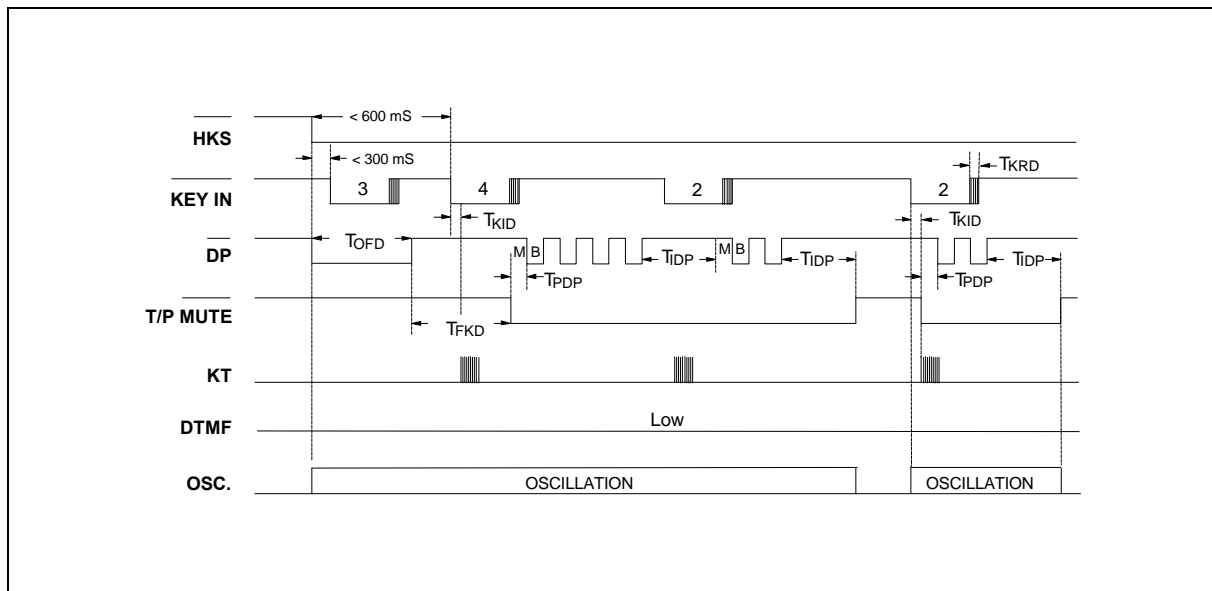


Figure 1(b). Normal Dialing Timing Diagram (Pulse Mode with Lock Function)

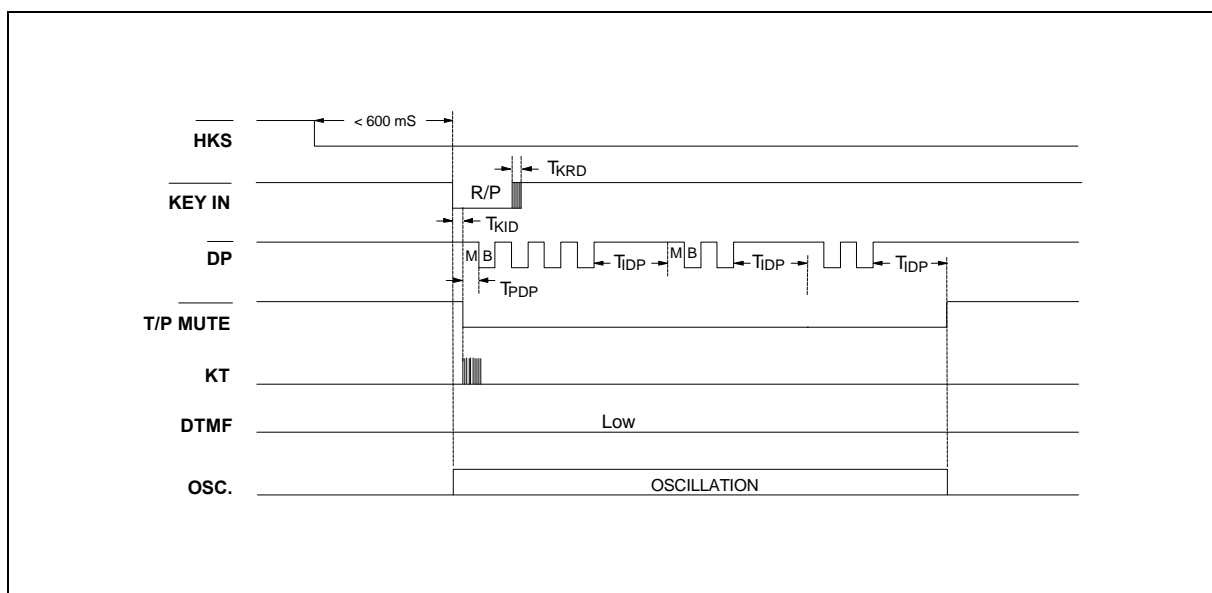


Figure 1(c). Auto Dialing Timing Diagram (Pulse Mode Without Lock Function)

Timing Waveforms, continued

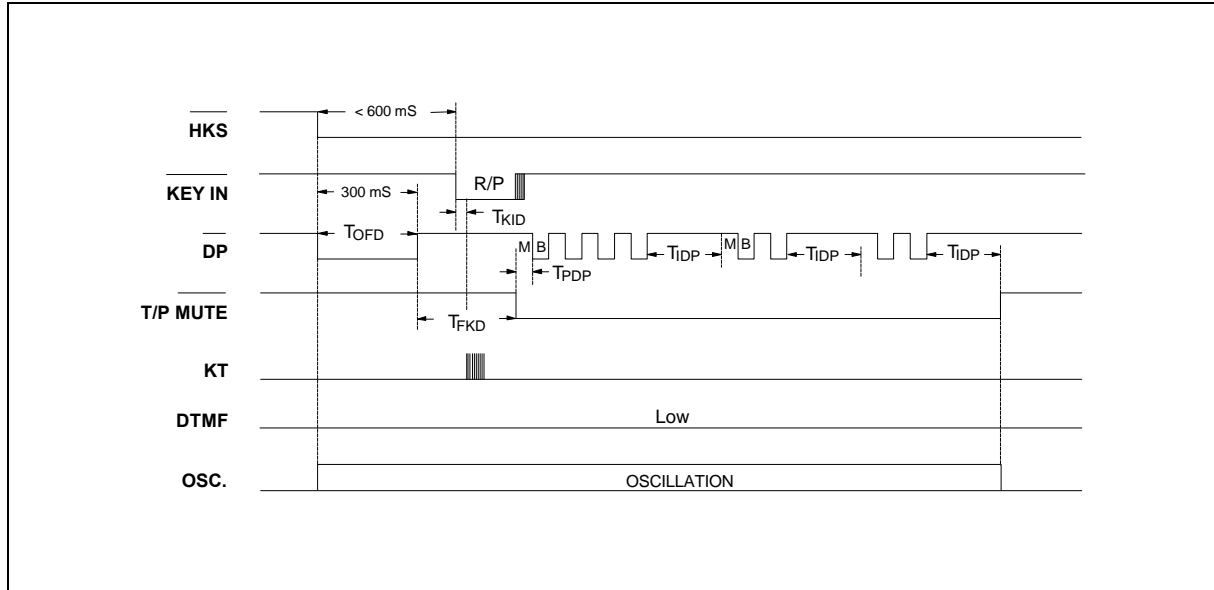


Figure 1(d). Auto Dialing Timing Diagram (Pulse Mode with Lock Function)

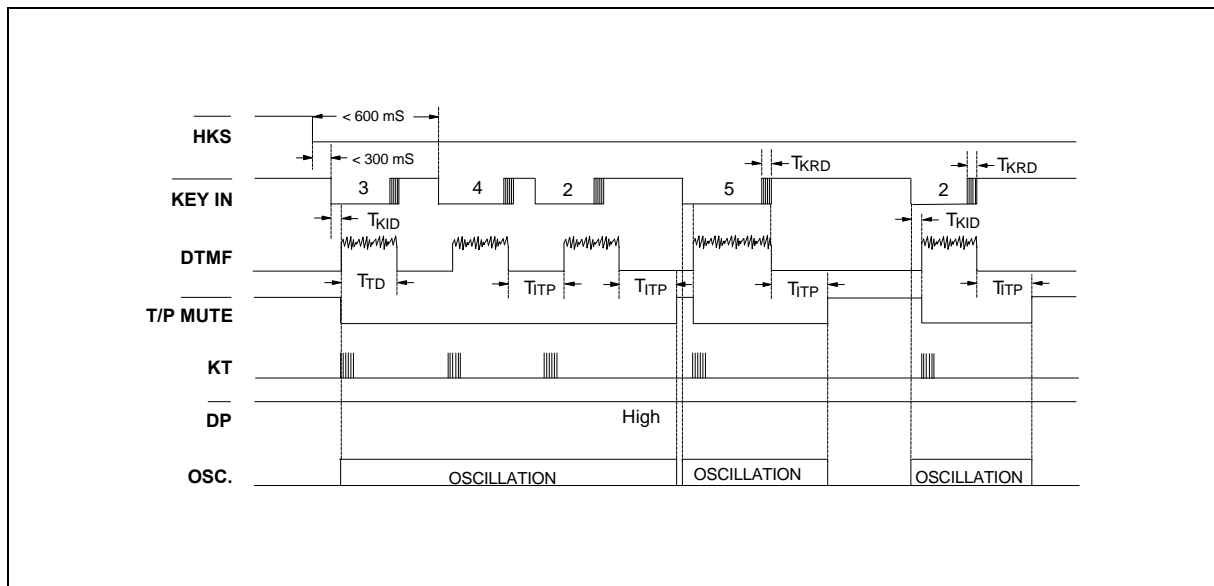


Figure 2(a). Normal Dialing Timing Diagram (Tone Mode Without Lock Function)

Timing Waveforms, continued

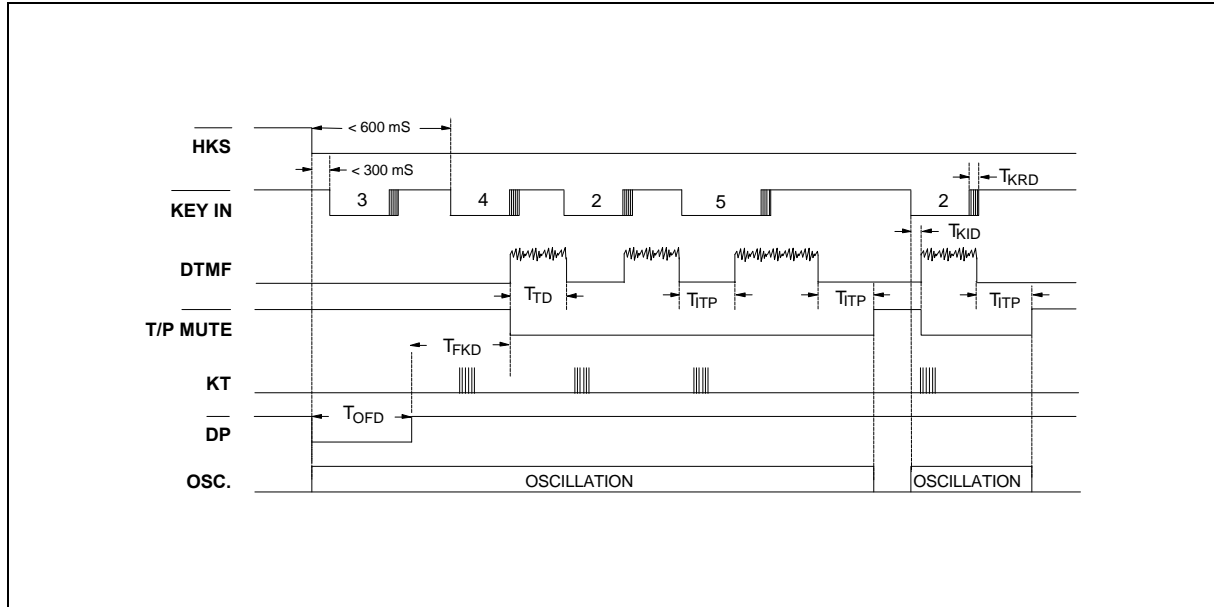


Figure 2(b). Normal Dialing Timing Diagram (Tone Mode with Lock Function)

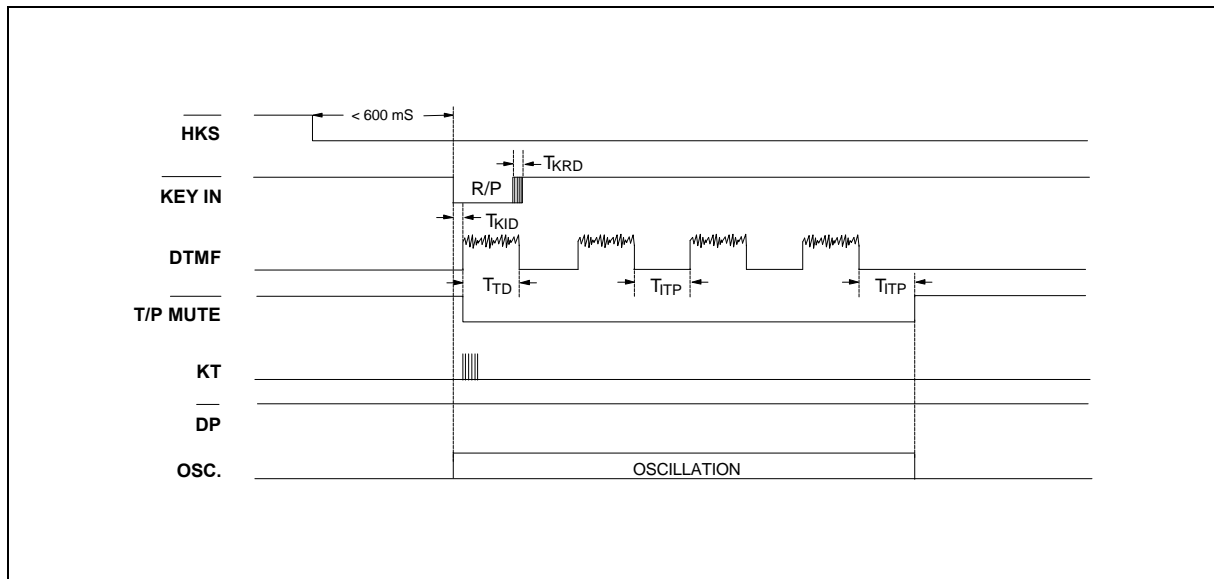


Figure 2(c). Auto Dialing Timing Diagram (Tone Mode Without Lock Function)

Timing Waveforms, continued

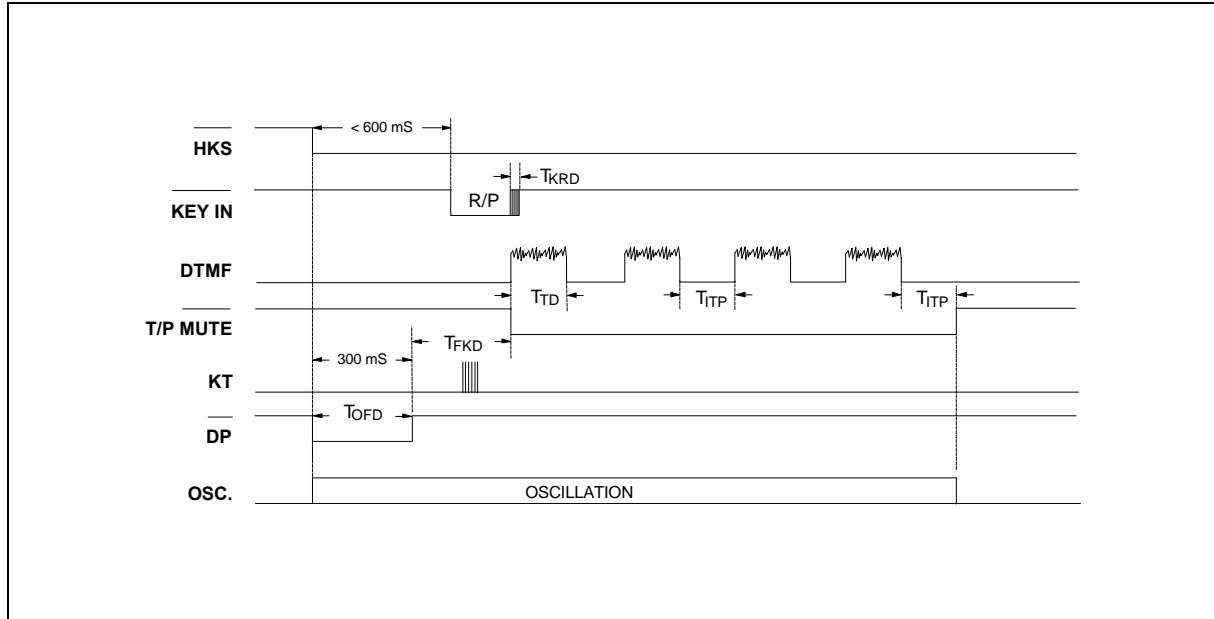


Figure 2(d). Auto Dialing Timing Diagram (Tone Mode with Lock Function)

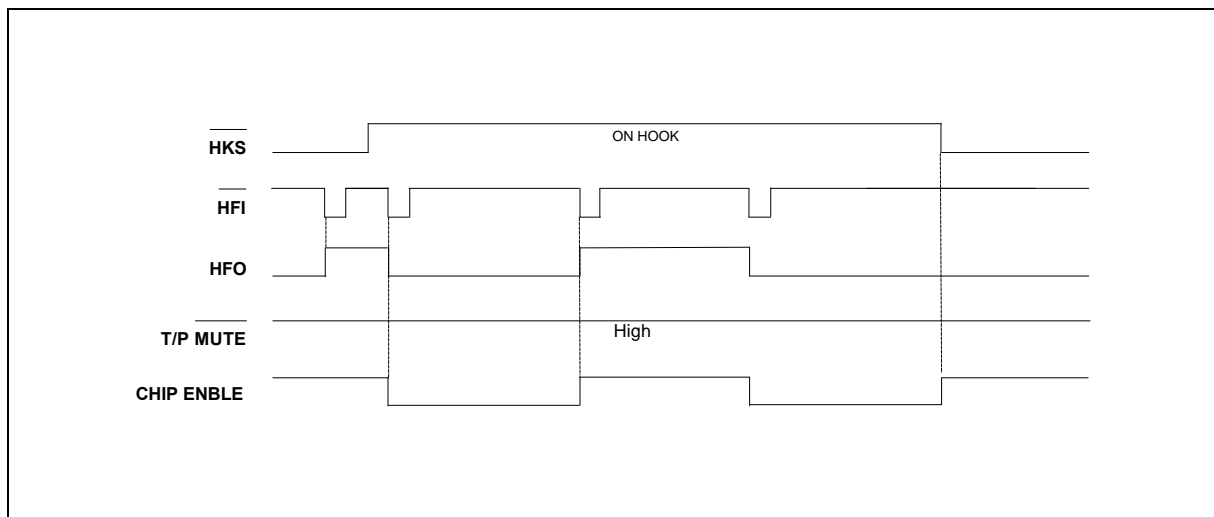


Figure 3. Handfree Dialing Timing Diagram

Timing Waveforms, continued

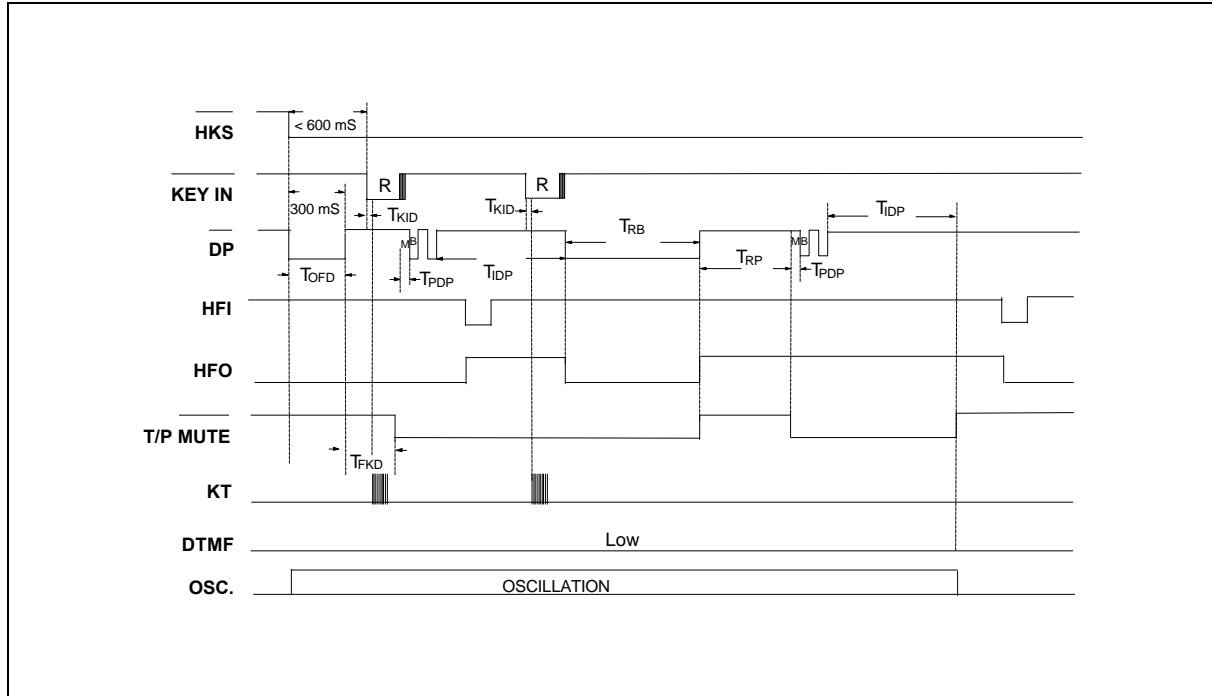


Figure 4. One-key Redial Timing Diagram (Pulse Mode)

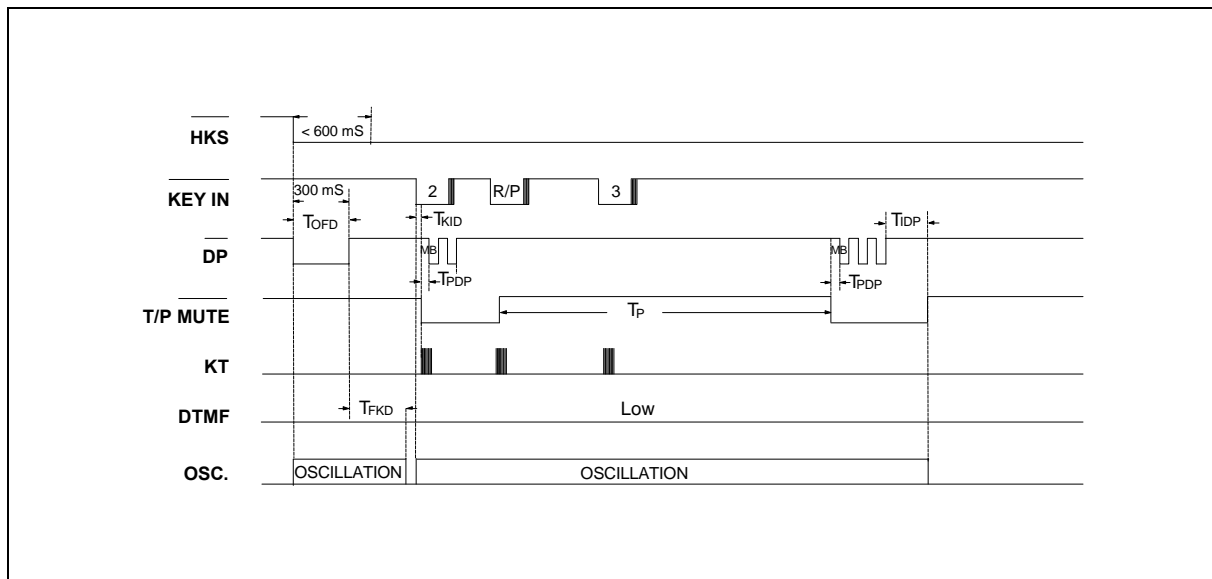


Figure 5. Pause Function Timing Diagram

Timing Waveforms, continued

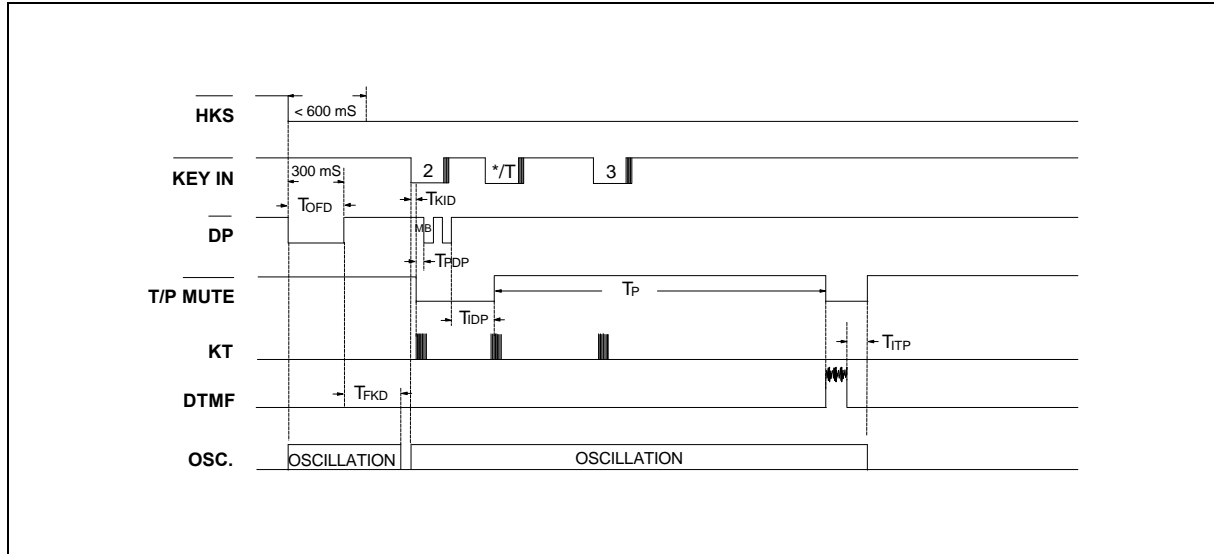


Figure 6. Pulse-to-tone Timing Diagram

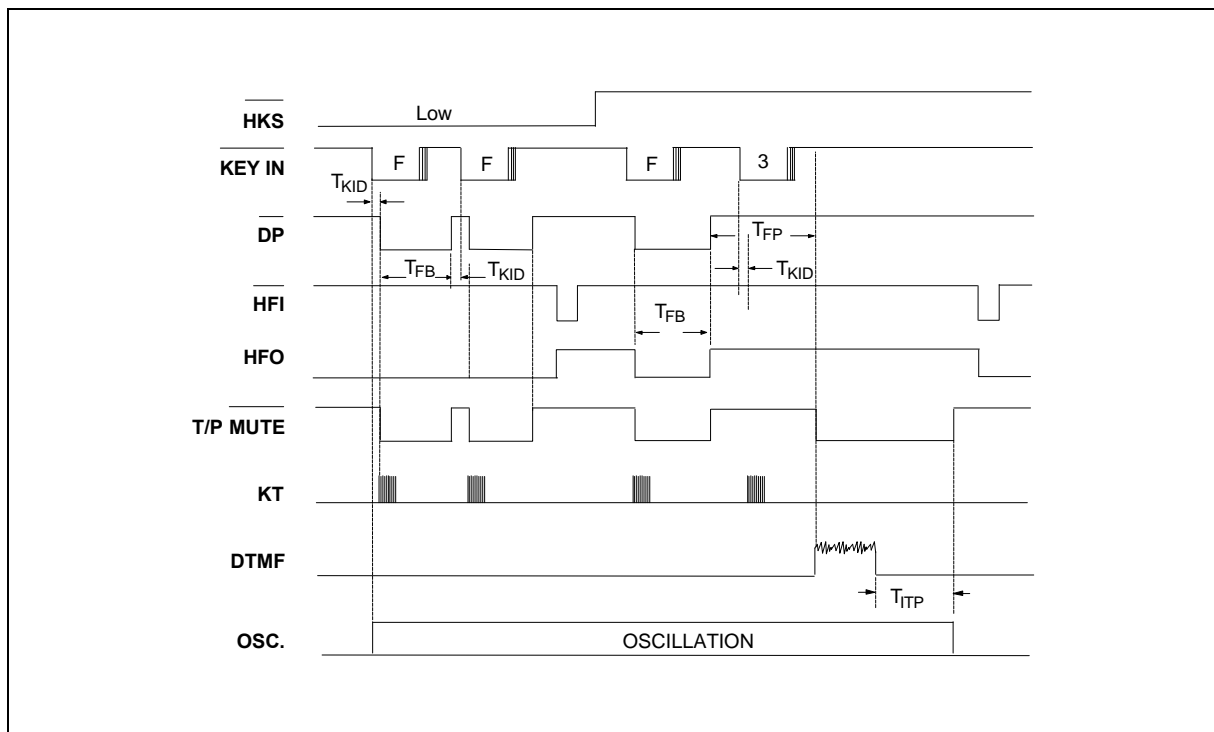


Figure 7. Flash Timing Diagram



W91330N SERIES

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Note: All data and specifications are subject to change without notice.