

## Test report

### Absolute maximum ratings

Parameters	Symbol	Value	Unit	Test no.
Output drain voltage Pin 5, 6, 7, 8	$V_{OD}$	20	V	84, 85, 86, 87
Analogue supply voltage Pin 16 (with 220 $\Omega$ seriell resistance one minute)	$V_A$ $V_A$	8 to 16 24	V V	24

### Electrical characteristics

$V_{DD} = 5\text{ V}$ ,  $T_{amb} = 25^\circ\text{C}$ , unless otherwise specified

Parameters	Test conditions / Pin	Symbol	Min.	Typ.	Max.	Unit	Test no.
Supply voltage	Pin 1	$V_{DD}$	4.5	5.0	5.5	V	–
Quiescent supply current	Pin 1	$I_{DD}$		6.0	11.6	mA	27
<b>FM input sensitivity, FMOSC Pin 9</b>							
$f_i = 70\text{ to }120\text{ MHz}$	$R_G = 50\ \Omega$	$V_{SFM}$	25			mV	168, 169, 170, 171
$f_i = 120\text{ to }130\text{ MHz}$	$R_G = 50\ \Omega$	$V_{SFM}$	50			mV	177
<b>AM input sensitivity, AMOSC Pin 11</b>							
$f_i = 0.5\text{ to }35\text{ MHz}$	$R_G = 50\ \Omega$	$V_{SAM}$	25			mV	150, 151, 152, 153, 154, 155
<b>Oscillator input sensitivity, OSCIN Pin 18</b>							
$f_i = 0.1\text{ to }15\text{ MHz}$	$R_G = 50\ \Omega$	$V_{SOSC}$	100			mV	Digital test: ok or not ok
<b>Switching output SWO 1, SWO 2, SWO 3, SWO 4 (open drain) Pins 5, 6, 7 and 8</b>							
Output voltage LOW	$I_L = 1\text{ mA}$	$V_{SWOL}$		200	400	mV	48, 49, 50, 51
Output voltage LOW	$I_L = 0.1\text{ mA}$	$V_{SWOL}$		20	100	mV	52, 53, 54
Output leakage current HIGH	$V_5, V_6, V_7, V_8 = 20\text{ V}$	$I_{OHL}$			100	nA	84, 85, 86, 87
<b>Phase detector PDFM Pin 13</b>							
Output current 1		$\pm I_{PDFM}$	400	500	600	$\mu\text{A}$	56, 57
Output current 2		$\pm I_{PDFM}$	100	125	150	$\mu\text{A}$	58, 59
Leakage current					20	nA	92
<b>Phase detector PDAM Pin 14</b>							
Output current 1		$\pm I_{PDAM}$	75	100	125	$\mu\text{A}$	88, 89
Output current 2		$\pm I_{PDAM}$	20	25	30	$\mu\text{A}$	90, 91
Leakage current					20	nA	60
<b>Analogue output PDFMO, PDAMO Pins 12 and 15</b>							
Saturation voltage	$I = 15\text{ mA}$	$V_{sat}$		270	400	mV	46, 83

## Electrical characteristics

$V_{DD} = 5\text{ V}$ ,  $T_{amb} = 25^\circ\text{C}$ , unless otherwise specified

Parameters	Test conditions / Pin	Symbol	Min.	Typ.	Max.	Unit	Test No.
I <sup>2</sup> C bus SCL, SDA, AS							
Input voltage HIGH LOW	Pin 2, 3, 4	V <sub>iBUS</sub>	3.0 0		V <sub>DD</sub> 1.5	V V	Digital test: ok or not ok
Output voltage Acknowledge LOW	Pin 3 I <sub>SDA</sub> = 3 mA	V <sub>O</sub>			0.4	V	
Clock frequency	Pin 2	f <sub>SCL</sub>			100	kHz	
Rise time SDA, SCL	Pin 2, 3	t <sub>r</sub>			1	µs	
Fall time SDA, SCL	Pin 2, 3	t <sub>f</sub>			300	ns	
Period of SCL HIGH LOW	Pin 2 HIGH LOW	t <sub>H</sub> t <sub>L</sub>	4.0 4.7			µs µs	
Setup time							
Start condition Data Stop condition Time the bus must be free before a new transmission can be started		t <sub>sSTA</sub> t <sub>sDAT</sub> t <sub>sSTOP</sub>  t <sub>wSTA</sub>	4.7 250 4.7  4.7			µs ns µs  µs	Digital test: ok or not ok
Hold time							
Start condition DATA		t <sub>hSTA</sub> t <sub>hDAT</sub>	4.0 0			µs µs	Digital test: ok or not ok

## Bus timing

