

**UHF television tuners****KS-D-134/134A****FEATURES**

- Member of the KS-130 family small sized UHF tuner
- Systems CCIR: I
- Digitally controlled (PLL) tuning via I<sup>2</sup>C-bus
- World standardized mechanical dimensions and world standard pinning
- Compact size
- Comply to "CENELEC EN55020" and "EN55013"

**MARKING**

The following items of information are printed on a sticker that is on the top cover of the tuner or printed directly on the top cover:

- Company logo
- Type number
- Year and month code
- Quality inspection print

**DESCRIPTION**

The KS-D-134/134A tuners belongs to the KS-130 family of tuners, which are designed to meet a wide range of applications. The IF output can drive a SAW filter directly and has capability to drive a symmetrical or asymmetrical load.

The tuners comply with the requirements of radiation, signal handling capability and immunity conforming with:

- CISPR 13 (1990) include. amendment 1 (1992) and amendment 2 (1993)
- European standards CENELEC EN55013, EN55020

**ORDERING INFORMATION**

TYPE	SYSTEM	DESCRIPTION
KS-D-134 E	CCIR	symmetrical IF output; IEC connector (14.5 mm), I <sup>2</sup> C status byte
KS-D-134 EA	CCIR	asymmetrical IF output; IEC connector (14.5 mm), I <sup>2</sup> C status byte

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**KS-D-134/134A**

## INTERMEDIATE FREQUENCIES

SIGNAL	FREQUENCY (MHz)
Picture carrier	38.90
Colour	34.47
Sound	32.90

### Note

1. The oscillator frequency is above the input signal frequency.

## CHANNEL COVERAGE

BAND	OFF-AIR CHANNELS	
	CHANNELS	FREQUENCY RANGE (MHz)
UHF	E21 to E69	471.25 to 855.25

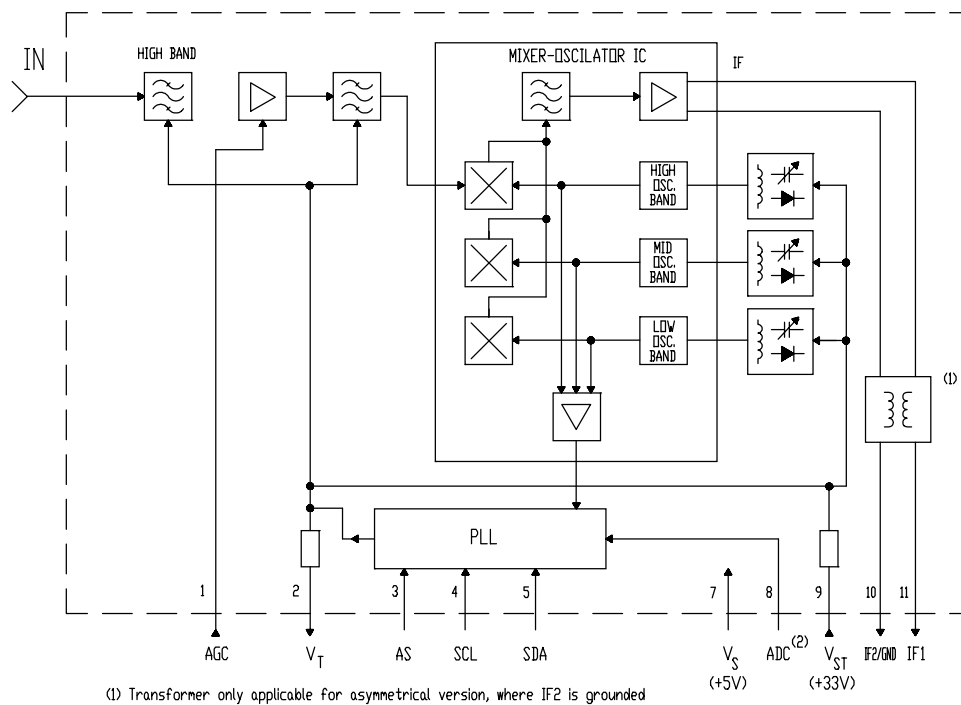


Fig.1 Electrical block diagram

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## PINNING

SYMBOL	PIN	DESCRIPTION
AGC	1	gain control voltage
$V_T$	2	tuning voltage
AS	3	I <sup>2</sup> C-bus address select
SCL	4	I <sup>2</sup> C-bus serial clock
SDA	5	I <sup>2</sup> C-bus serial data
n.c.	6	not connected
$V_S$	7	PLL supply voltage +5 V
ADC	8	ADC input
$V_{ST}$	9	tuning supply voltage +33 V
IF2/GND	10	KS-D-134: symmetrical IF output; KS-D-134A: ground
IF1	11	KS-D-134: symmetrical IF output; KS-D-134A: asymmetrical IF output
GND	MT1, MT2	mounting tags (ground)
IN		aerial input connector IEC (14.5 mm)

## LIMITING VALUES

## Environmental conditions

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
<b>Non-operational conditions</b>				
$T_{amb}$	ambient temperature	-40	+60	°C
RH	relative humidity	-	100	%
<b>Operational conditions</b>				
$T_{amb}$	ambient temperature	-15	+60	°C
RH	relative humidity	-	93	%

## Limiting values under operational conditions

The tuner can be guaranteed to function properly under the following conditions

SYMBOL	PARAMETER	PIN	MIN.	TYP.	MAX.	UNIT
$V_S$	supply voltage	7	4.75	5.00	5.5	V
$I_S$	supply current		-	-	130	mA
$V_{ST}$	supply voltage	9	30	33	35	V
$I_{ST}$	supply current		-	-	1.7	mA
$V_{AGC}$	AGC input voltage	1	-	4.0	4.5	V
$\Delta V_{AGC}$	AGC input voltage range		0.3	-	4.0	V
$I_{AGC}$	AGC input current		-	-	20	µA
$V_{AS}$	address select input voltage	3	-	-	5.5	V
$V_{SCL}$	serial clock input voltage	4	-	-	5.5	V
$V_{SDA}$	serial data input voltage	5	-	-	5.5	V
$I_{SDA}$	serial data input current		-1	-	5	mA

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## ELECTRICAL DATA

## Conditional data

Unless otherwise specified, all electrical values for Chapter "Electrical data" apply at the following conditions and the electrical performance is related both to systems B, G, H and D, K.

A proper function is guaranteed within the specified operational conditions but a certain deterioration of performance parameters may occur at the limits of operational conditions.

SYMBOL	PARAMETER	VALUE	UNIT
T <sub>amb</sub>	ambient temperature	25 +/- 5	°C
RH	relative humidity	60 +/- 15	%
V <sub>S</sub>	supply voltage	5.0 +/- 0.1	V
V <sub>AGC</sub>	AGC input voltage	4.0 +/- 0.1	V
V <sub>ST</sub>	tuning supply voltage	33 +/- 0.5	V
t <sub>pr</sub>	pre-heating time (+5 V at pin 7)	10	minute
Z <sub>S(AE)</sub>	aerial source impedance (unbalanced)	75	Ω

## Aerial input characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VSWR	reflection coefficient	referred to 75 Ω impedance	-	2	4	
V <sub>ant</sub>	antenna connection disturbance voltage	< 1.75 GHz; comply to "EN55013 section 3.3"	-	-	46	dBμV

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## General characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
$f_b$	frequency range:		471.25	-	855.25	MHz
$G_V$	voltage gain: all channels gain taper	The IF output is loaded with a test circuit according diagram fig.2	40 -	45 -	52 7	dB dB
F	noise:	The IF output is loaded with a test circuit according diagram fig.3	-	6.0	8	dB
$\Delta V_{AGC}$	AGC input voltage range:		40	50	-	dB
$\alpha_i$	image rejection:		50	60	-	dB
$\alpha_{IF}$	IF rejection (picture):		65	71	-	dB
$V_{ESD}$	electrostatic discharge (ESD):  protection on pins 1 to 5 and 6 to 11 protection on antenna socket	note 1	 2 8	 - -	 - -	 kV kV
	oscillator characteristics:  oscillator tuning resolution lock-in time		 - -	 - -	 note 2 150	 kHz msec

## Notes

1. The tuner meets specifications IEC 1000-4-2 level 1 for pins and level 4 for antenna socket.
2. Resolution 31.25 kHz, 50.00 kHz or 62.5 kHz (see Table "Ratio select bits").

## Visibility test

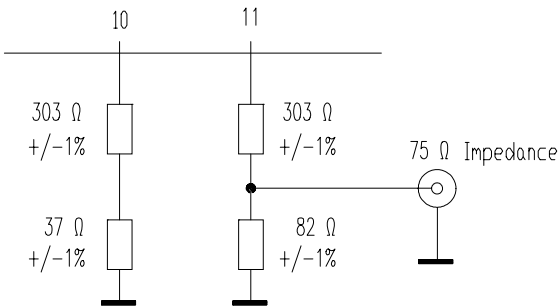
The tuners meet the requirements of the European norm "EN55020", when measured in an adequate television receiver.

## Recommended adjustment of Tuner AGC in TV chassis:

Channel: E21 (471.25 MHz PC-frequency)  
 Input level: 70 dB $\mu$ V/75  $\Omega$   
 IF output level: 105 dB $\mu$ V  
 Gain reduction: 10 dB  
 AGC-Voltage: 2.6 V +/-0.2V

## Radiation

The tuners meet the requirements of the European norm "EN55013" and "CISPR13" (1990), when measured in an adequate television receiver.



test circuit attenuation : 26 dB

Fig. 2 Test circuit for voltage gain.

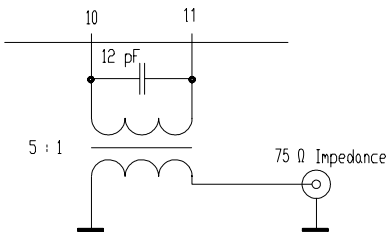


Fig. 3 Test circuit for noise figure.

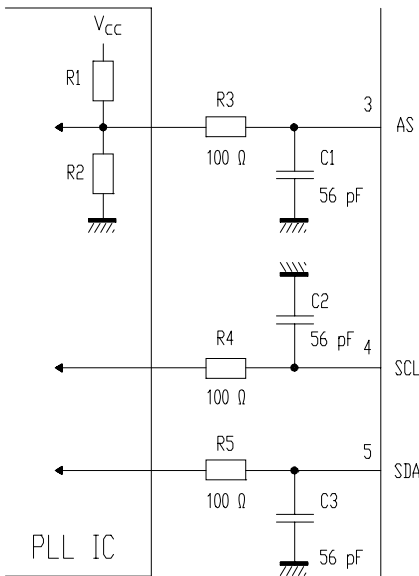


Fig.4 I²C-bus load.

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## APPLICATION INFORMATION

## WRITE mode

BYTE	BITS								
	7 <sup>(1)</sup> MSB	6	5	4	3	2	1	0 LSB	A <sup>(2)</sup>
Address byte	1	1	0	0	0	MA1	MA2	RW <sup>(3)</sup>	A
Program divider byte 1	0	n14	n13	n12	n11	n10	n9	n8	A
Program divider byte 2	n7	n6	n5	n4	n3	n2	n1	n0	A
Control information byte1	1	CP	T2	T1	T0	RSA	RSB	0	A
Control information byte 2	X	X	X	X	X	1	0	0	A

## Notes

1. X = don't care.
2. A = Acknowledge.
3. R/W bit = 0 for WRITE mode, R/W bit = 1 for READ mode.

## Address selection

$V_s = \pm 5\text{ V}$  (PLL supply voltage).

MA1	MA0	ADDRESS	VOLTAGE AT PIN 3
0	0	C0	GND to $0.1XV_s$
0	1	C2	OPEN or $0.2XV_s$ to $0.3XV_s$
1	0	C4	$0.4XV_s$ to $0.7XV_s$
1	1	C6	$0.8XV_s$ to $1.1XV_s$

## Programmable divider settings (bytes 1 and 2)

Divider ratio:

$$N = R \times \{ f_{RF,pc} + f_{IF,pc} \},$$

R = 16 with reference divider = 512

R = 20 with reference divider = 640

R = 32 with reference divider = 1024

$$N = (16384 \times n_{14}) + (8192 \times n_{13}) + (4096 \times n_{12}) + (2048 \times n_{11}) + (1024 \times n_{10}) + (512 \times n_9) + (256 \times n_8) + (128 \times n_7) + (64 \times n_6) + (32 \times n_5) + (16 \times n_4) + (8 \times n_3) + (4 \times n_2) + (2 \times n_1) + n_0$$

## Control byte 1

CP can be set to either 0 (low current) or 1 (high current).

Charge pump settings:

CP = 1, for fast tuning

CP = 0, for moderate speed tuning with slightly better residual oscillator FM.

Unnecessary charge pump action will result in very low tuning voltage ( $V_T=0V$ ) which may drive the oscillator to extreme conditions.

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## Test mode setting bits

T2	T1	T0	Setting
0	0	0	normal operation with automatic charge pump switch OFF
0	0	1	normal operation with automatic charge pump switch ON <sup>(1)</sup>
0	1	X	charge pump OFF
1	1	0	charge pump ON; sinking current
1	1	1	charge pump ON; sourcing current
1	0	0	internal test mode
1	0	1	internal test mode

## Note

1. This function automatically switches the CP to HIGH at a new tuning action and forces CP to LOW when the PLL is locked.

## Ratio select bits

RSA	RSB	REFERENCE DIVIDER	STEP SIZE (kHz)
X	0	640	50.00
0	1	1024	31.25
1	1	512	62.50

## READ mode

BYTE	BITS								A <sup>(1)</sup>
	7 MSB	6	5	4	3	2	1	0 LSB	
Address byte	1	1	0	0	0	MA1	MA0	1	A
Status byte	POR <sup>(2)</sup>	FL <sup>(3)</sup>	ACPS <sup>(4)</sup>	X	X	A2 <sup>(5)</sup>	A1 <sup>(5)</sup>	A0 <sup>(5)</sup>	A

## Notes

1. A = Acknowledge.
2. POR = Power On Reset flag (POR=1 at power on).
3. FL = In-lock flag (FL=1 at loop is phase-locked).
4. ACPS = Automatic Charge Pump Switch flag, active ACPS=0, non active ACPS=1.
5. A2, A1, and A0 are the digital outputs of the 5 level ADC.

## ADC byte

VOLTAGE AT PIN 8	A2	A1	A0
0.60XV <sub>S</sub> to V <sub>S</sub>	1	0	0
0.45XV <sub>S</sub> to 0.60XV <sub>S</sub>	0	1	1
0.30XV <sub>S</sub> to 0.45XV <sub>S</sub>	0	1	0
0.15XV <sub>S</sub> to 0.30XV <sub>S</sub>	0	0	1
0 to 0.15XV <sub>S</sub>	0	0	0



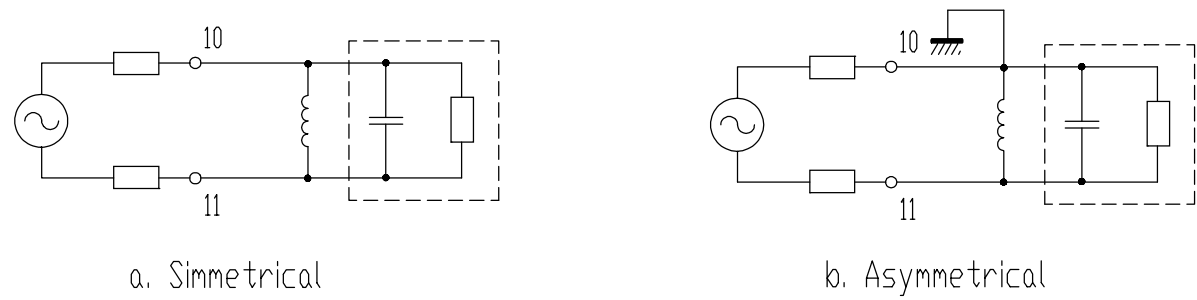


Fig.5 IF loading using SAW filters.

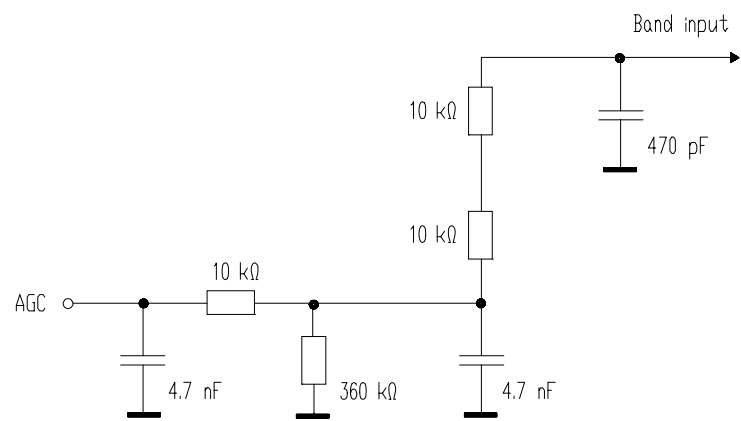


Fig.6 Internal AGC circuit.

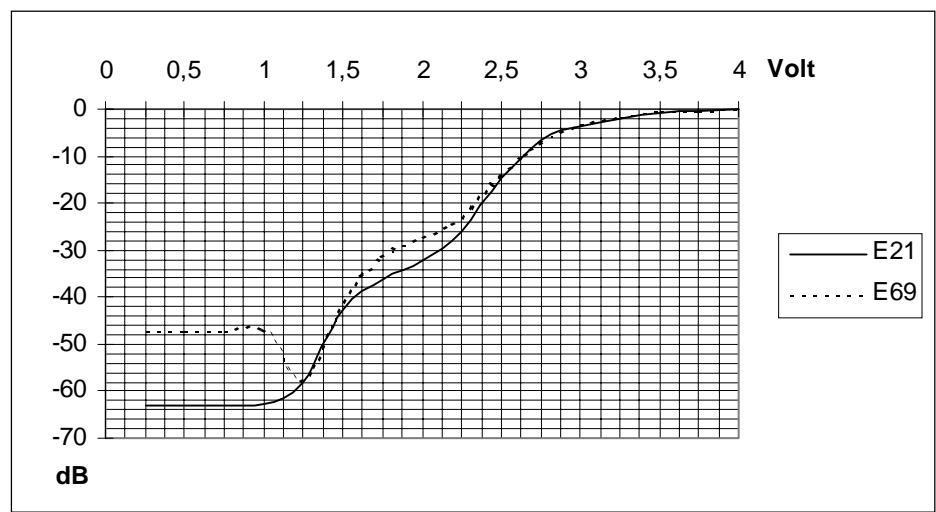


Fig.7 AGC characteristics.

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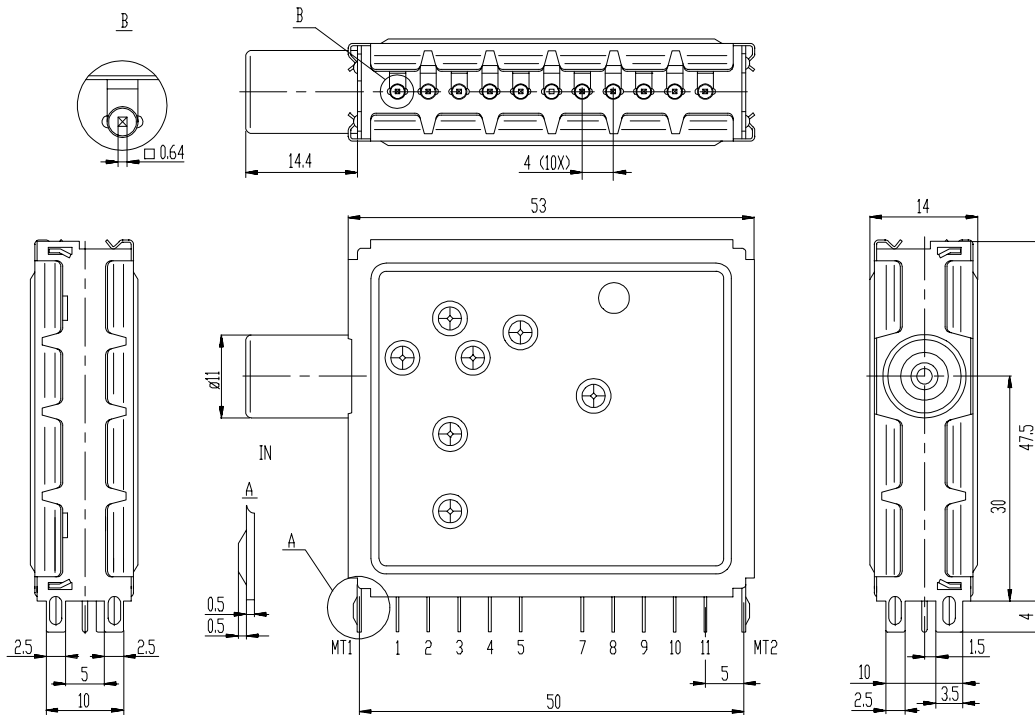


Fig.8 Mechanical outline

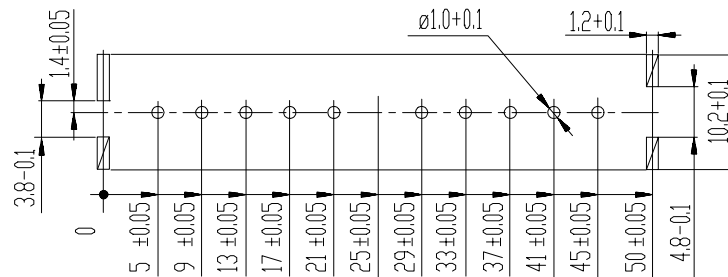


Fig.9 Punching pattern seen from solder side

**Aerial connections**

Standard IEC socket female 75 Ω.

**LIFE SUPPORT APPLICATIONS**

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Selteka customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Selteka for any damages resulting from such improper use or sale.