

Hyperband television tuner

KS-H-132

FEATURES

- Member of the KS-H-130 family small sized VHF/Hyperband/UHF tuner
- Systems CCIR: B/G, H; OIRT: D/K
- Digitally controlled (PLL) tuning via I²C-bus
- Off-air channels, S-cable channels and Hyperband
- World standardized mechanical dimensions and world standard pinning
- Compact size
- Comply to "CENELEC EN55020" and "EN55013"

MARKING

The following items of information are printed on a sticker that is on the top cover of the tuner or printed directly on the top cover:

- Company logo
- Type number
- Year and month code
- Quality inspection print

DESCRIPTION

The KS-H-132 tuner belongs to the KS-H-130 family of tuners, which are designed to meet a wide range of applications. It is a combined VHF/Hyperband/UHF tuner suitable for CCIR systems B/G, H, or OIRT systems D/K. The low IF output impedance has been designed for direct drive of a wide variety of SAW filters with sufficient suppression of triple transient.

The tuners comply with the requirements of radiation, signal handling capability and immunity conforming with:

- CISPR 13 (1990) include. amendment 1 (1992) and amendment 2 (1993)
- European standards CENELEC EN55013, EN55020

ORDERING INFORMATION

TYPE	SYSTEM	DESCRIPTION
KS-H-132 E	CCIR	symmetrical IF output; IEC connector (14.5 mm), I ² C status byte
KS-H-132 O	OIRT	symmetrical IF output; IEC connector (14.5 mm), I ² C status byte

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INTERMEDIATE FREQUENCIES

SIGNAL	FREQUENCY (MHz)	
	SYSTEM B/G, H	SYSTEM D/K
Picture carrier	38.90	38.00
Colour	34.47	33.594, 33.75
Sound	33.40	31.5

Note

1.The oscillator frequency is above the input signal frequency.

CHANNEL COVERAGE

BAND	OFF-AIR CHANNELS		CABLE CHANNELS	
	CHANNELS	FREQUENCY RANGE (MHz)	CHANNELS	FREQUENCY RANGE (MHz)
Low band	E2 to C	48.25 to 82.25 ⁽¹⁾	S01 to S10	69.25 to 168.25
Mid band	E5 to E12	175.25 to 224.25	S11 to S41	231.25 to 463.25
High band	E21 to E69	471.25 to 855.25 ⁽²⁾		

Notes

- 1.Enough margin is available to tune down to 45.25 MHz.
- 2.Enough margin is available to tune up to 863.25 MHz.

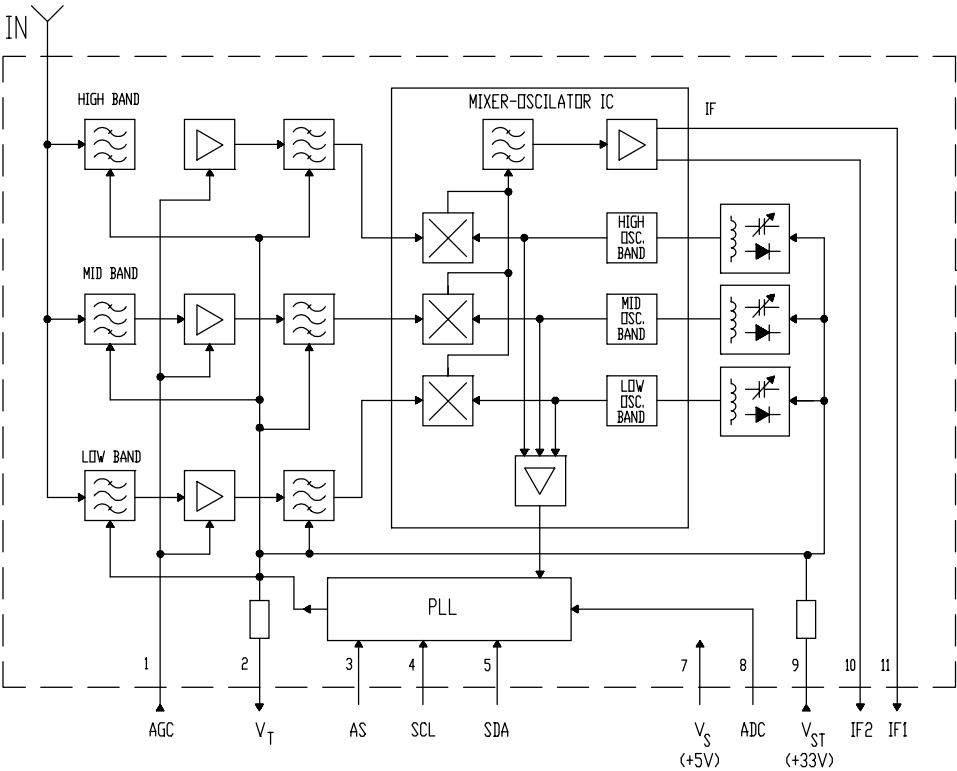


Fig.1 Electrical block diagram

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PINNING

SYMBOL	PIN	DESCRIPTION
AGC	1	gain control voltage
V _T	2	tuning voltage
AS	3	I ² C-bus address select
SCL	4	I ² C-bus serial clock
SDA	5	I ² C-bus serial data
n.c.	6	not connected
V _S	7	PLL supply voltage +5 V
ADC	8	ADC input
V _{ST}	9	tuning supply voltage +33 V
IF2	10	symmetrical IF output
IF1	11	symmetrical IF output
GND	MT1, MT2	mounting tags (ground)
IN		aerial input connector IEC (14.5 mm)

LIMITING VALUES

Environmental conditions

SYMBOL	PARAMETER	MIN.	MAX.	UNIT
Non-operational conditions				
T _{amb}	ambient temperature	-40	+60	°C
RH	relative humidity	-	100	%
Operational conditions				
T _{amb}	ambient temperature	-15	+60	°C
RH	relative humidity	-	93	%

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Limiting values under operational conditions

The tuner can be guaranteed to function properly under the following conditions

SYMBOL	PARAMETER	PIN	MIN.	TYP.	MAX.	UNIT
V_S	supply voltage	7	4.75	5.00	5.5	V
I_S	supply current		-	-	130	mA
V_{ST}	supply voltage	9	30	33	35	V
I_{ST}	supply current		-	-	1.7	mA
V_{AGC}	AGC input voltage	1	-	4.0	4.5	V
ΔV_{AGC}	AGC input voltage range		0.3	-	4.0	V
I_{AGC}	AGC input current		-	-	20	μ A
V_{AS}	address select input voltage	3	-	-	5.5	V
V_{SCL}	serial clock input voltage	4	-	-	5.5	V
V_{SDA}	serial data input voltage	5	-	-	5.5	V
I_{SDA}	serial data input current		-1	-	5	mA

ELECTRICAL DATA

Conditional data

Unless otherwise specified, all electrical values for Chapter "Electrical data" apply at the following conditions and the electrical performance is related both to systems B, G, H and D, K.

A proper function is guaranteed within the specified operational conditions but a certain deterioration of performance parameters may occur at the limits of operational conditions.

SYMBOL	PARAMETER	VALUE	UNIT
T_{amb}	ambient temperature	25 +/- 5	$^{\circ}$ C
RH	relative humidity	60 +/- 15	%
V_S	supply voltage	5.0 +/- 0.1	V
V_{AGC}	AGC input voltage	4.0 +/- 0.1	V
V_{ST}	tuning supply voltage	33 +/- 0.5	V
t_{pr}	pre-heating time (+5 V at pin 7)	10	minute
$Z_{S(AE)}$	aerial source impedance (unbalanced)	75	Ω

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Aerial input characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
VSWR	reflection coefficient	referred to 75 Ω impedance	-	2	4	
V _{ant}	antenna connection disturbance voltage	< 1.75 GHz; comply to "EN55013 section 3.3"	-	-	46	dB μ V

General characteristics

SYMBOL	PARAMETER	CONDITIONS	MIN.	TYP.	MAX.	UNIT
f _p	frequency range:					
	low band		48.25	-	168.25	MHz
	mid band		175.25	-	463.25	MHz
	high band		471.25	-	855.25	MHz
G _v	voltage gain:	The IF output is loaded with a test circuit according diagram fig.2				
	all channels		40	45	52	dB
	gain taper		-	-	7	dB
F	noise:	The IF output is loaded with a test circuit according diagram fig.3				
	low band		-	6.0	9	dB
	mid band		-	6.0	9	dB
	high band		-	6.0	8	dB
ΔV_{AGC}	AGC input voltage range:					
	low and mid band		45	60	-	dB
	high band		40	50	-	dB
α_i	image rejection:					
	low band		66	70	-	dB
	mid band		60	69	-	dB
	high band		50	60	-	dB
α_{IF}	IF rejection (picture):					
	channel E2		55	68	-	dB
	low, mid and high bands		65	71	-	dB
V _{ESD}	electrostatic discharge (ESD):	note 1				
	protection on pins 1 to 5 and 6 to 11		2	-	-	kV
	protection on antenna socket		8	-	-	kV
	oscillator characteristics:					
	oscillator tuning resolution		-	-	note 2	kHz
	lock-in time		-	-	150	msec

Notes

1. The tuner meets specifications IEC 1000-4-2 level 1 for pins and level 4 for antenna socket.
2. Resolution 31.25 kHz, 50.00 kHz or 62.5 kHz (see Table "Ratio select bits").

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Visibility test

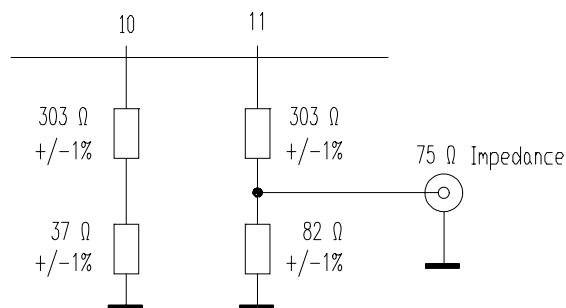
The tuners meet the requirements of the European norm "EN55020", when measured in an adequate television receiver.

Recommended adjustment of Tuner AGC in TV chassis:

Channel: E21 (471.25 MHz PC-frequency)
 Input level: 70 dB μ V/75 Ω
 IF output level: 105 dB μ V
 Gain reduction: 10 dB
 AGC-Voltage: 2.6 V \pm 0.2V

Radiation

The tuners meet the requirements of the European norm "EN55013" and "CISPR13" (1990), when measured in an adequate television receiver.



test circuit attenuation : 26 dB

Fig. 2 Test circuit for voltage gain.

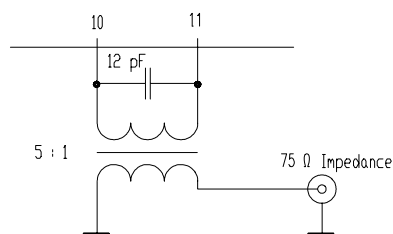


Fig. 3 Test circuit for noise figure.

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APPLICATION INFORMATION

WRITE mode

BYTE	BITS								
	7 ⁽¹⁾ MSB	6	5	4	3	2	1	0 LSB	A ⁽²⁾
Address byte	1	1	0	0	0	MA1	MA2	RW ⁽³⁾	A
Program divider byte 1	0	n14	n13	n12	n11	n10	n9	n8	A
Program divider byte 2	n7	n6	n5	n4	n3	n2	n1	n0	A
Control information byte1	1	CP	0	0	1	RSA	RSB	0	A
Control information byte 2	P7	P6	P5	P4	X	P2	P1	P0	A

Notes

1. X = don't care.
2. A = Acknowledge.
3. R/W bit = 0 for WRITE mode, R/W bit = 1 for READ mode.

Address selection

$V_s = \pm 5$ V (PLL supply voltage).

MA1	MA0	ADDRESS	VOLTAGE AT PIN 3
0	0	C0	GND to $0.1XV_s$
0	1	C2	OPEN or $0.2XV_s$ to $0.3XV_s$
1	0	C4	$0.4XV_s$ to $0.7XV_s$
1	1	C6	$0.8XV_s$ to $1.1XV_s$

Programmable divider settings (bytes 1 and 2)

Divider ratio:

$$N = R \times \{ f_{RF,pc} + f_{IF,pc} \},$$

R = 16 with reference divider = 512

R = 20 with reference divider = 640

R = 32 with reference divider = 1024

$$N = (16384 \times n_{14}) + (8192 \times n_{13}) + (4096 \times n_{12}) + (2048 \times n_{11}) + (1024 \times n_{10}) + (512 \times n_9) + (256 \times n_8) + (128 \times n_7) + (64 \times n_6) + (32 \times n_5) + (16 \times n_4) + (8 \times n_3) + (4 \times n_2) + (2 \times n_1) + n_0$$

Control byte 1

CP can be set to either 0 (low current) or 1 (high current).

Charge pump settings:

CP = 1, for fast tuning

CP = 0, for moderate speed tuning with slightly better residual oscillator FM.

Unnecessary charge pump action will result in very low tuning voltage ($V_T=0V$) which may drive the oscillator to extreme conditions.

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Ratio select bits

RSA	RSB	REFERENCE DIVIDER	STEP SIZE (kHz)
X	0	640	50.00
0	1	1024	31.25
1	1	512	62.50

Band switching (Control byte 2)

BIT								ACTIVE PORT	BAND
P7 MSB	P6	P5	P4	P3	P2	P1	P0 LSB		
X	X	X	X	X	0	1	0	P1	Low band
X	X	X	X	X	1	0	0	P2	Mid band
X	X	X	X	X	0	0	1	P0	High band

READ mode

BYTE	BITS								
	7 MSB	6	5	4	3	2	1	0 LSB	A ⁽¹⁾
Address byte	1	1	0	0	0	MA1	MA0	1	A
Status byte	POR ⁽²⁾	FL ⁽³⁾	X	X	X	A2 ⁽⁴⁾	A1 ⁽⁴⁾	A0 ⁽⁴⁾	A

Notes

1. A = Acknowledge.
2. POR = Power On Reset flag (POR=1 at power on).
3. FL = In-lock flag (FL=1 at loop is phase-locked).
4. A2, A1, and A0 are the digital outputs of the 5 level ADC.

ADC byte

VOLTAGE AT PIN 8	A2	A1	A0
$0.60XV_S$ to V_S	1	0	0
$0.45XV_S$ to $0.60XV_S$	0	1	1
$0.30XV_S$ to $0.45XV_S$	0	1	0
$0.15XV_S$ to $0.30XV_S$	0	0	1
0 to $0.15XV_S$	0	0	0

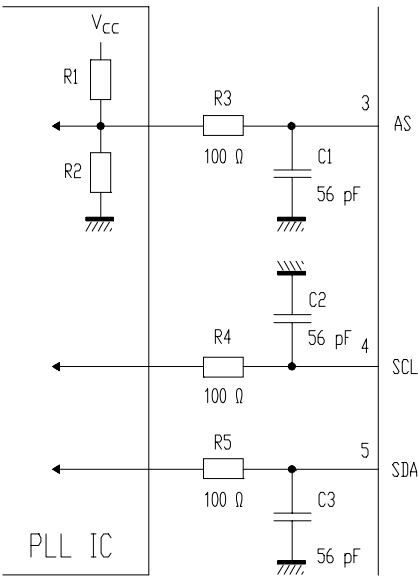


Fig.4 I²C-bus load.

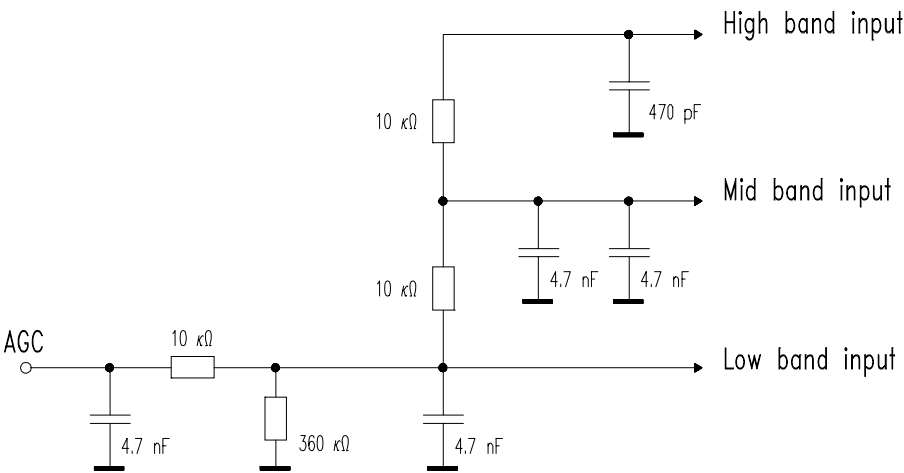


Fig.5 Internal AGC circuit.

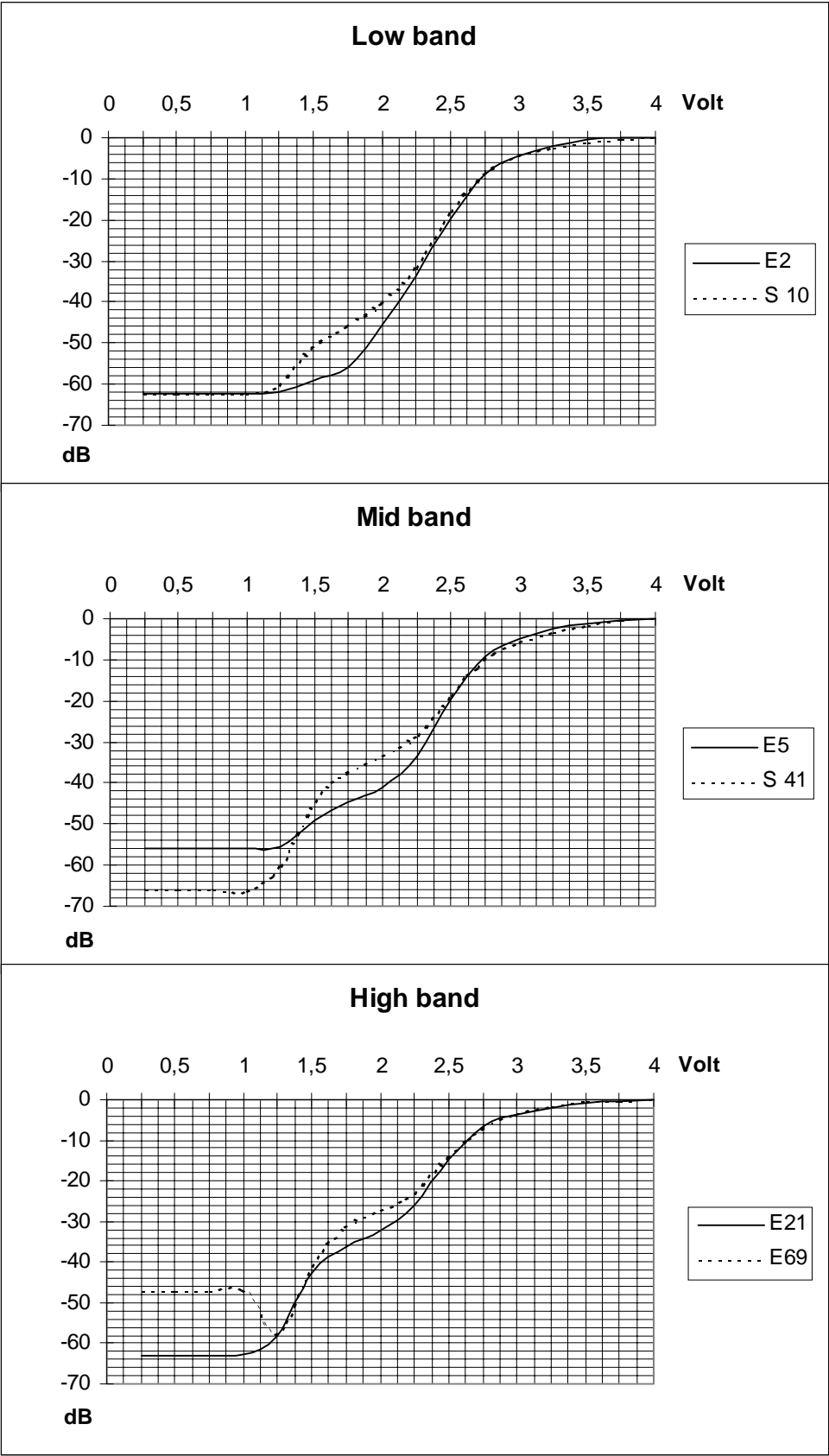


Fig.6 AGC characteristics.

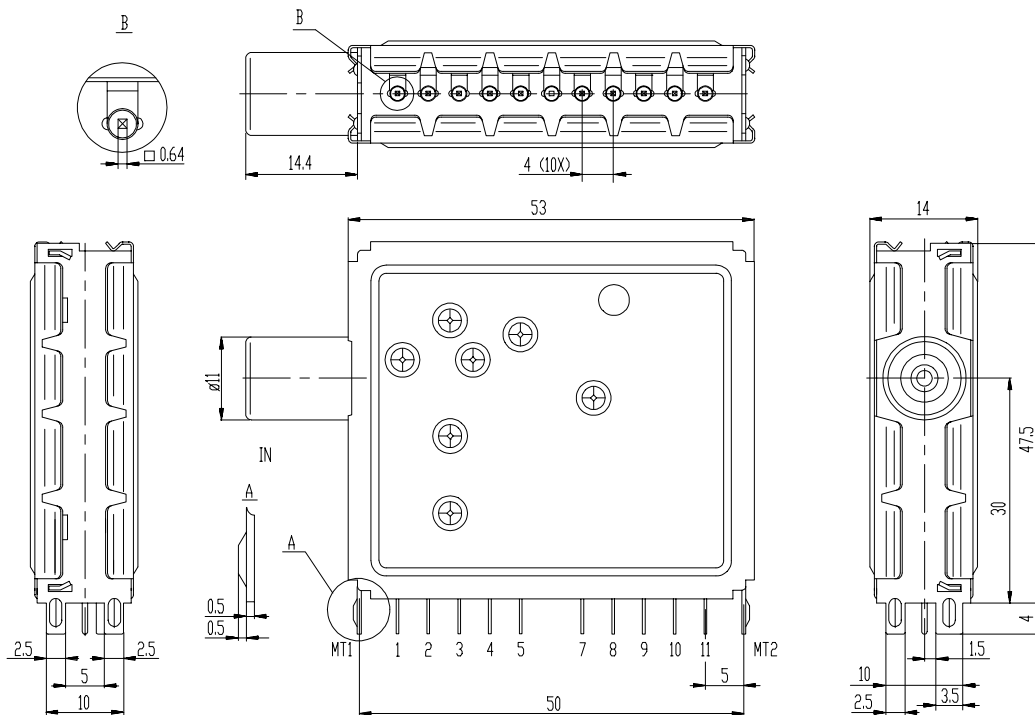


Fig.7 Mechanical outline

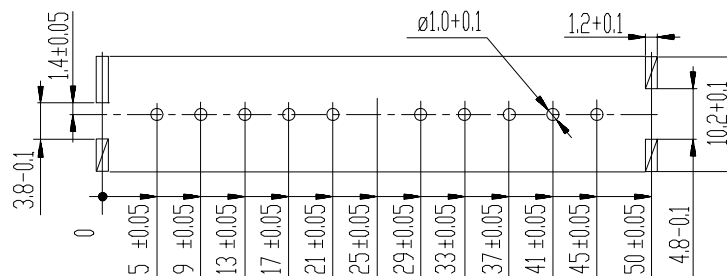


Fig.8 Punching pattern seen from solder side

Aerial connections

Standard IEC socket female 75 Ω .

LIFE SUPPORT APPLICATIONS

These products are not designed for use in life support appliances, devices, or systems where malfunction of these products can reasonably be expected to result in personal injury. Selteka customers using or selling these products for use in such applications do so at their own risk and agree to fully indemnify Selteka for any damages resulting from such improper use or sale.