EDITED BY BILL TRAVIS & ANNE WATSON SWAGER

Boost converter generates three analog rails

TIM HERKLOTS, MAXIM INTEGRATED PRODUCTS LTD, THEALE, BERKSHIRE, UK

The standard boost converter in **Figure 1** uses not only IC_1, C_1, L_1, D_1, and C_2 to generate a main 5V output, but also additional small, low-cost components to provide two auxiliary supply rails of 10 and –5V. These auxiliary outputs are useful for analog circuitry in small handheld instruments, which often require supply voltages greater than the signal range. Input voltages of 0.8 to 5.5V, which is equivalent to voltages from a battery pack of one to three cells, sustain the main regulated output of 5V±2%. With an input of 1.8V from two flat cells, for instance, and with the other rails unloaded, the circuit can produce 25 mA with 80 to 90% efficiency.

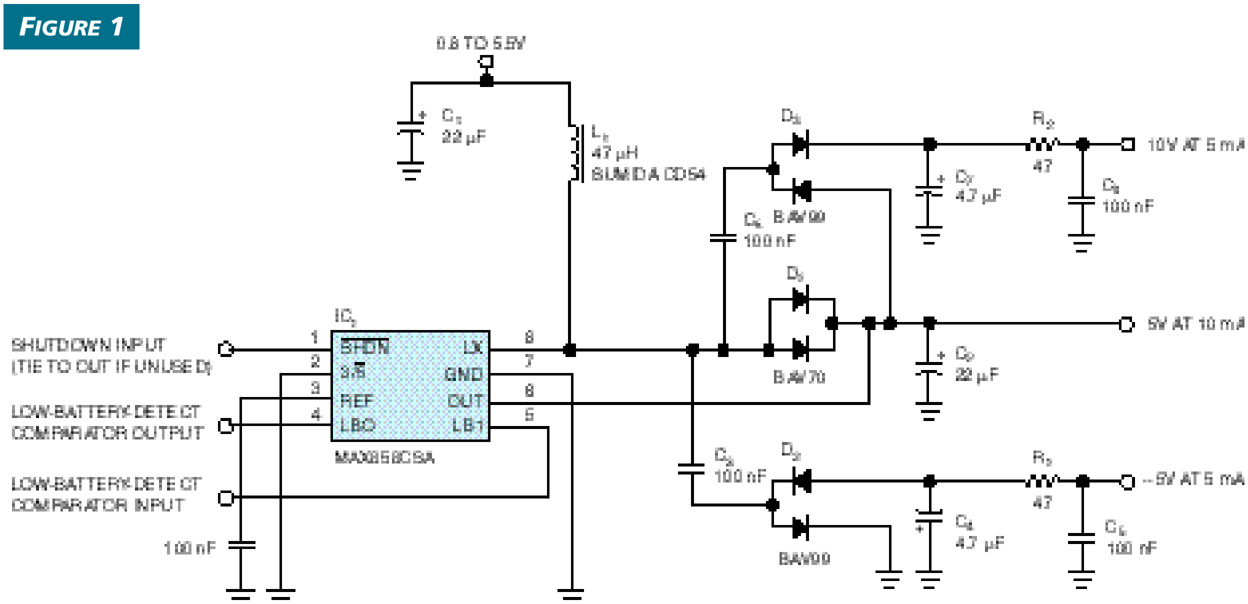
The converter's LX switching node drives low-cost, discrete charge pumps via "flying capacitors" C_3 and C_6 to create the –5V and 10V outputs. The LX node switches between 0V and a level-one diode drop above the 5V rail, so the charge pumps' drive voltage is reasonably well-regulated. Moreover, the drop across D_1 roughly compensates for diode drops in the two charge-pump outputs. IC_1's internal control scheme also assists in regulating the auxiliary outputs. This IC's current-limited, minimum-off-time, pulse-frequency modulation constantly adapts its switching frequency to the net load current; the frequency increases when the load increases, producing a greater transfer of energy via the flying capacitors. The result is a type of pseudoregulation for the charge-pump outputs.

These analog supply rails can drive precision op amps, such as the MAX400 and OP-07, whose input common-mode-rejection and output-range specifications are 2 to 3V within the supply rails. Thus, the rails are good enough if the –5V output is less than –3V and the 10V output is more than 8V. Accordingly, the component choices in **Figure 1**, such as the lossy RC output filters and silicon signal diodes in place of Schottky diodes, provide for minimal cost and ripple rather than maximum regulation. The 4.7-μF capacitors, C_4 and C_7, can be high-ESR, commodity, multilayer-ceramic types with 16V ratings, a 1206 case, and a Y5V dielectric, such as the 1206YG475ZAT2A from AVX Corp (www.avxcorp.com).

The output ripple varies with the supply voltage and output load. Operating with an input voltage of 1.8V, the circuit produces ripple amplitudes over the load of 2 to 10 mV p-p for the 10V rail and 15 to 30 mV p-p for the –5V rail. By increasing C_5 and C_8 to 2.2 μF, you can reduce these ripple levels to 1 and 5 mV, respectively.

With no load on the auxiliary rails, the 5V output's maximum available load current rises with input supply voltage (**Figure 2a**). You can increase this available output power by replacing D_1 with a lower loss Schottky diode. At an input of 1.8V, the output power available for the three rails (loaded with 10 mA at 5V, 5 mA at 10V, and 5 mA at –5V) is somewhat less than 125 mA; with a 5-mA load, the 10V and –5V outputs are approximately 9.75 and –3.7V, respectively (**Figure 2b**). A 2.7V input based on three flat cells yields

FIGURE 1



Adding external charge pumps to this 5V boost converter produces auxiliary analog rails of 10 and –5V.

around 275 mW.

The MAX858 operates with peak inductor currents of 125 mA. If you need more current, you can replace this IC with related parts that have 500 mA and 1A ratings. Note that these changes require different passive components; the inductor and main output diode ratings must match the inductor's peak current. The charge pumps can remain the same if their output currents don't change much.

You can also retain the cheap, common, commodity dual diodes D_1, D_2, and D_3, but detail specifications vary, so look carefully at data sheets for the part you actually use. For example, the BAV70's dc forward current, I_F, and peak forward surge current, I_{FSM} for 1 µsec, differ among manufacturers. For the Motorola (www.motorola.com) part, I_F=200 mA, and I_{FSM}=500 mA. For National Semiconductor (www.national.com), I_F=600 mA, and I_{FSM}=2A. For Philips (www.philips.com), I_F=125 mA, and I_{FSM}=4A, and for Vishay-Siliconix (www.siliconix.com), I_F=250 mA, and I_{FSM}=4.5A. This caution is advisable in all second-source considerations. (DI #2200) EDN

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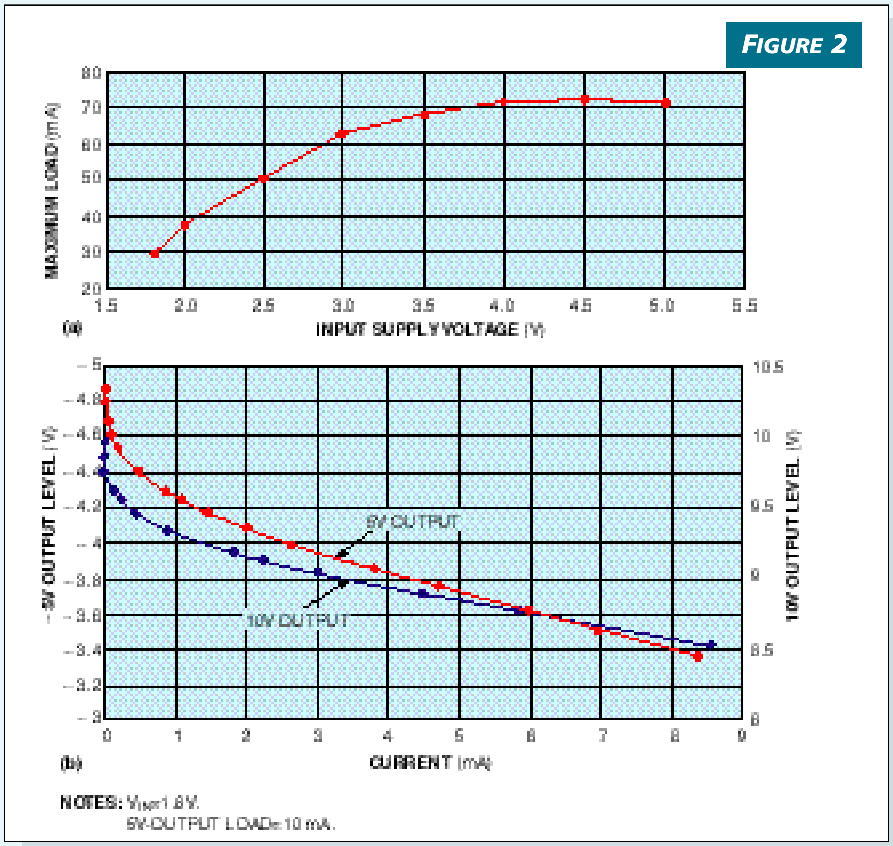


With auxiliary rails unloaded, the 5V output's maximum available load current rises with input supply voltage (a). The auxiliary-output voltage levels depend on the load current (b).

Automatic-exposure scheme uses CCD shutter

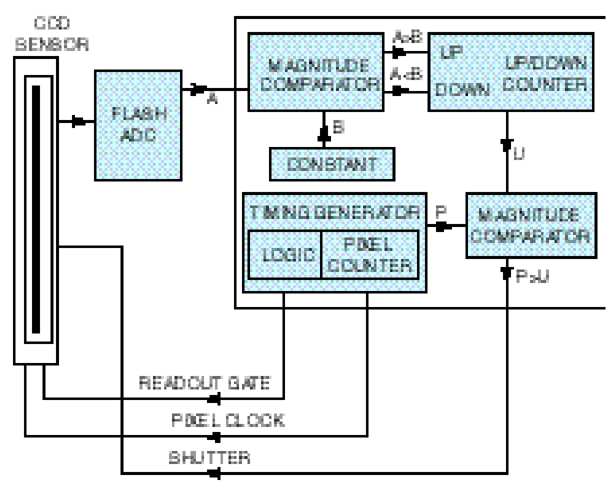
GIOVANNI ROMEO AND SANDRO RAO, ISTITUTO NAZIONALE DI GEOFISICA, ROME, ITALY

This application follows the Design Idea, "Peak detector maximizes CCD-sensor range" (*EDN*, Aug 15, 1996). Its aim was to optimize the performance of an A/D converter used to digitize a linear CCD sensor's analog output. The method involved stretching the upper reference of the flash ADC for the highest lit pixel in the array. The method works well, but does not obtain the best performance from the CCD, which can saturate for overexposure or can produce noise for underexposure. **Figure 1** shows a better method that you can use with CCD sensors that provide a shutter facility. The shutter signal in a modern CCD array (such as the Sony ILX703A) removes the electrical charges the light produces during the exposure. Thus, the time between the shutter signal and the data reading is the exposure time. The circuit in **Figure 1** simply moves the shutter pulse between two subsequent readout gates.

The circuit digitally compares the ADC's output with the desired level (near the maximum ADC output). If the output exceeds the threshold level, the up/down counter increments; otherwise, it decrements. The magnitude comparator compares the up/down counter's register contents with the pixel-counter data, and, when the data exceeds the contents, the shutter signal activates. The system requires an average settling time of (number of pixels)/(2×pixel time) and, in the steady-state condition, oscillates with a period of one pixel time. Our application required obtaining the shape of the light distribution, neglecting the absolute illumination information. You can use the contents of the up/down counter's register as a scale factor, when you need to measure the absolute illumination.

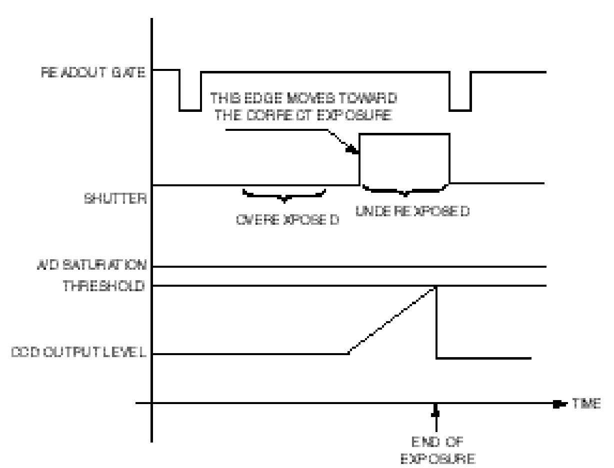
Figure 2 shows the waveforms in the system. A 1016 PLD generates the signals to control the system and the CCD. **Listing 1** gives the Abel program for the 1016. You can download the file from *EDN*'s Web site www.ednmag.com. At the registered-user area, go into the Software Center to download the files from DI-SIG, #2213. You can better understand the CCD's operation by referring to Sony's 1992 application note, "Linear Sensor Application Note." (DI #2213)

FIGURE 1



To adjust the automatic-exposure system, set constant B near the maximum ADC level, tuned to match the maximum unsaturated CCD output.

FIGURE 2



The shutter signal keeps the sensor empty after asserting the readout gate. The exposure begins just in time to keep the CCD's output at a level that uses the ADC's entire dynamic range.

ABEL PROGRAM FOR AUTOMATIC-EXPOSURE PLD

```
MODULE ccd

TITLE ' ccd, timing and shutter generator '
shutter INTERFACE (clk,p11..p0,ud11..ud0,ff -> sh);
   shut  FUNCTIONAL_BLOCK shutter;

clk                         pin;
[AD9..AD0]                  pin;  //comparator input
[CK1..CK0]                  pin       istype 'reg,buffer';  //frequency
divider.
[P11..P0]                   node      istype 'reg,buffer';  // pixel counter
[UD11..UD0]                 node      istype 'reg,buffer';  // UP/DOWN
counter
ROG                         pin;         //rog pulse
CCDCLOCK, ADCLOCK           pin       istype 'buffer';      // ccd and AD
clock
OUT                         node;                          // UP/DOWN
selection
FF                          node istype 'reg_D';   //peak detector FF
SHU                         pin; shutter signal

"Sets
Input  = [AD9..AD0];
Count1 = [P11..P0];
Count2 = [UD11..UD0];

Equations
shut.clk = clk;
SHU = shut.sh;
shut.[p11..p0] = [P11..P0];
shut.[ud11..ud0] = [UD11..UD0];
shut.ff = FF;
FF.D = OUT;
FF.clk = ROG;
FF.AP  = OUT;
[CK1..CK0].clk = clk;
Count1.clk  = CK1;
Count2.clk = !ROG;
[CK1..CK0] := [CK1..CK0] + 1;

when (Count1 == 2169) then Count1 := 0 else Count1 := Count1 + 1;
when ((Count1 > 2085) & (Count1 < 2168)) then ADCLOCK = 0 else ADCLOCK =
!CK1;
when (Count1 < 2086) then CCDCLOCK = CK1 else CCDCLOCK = 0;
ROG = (Count1 < 2137) # (Count1 >= 2147);

when (Input>= [1,1,1,1,1,1,0,1,0,0,1]) then OUT = 1 else OUT = 0;
when (FF== 1) then {
        when (Count2<2047 ) then Count2 := Count2 + 1 else Count2 := 2047;
}

                else {
        when (Count2>0)     then Count2 := Count2 - 1 else Count2 := 0; }


End




MODULE shutter

TITLE 'shutter'
clk                         pin;
[p11..p0]                   pin;
[ub11..ub0]                 pin;  //UP/DOWN counter
ff                          pin;
sh                          pin  istype 'reg'; //shutter
SHU0,SHU1,SHU2,SHU3         node;

EQUATIONS
sh.clk = clk;
SHU0 = [p11..p7] > [uB11..uB7];
SHU1 = [p11..p7] == [uB11..uB7];
SHU2 = [p7..p0] > [uB7..uB0];
SHU3 = (ff==0)&([uB11..uB0]==0);
sh    := SHU0 # (SHU1 & SHU2) # SHU3);

END
```

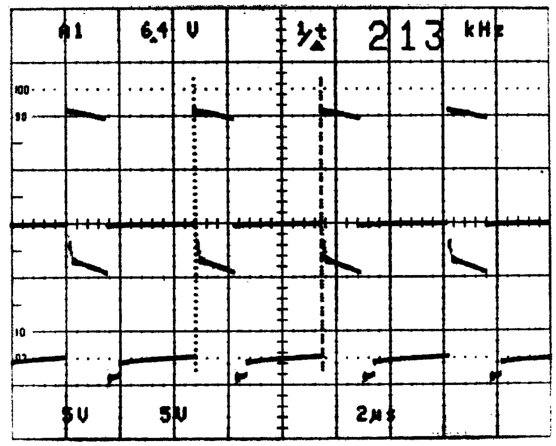
Low-power converter has galvanic isolation

JOSE CARRASCO, UNIVERSIDAD DE VALENCIA, SPAIN

Certain low-power applications require a simple, low-cost, galvanically isolated power supply. **Figure 1** shows a circuit that meets these requirements. The dc/dc converter provides a 12V, 150-mW output using only a few components and a small transformer. The input can come from any power source that supplies 14 to 18V. The CD4049 forms an oscillator that operates at approximately 200 kHz (**Figure 2**). The asymmetry of the oscillator's waveform depends on the value of R. The voltage V_S in **Figure 1** is proportional to the waveform's asymmetry.

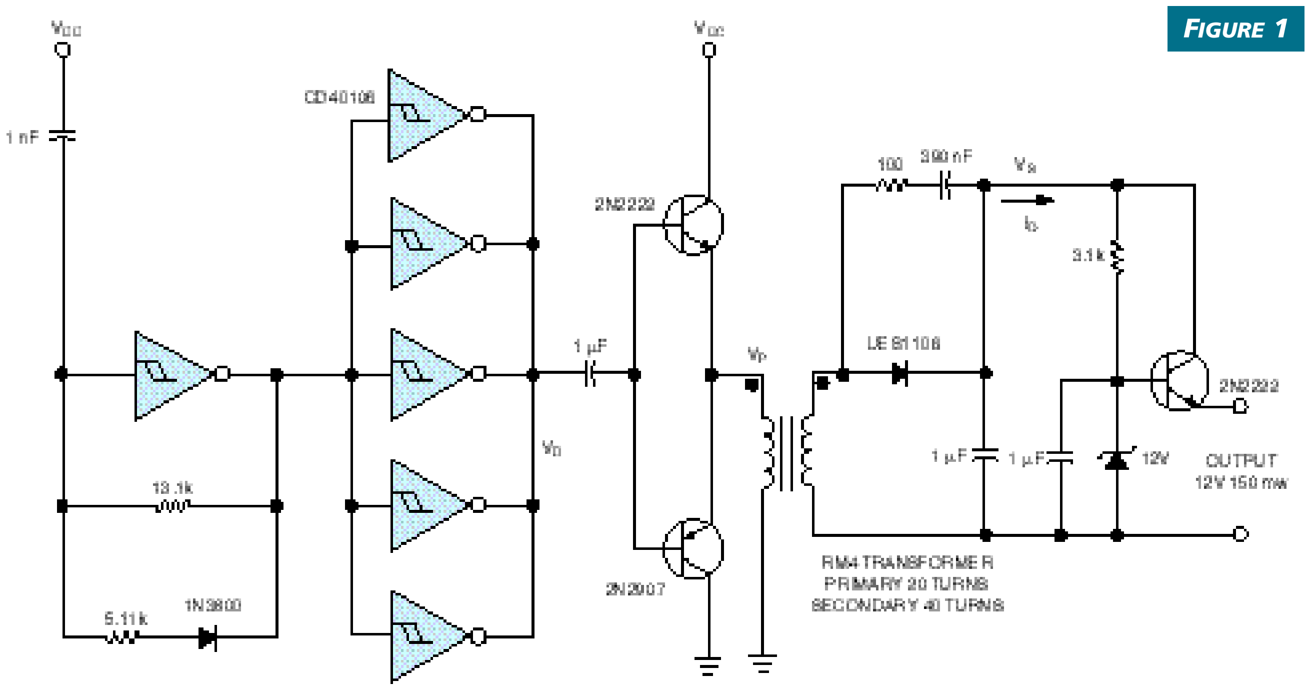
You could also use the circuit as a dc/dc converter with unity transfer ratio by removing the regulator stage at the output. You can easily change the transfer ratio by varying the oscillator's duty cycle (by adjusting R). If you need to increase the output power, remember that in this configuration, the load current flowing through the transformer must be much lower than the magnetizing current. (DI #2214) EDN

FIGURE 2



The symmetry of the waveforms of V_D and V_P in Figure 1 determines the value of V_S.

FIGURE 1



A simple CMOS oscillator, an inexpensive transformer, and a few components form a low-cost, galvanically isolated dc/dc converter

Circuit protects against ac-line disturbances

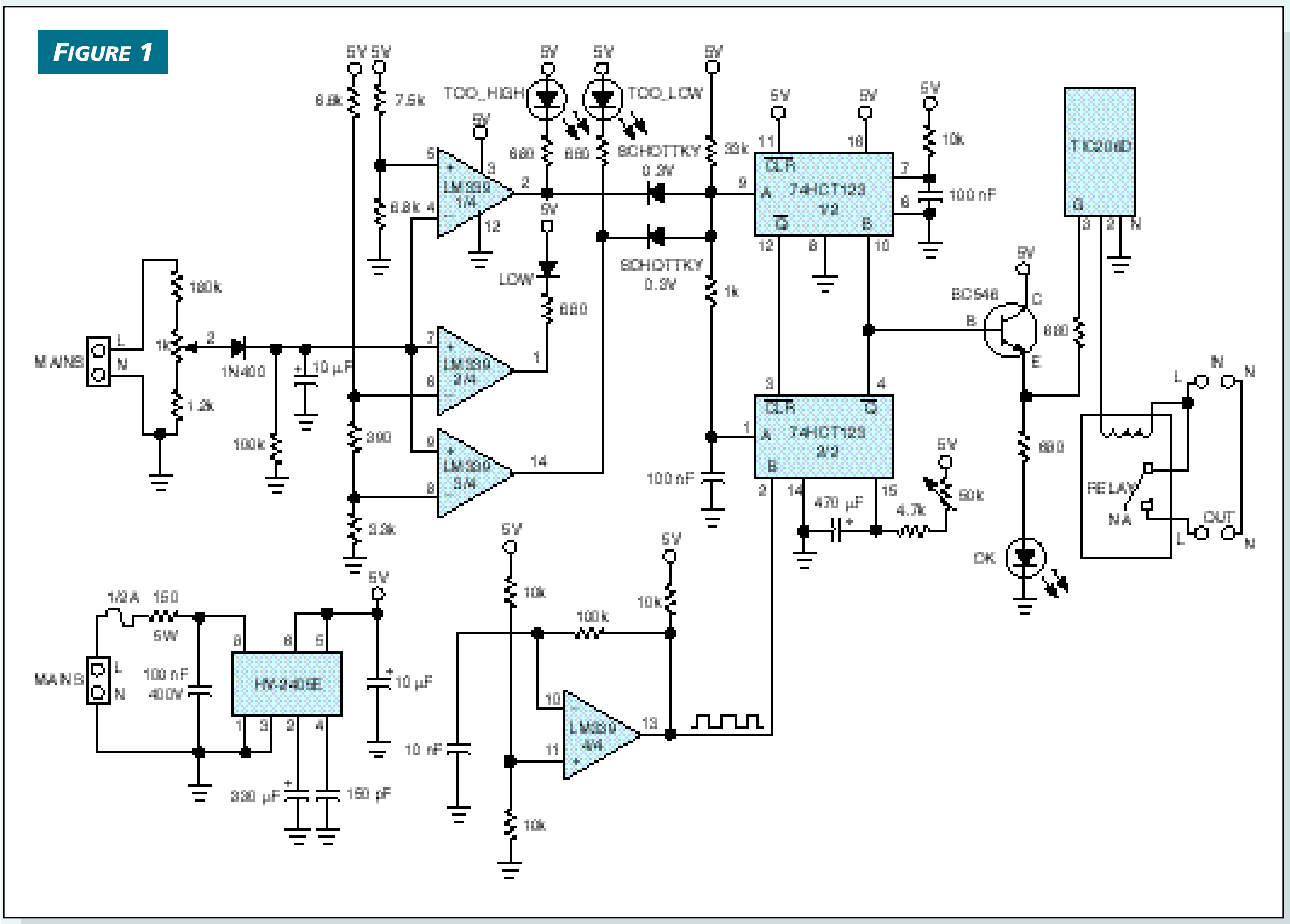
BASILIO SIMOES, ISA, COIMBRA, PORTUGAL

The circuit in **Figure 1** protects the ac line against disturbances. It operates by switching off the power supply upon detection of undervoltage or overvoltage conditions. The circuit thus protects refrigerators, washing machines, air conditioners, and other appliances from permanent damage that could accrue from working outside their specified power requirements. The problem assumes particular importance in underdeveloped countries or regions where the ac-supply network is incorrectly configured, and the voltage frequently drops to levels low enough to damage coils and motors. When the ac-line voltage returns to its nominal level, the circuit automatically resets a switch and reconnects the line voltage.

The input stage contains a voltage divider, which you can adjust with the 1-kΩ potentiometer. The circuit incorporates a rectifying diode and a 10-μF storage capacitor that provides lowpass filtering to stabilize the ac-supply voltage-comparison level. You should adjust the potentiometer such that the normal condition of the ac supply, 220V, corresponds to a 1.97V voltage-comparison level. Three comparison voltages verify the ac-line status, using resistive voltage dividers. The voltages correspond to a 10%-undervoltage warning, a 20%-undervoltage failure level, and a 20%-overvoltage failure level. These comparison voltages correspond to ac-supply voltages of 198, 176, and 264V, respectively. Three sections of the quad open-collector LM339 comparator convert these voltage thresholds to digital signals.

The 10%-undervoltage warning condition turns on a yellow LED. Failure conditions turn on a red LED and trigger

FIGURE 1



Avoid motor burnout, using this circuit that provides undervoltage warning signals and disconnects the line from the load for severe under- and overvoltage conditions.

the dual retriggerable monostable multivibrator, IC_2. The output of the first ,IC_{2A}, is narrow and serves to define a time window that prevents sudden transient disturbances from triggering IC_{2B}. Consequently, if the ac-line voltage quickly returns to its nominal condition, the circuit does not disconnect the load. The output pulse width of the other monostable, which you can adjust via the 50-kΩ potentiometer, defines the time the load remains disconnected after the return of the nominal ac-line voltage.

An RC delay line ensures that when the second monostable triggers, the first one has already activated its Clear input. The fourth comparator of the LM339 produces a high-frequency square wave that continuously retriggers the monostable while the fault condition is present. To save power from the regulated 5V supply and to allow use of this circuit to protect high-current equipment, you should use an output relay whose coil control comes from the power-supply rail. A TIC206D triac, gated by the monostable, switches the relay coil. A green LED indicates that the ac-line level is normal and the relay's contact is closed. IC_1, a Harris HV-2405E offline regulator, supplies the regulated 5V. Because this circuit connects to the ac line, you should use an insulated enclosure, and take care in testing the circuit. (DI #2215)

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Fleapower circuit detects short circuits

W DIJKSTRA, WAALRE, THE NETHERLANDS

Sometimes, the need arises for a short-circuit tester that supplies a low current to the device under test (DUT) and also uses voltages lower than 100 mV to prevent conduction of semiconductors. The circuit in **Figure 1** meets these requirements. R_1 limits the current in the DUT to 0.9 mA. The voltage on the DUT can not exceed the value set by the ratio $R_2/(R_1+R_2)$. The NE5230 micropower op amp compares the voltage on R_X (representing the DUT) with the voltage at the junction of R_3 and R_4. You can adjust the op amp's supply current by trimming R_5; in this circuit, the current is 0.1 mA. If the value of R_X falls below 14Ω, the output of the op amp switches low and the LED illuminates. The circuit derives its power from a 1.5V battery. IC_1 converts the battery voltage to 5V. (DI #2216)

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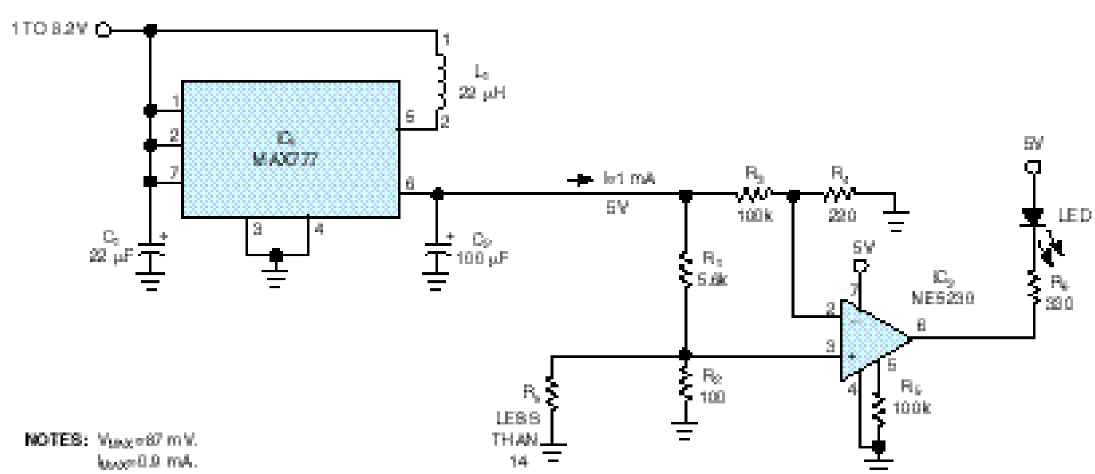
FIGURE 1



This short-circuit detector uses little power, and provides low currents and voltages to avoid damage to the device under

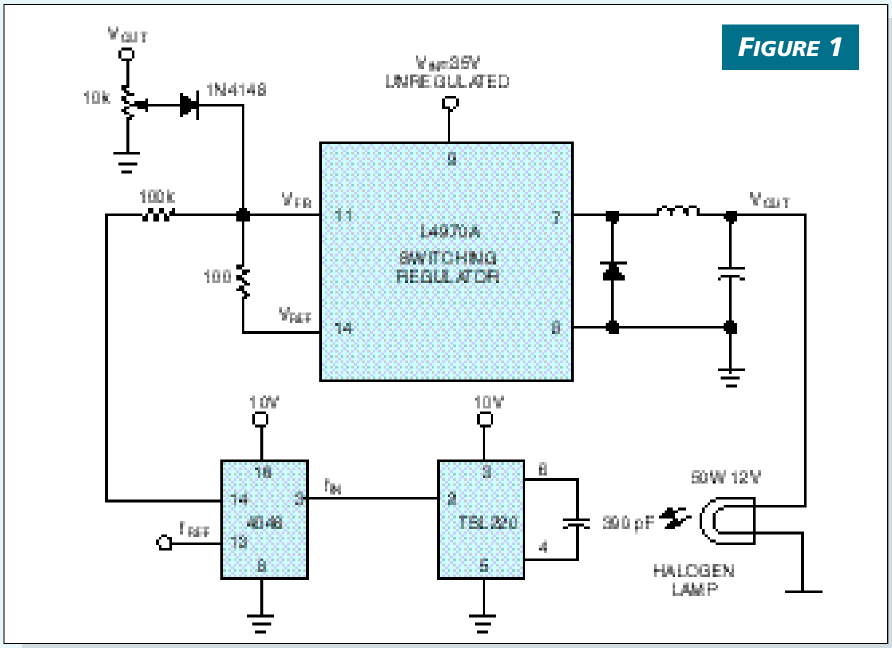
PLL-based converter controls light source

MASSIMO GOTTARDI, ITC-IRST, TRENTO, ITALY

Using the circuit in **Figure 1** , you can digitally control the light intensity of a lamp. The control loop is based on a PLL, in which the VCO comprises a light-to-frequency converter (TSL220) coupled to a light source that derives its drive from a switching regulator (L4970A). The output of the phase/frequency comparator (4046) serves as the control voltage for the switching regulator. The control voltage is proportional to the frequency error between the reference frequency (f_{REF}) and the signal frequency (f_{IN}) coming from the light-to-frequency converter.

Changing the reference frequency regulates the voltage supplied to the lamp to force the output of the TSL220 to lock to f_{REF}. The two resistors at the output of the 4046 provide an attenuation of 1000 to guarantee the loop stability. As an example, we used the L4970A to drive a 12V, 50W halogen lamp. The control loop operates over a frequency of dc to 500 kHz. To prevent the system from entering a positive-feedback condition, the maximum allowable value of f_{REF} should not exceed the saturation frequency of the TSL220. This maximum value depends on the integrating capacitor used for the light-to-frequency converter and must not exceed 750 kHz. To prevent lamp damage, the 10-kΩ trimmer limits the voltage V_{OUT} applied to the light source. (DI #2219)

FIGURE 1



A PLL and a light-to-frequency converter allow you to digitally control the intensity of a lamp.

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Relay driver saves substantial power

TIM HERKLOTS, MAXIM INTEGRATED PRODUCTS, SOUTHAMPTON, UK

It is common practice to operate relays and solenoids at a reduced holding power once the mechanical actuation takes place. Relays are usually specified to pull in within 3 msec at 80% of the rated voltage and to release at 30% of the rated voltage. The circuit in **Figure 1** drives as many as eight 12V (120Ω coil) power relays, which memory-map into an 8-bit μP bus. An octal latch stores the relay status, where each bit of the 8-bit word serves a separate relay (0=off, 1=on). The latch's Select line latches data on the rising edge. Whenever the relay's status data changes, the relay's drive voltage rises to the full 12V for 140 msec to ensure that the relay pulls in. A series zener diode then reduces the relay's drive voltage by 50% to reduce dissipation.

A ULN2803, an octal Darlington array with base resistors for direct logic interface, drives the relays. A useful feature is the inclusion of eight inductive-load clamping diodes, internally connected between the Outx pins and the Com pin. Com thus connects to the relay-supply rail. The power-saving timing comes from IC_1, a micropower MAX810 processor supervisor powered by the normally high Select line. When the system processor writes to the IC_2 latch, the supply to IC_1 toggles for 200 nsec, causing IC_1 to take its RST output high for 140 to 560 msec. Q_1 operates as a gated current source, dragging current from Q_2, thereby shorting out D_1, a 5.6V zener diode. Hence, the relays receive full bus power during the switching phase. After this period, Q_2 turns off, and D_1 drops the relay supply to the holding voltage. (DI #2217)

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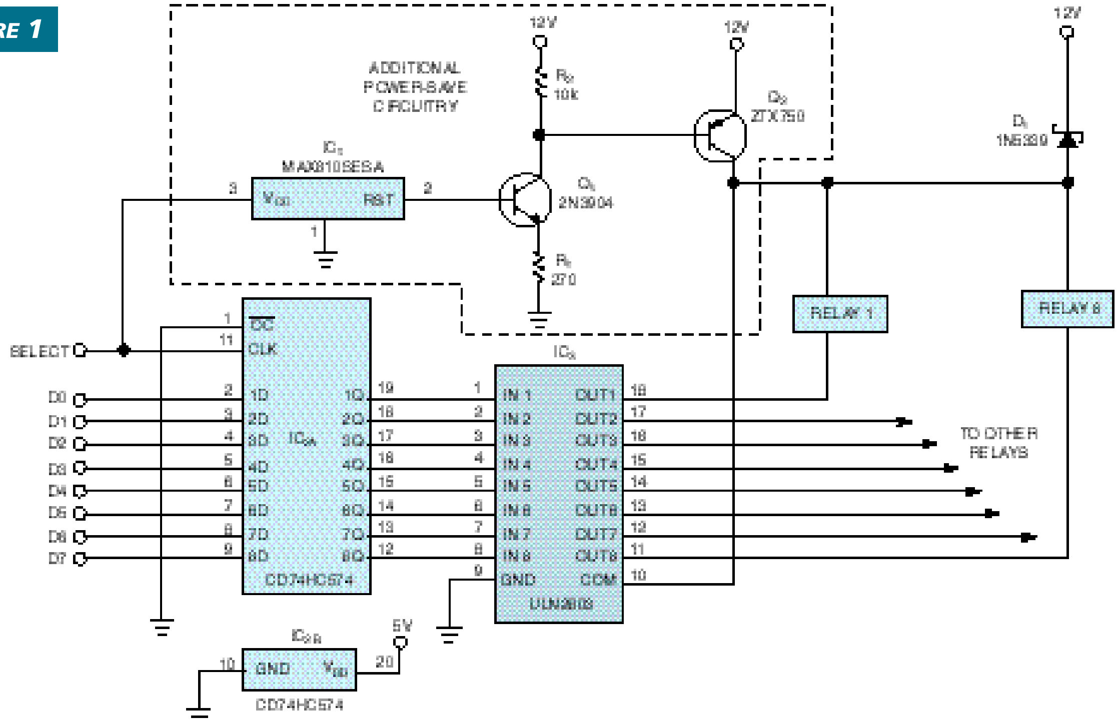
FIGURE 1



This power-saving circuit takes advantage of the large turn-on/turn-off hysteresis in electromechanical relays and solenoids.