

Power MOSFET Basics

Vrej Barkhordarian, International Rectifier, El Segundo, Ca.

Discrete power MOSFETs employ semiconductor processing techniques that are similar to those of today's VLSI circuits, although the device geometry, voltage and current levels are significantly different from the design used in VLSI devices. The metal oxide semiconductor field effect transistor (MOSFET) is based on the original field-effect transistor introduced in the 70s. Figure 1 shows the device schematic, transfer characteristics and device symbol for a MOSFET. The invention of the power MOSFET was partly driven by the limitations of bipolar power junction transistors (BJTs) which, until recently, was the device of choice in power electronics applications.

Although it is not possible to define absolutely the operating boundaries of a power device, we will loosely refer to the power device as any device that can switch at least 1A. The bipolar power transistor is a current controlled device. A large base drive current as high as one-fifth of the collector current is required to keep the device in the ON state.

Also, higher reverse base drive currents are required to obtain fast turn-off. Despite the very advanced state of manufacturability and lower costs of BJTs, these limitations have made the base drive circuit design more complicated and hence more expensive than the power MOSFET.

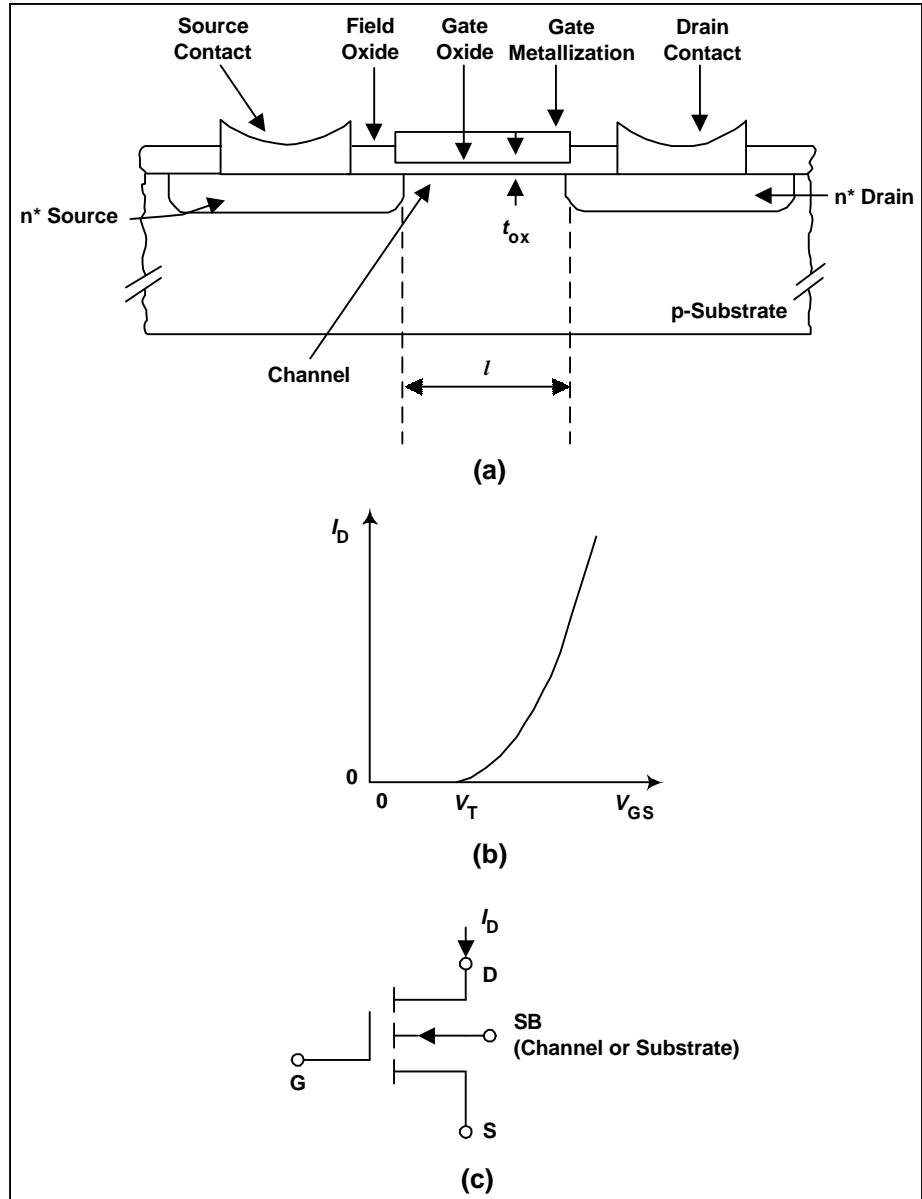


Figure 1. Power MOSFET (a) Schematic, (b) Transfer Characteristics, (c) Device Symbol.

Another BJT limitation is that both electrons and holes contribute to conduction. Presence of holes with their higher carrier lifetime causes the switching speed to be several orders of magnitude slower than for a power MOSFET of similar size and voltage rating. Also, BJTs suffer from thermal runaway. Their forward voltage drop decreases with increasing temperature causing diversion of current to a single device when several devices are paralleled. Power MOSFETs, on the other hand, are majority carrier devices with no minority carrier injection. They are superior to the BJTs in high frequency applications where switching power losses are important. Plus, they can withstand simultaneous application of high current and voltage without undergoing destructive failure due to second breakdown. Power MOSFETs can also be paralleled easily because the forward voltage drop increases with increasing temperature, ensuring an even distribution of current among all components.

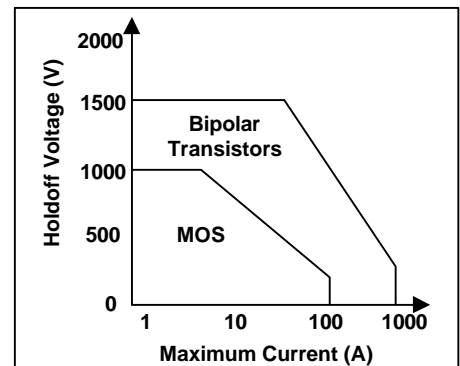


Figure 2. Current-Voltage Limitations of MOSFETs and BJTs.

However, at high breakdown voltages (>200V) the on-state voltage drop of the power MOSFET becomes higher than that of a similar size bipolar device with similar voltage rating. This makes it more attractive to use the bipolar power transistor at the expense of worse high frequency performance. Figure 2 shows the present current-voltage limitations of power MOSFETs and BJTs. Over time, new materials, structures and processing techniques are expected to raise these limits.

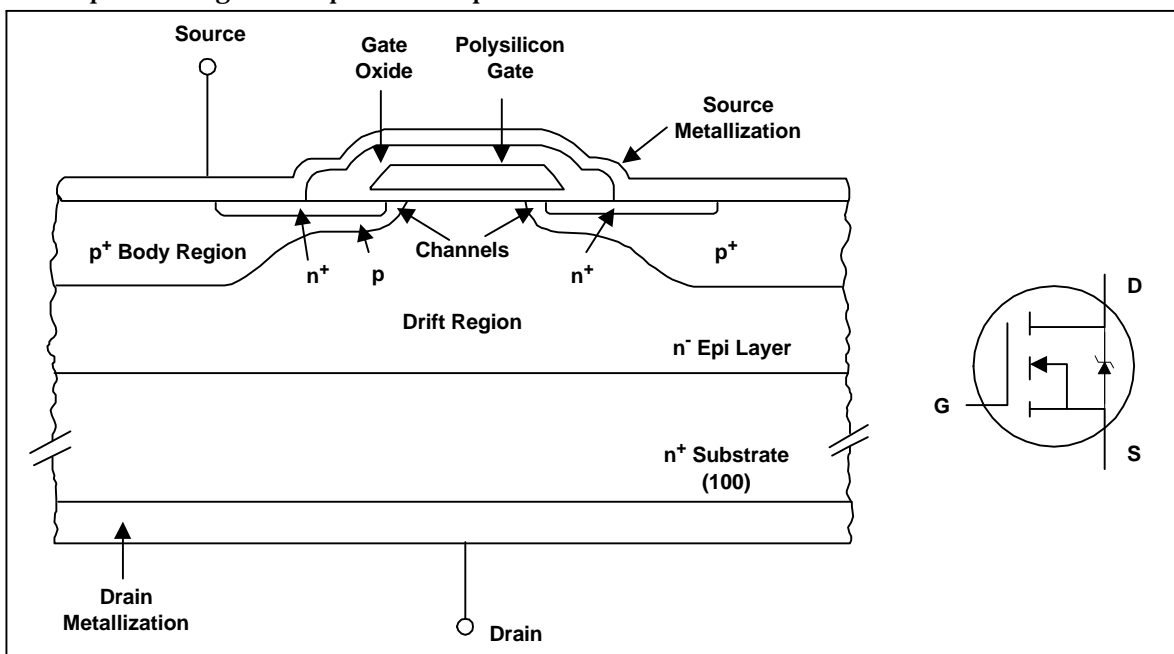


Figure 3. Schematic Diagram for an n-Channel Power MOSFET and the Device.

Figure 3 shows schematic diagram and Figure 4 shows the physical origin of the parasitic components in an n-channel power MOSFET. The parasitic JFET appearing between the two body implants restricts current flow when the depletion widths of the two adjacent body diodes extend into the drift region with increasing drain voltage. The parasitic BJT can make the device susceptible to unwanted device turn-on and premature breakdown. The base resistance R_B must be minimized through careful design of the doping and distance under the source region. There are several parasitic capacitances associated with the power MOSFET as shown in Figure 3.

C_{GS} is the capacitance due to the overlap of the source and the channel regions by the polysilicon gate and is independent of applied voltage. C_{GD} consists of two parts, the first is the capacitance associated with the overlap of the polysilicon gate and the silicon underneath in the JFET region. The second part is the capacitance associated with the depletion region immediately under the gate. C_{GD} is a nonlinear function of voltage. Finally, C_{DS} , the capacitance associated with the body-drift diode, varies inversely with the square root of the drain-source bias. There are currently two designs of power MOSFETs, usually referred to as the planar and the trench designs. The planar design has already been introduced in the schematic of Figure 3. Two variations of the trench power MOSFET are shown Figure 5. The trench technology has the advantage of higher cell density but is more difficult to manufacture than the planar device.

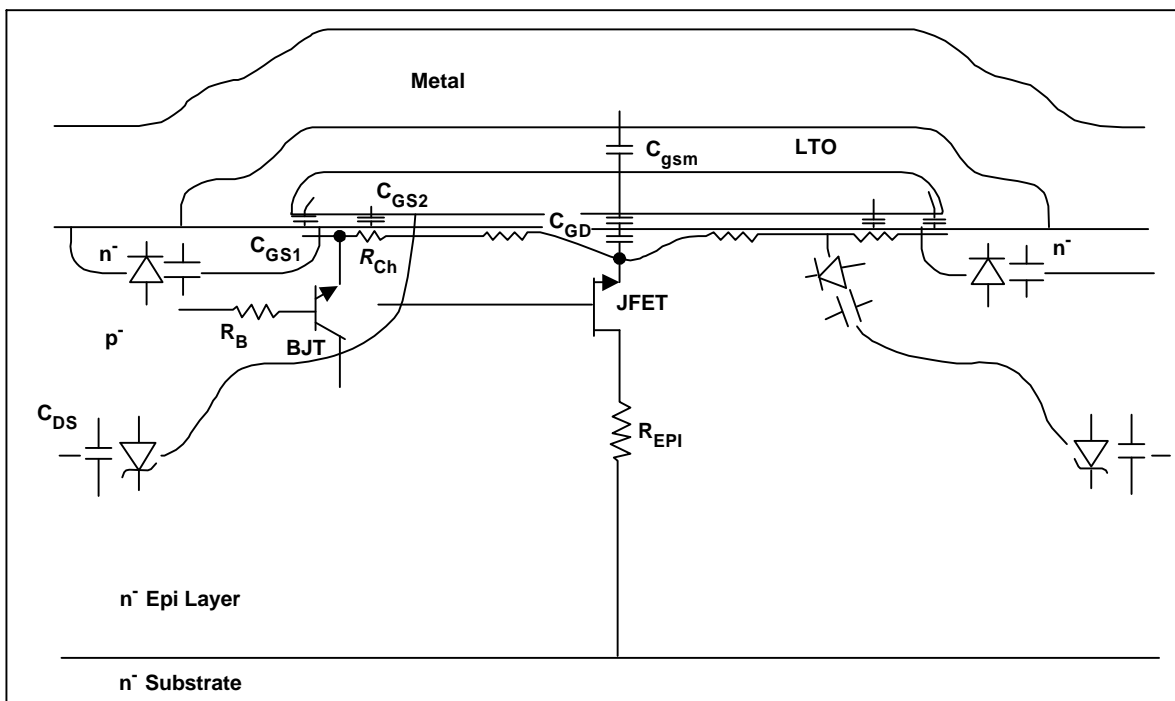


Figure 4. Power MOSFET Parasitic Components.

BREAKDOWN VOLTAGE

Breakdown voltage, BV_{DSS} , is the voltage at which the reverse-biased body-drift diode breaks down and significant current starts to flow between the source and drain by the avalanche multiplication process, while the gate and source are shorted together. Current-voltage characteristics of a power MOSFET are shown in Figure 6. BV_{DSS} is normally measured at $250\mu A$ drain current. For drain voltages below BV_{DSS} and with no bias on the gate, no channel is formed under the gate at the surface and the drain voltage is entirely supported by the reverse-biased body-drift p-n junction. Two related phenomena can occur in poorly designed and processed devices: punch-through and reach-through. Punch-through is observed when the depletion region on the source side of the body-drift p-n junction reaches the source region at drain voltages below the rated avalanche voltage of the device. This provides a current path between source and drain and causes a soft breakdown characteristics as shown in Figure 7. The leakage current flowing between

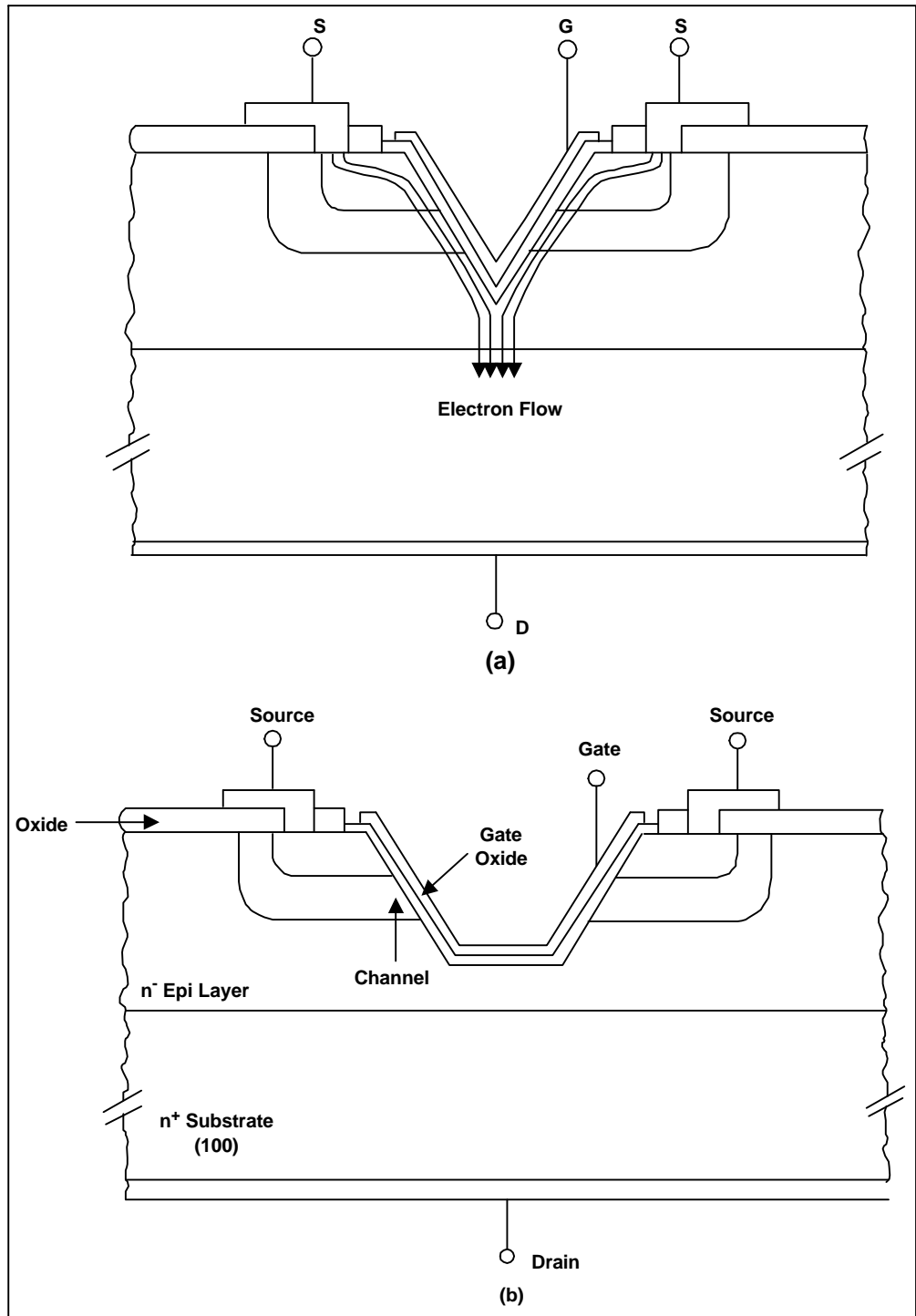


Figure 5. Trench MOSFET (a) Current Crowding in V-Groove Trench MOSFET, (b) Truncated V-Groove MOSFET

source and drain is denoted by I_{DSS} . There are tradeoffs to be made between $R_{DS(on)}$ that requires shorter channel lengths and punch-through avoidance that requires longer channel lengths.

The reach-through phenomenon occurs when the depletion region on the drift side of the body-drift p-n junction reaches the epilayer-substrate interface before avalanching takes place in the epi. Once the depletion edge enters the high carrier concentration substrate, a further increase in drain voltage will cause the electric field to quickly reach the critical value of 2×10^5 V/cm where avalanching begins.

ON-RESISTANCE

The on-state resistance of a power MOSFET is made up of several components as shown in Figure 8:

$$R_{DS(on)} = R_{source} + R_{ch} + R_A + R_J + R_D + R_{sub} + R_{wcml} \quad (1)$$

where:

R_{source} = Source diffusion resistance

R_{ch} = Channel resistance

R_A = Accumulation resistance

R_J = "JFET" component-resistance of the region between the two body regions

R_D = Drift region resistance

R_{sub} = Substrate resistance

Wafers with substrate resistivities of up to 20mΩ-cm are used for high voltage devices and less than 5mΩ-cm for low voltage devices.

R_{wcml} = Sum of Bond Wire resistance, the Contact resistance between the source and drain Metallization and the silicon, metallization and Leadframe contributions. These are normally negligible in high voltage devices but can become significant in low voltage devices.

Figure 9 shows the relative importance of each of the components to $R_{DS(on)}$ over the voltage spectrum. As can be seen, at high voltages the $R_{DS(on)}$ is dominated by epi resistance and JFET component. This component is higher in high voltage devices due to the higher resistivity or lower background carrier concentration in the epi. At lower voltages, the $R_{DS(on)}$ is dominated by the channel resistance and the contributions from the metal to semiconductor contact, metallization, bond wires and leadframe. The substrate contribution becomes more significant for lower breakdown voltage devices.

TRANSCONDUCTANCE

Transconductance, g_{fs} , is a measure of the sensitivity of drain current to changes in gate-source bias. This parameter is normally quoted for a V_{gs} that gives a drain current equal to about one half of the maximum current rating value and for a V_{DS} that ensures operation in the constant current region. Transconductance is influenced by gate width, which increases in proportion to the active area as cell density increases. Cell density has increased over the years from around half a million per square inch in 1980 to around eight million for planar MOSFETs and around 12 million for the trench technology. The limiting factor for even higher cell densities is the photolithography process control and resolution that allows contacts to be made to the source metallization in the center of the cells.

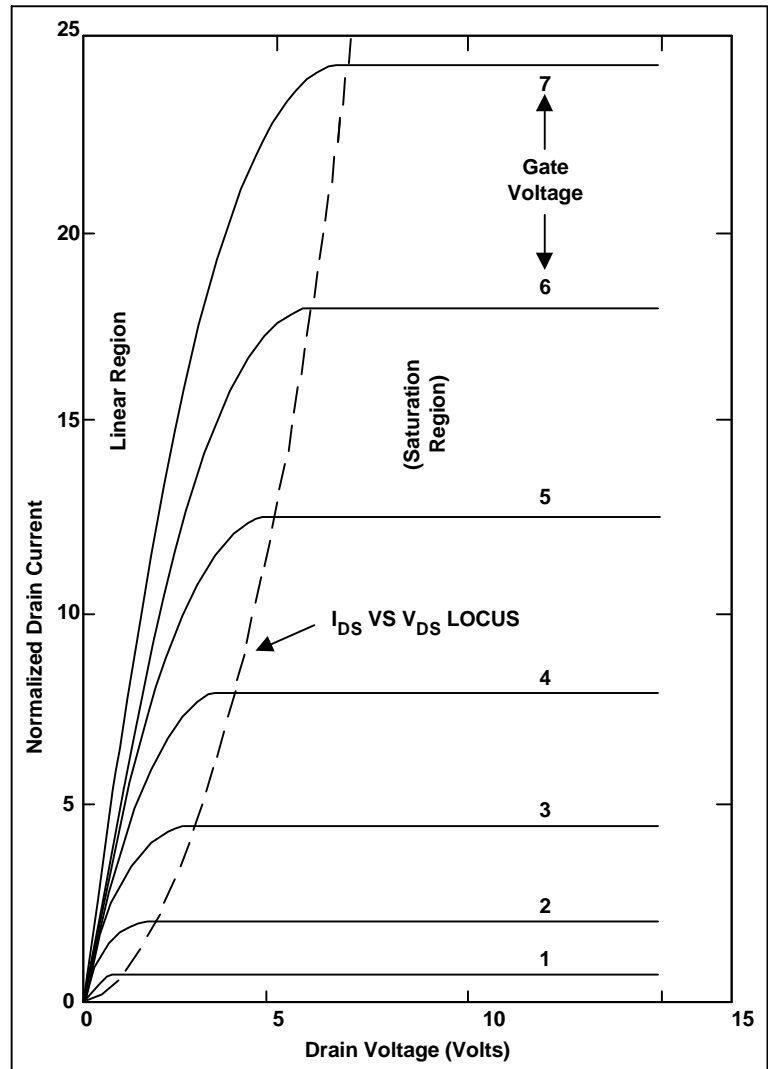


Figure 6. Current-Voltage Characteristics of Power MOSFET

Channel length also affects transconductance. Reduced channel length is beneficial to both g_{fs} and on-resistance, with punch-through as a tradeoff. The lower limit of this length is set by the ability to control the double-diffusion process and is around 1-2 μ m today. Finally the lower the gate oxide thickness the higher the g_{fs} .

THRESHOLD VOLTAGE

Threshold voltage, V_{th} , is defined as the minimum gate electrode bias required to strongly invert the surface under the poly and form a conducting channel between the source and the drain regions. V_{th} is usually measured at a drain-source current of 250 μ A. Common values are 2-4V for high voltage devices with thicker gate oxides, and 1-2V for lower voltage, logic-compatible devices with thinner gate oxides. With power MOSFETs finding increasing use in portable electronics and wireless communications where battery power is at a premium, the trend is toward lower values of $R_{DS(on)}$ and V_{th} .

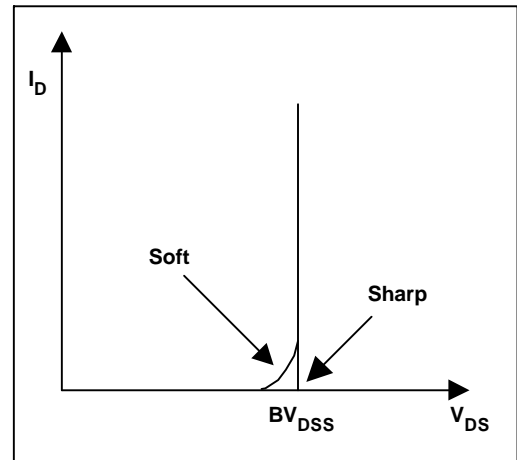


Figure 7. Power MOSFET Breakdown Characteristics

DIODE FORWARD VOLTAGE

The diode forward voltage, V_F , is the guaranteed maximum forward drop of the body-drain diode at a specified value of source current. Figure 10 shows a typical I-V characteristics for this diode at two temperatures. P-channel devices have a higher V_F due to the higher contact resistance between metal and p-silicon compared with n-type silicon. Maximum values of 1.6V for high voltage devices (>100V) and 1.0V for low voltage devices (<100V) are common.

POWER DISSIPATION

The maximum allowable power dissipation that will raise the die temperature to the maximum allowable when the case temperature is held at 25 $^{\circ}$ C is important. It is given by P_d where:

$$P_d = \frac{T_{jmax} - 25}{R_{thJC}} \quad (2)$$

T_{jmax} = Maximum allowable temperature of the p-n junction in the device (normally 150 $^{\circ}$ C or 175 $^{\circ}$ C)
 R_{thJC} = Junction-to-case thermal impedance of the device.

DYNAMIC CHARACTERISTICS

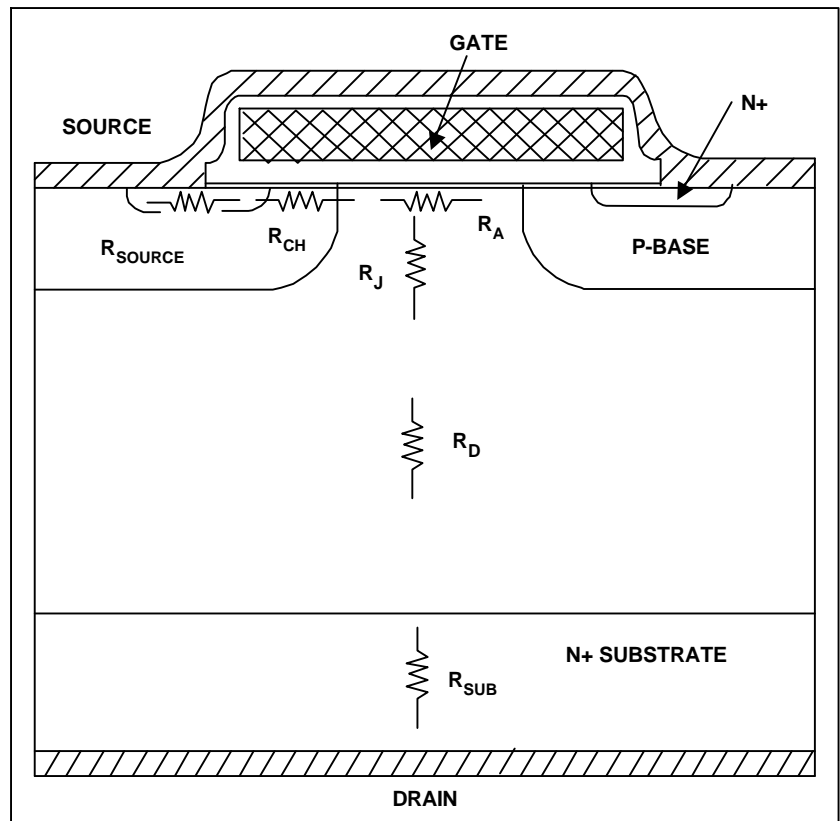


Figure 8. Origin of Internal Resistance in a Power MOSFET.

When the MOSFET is used as a switch, its basic function is to control the drain current by the gate voltage. Figure 11(a) shows the transfer characteristics and Figure 11(b) is an equivalent circuit model often used for the analysis of MOSFET switching performance.

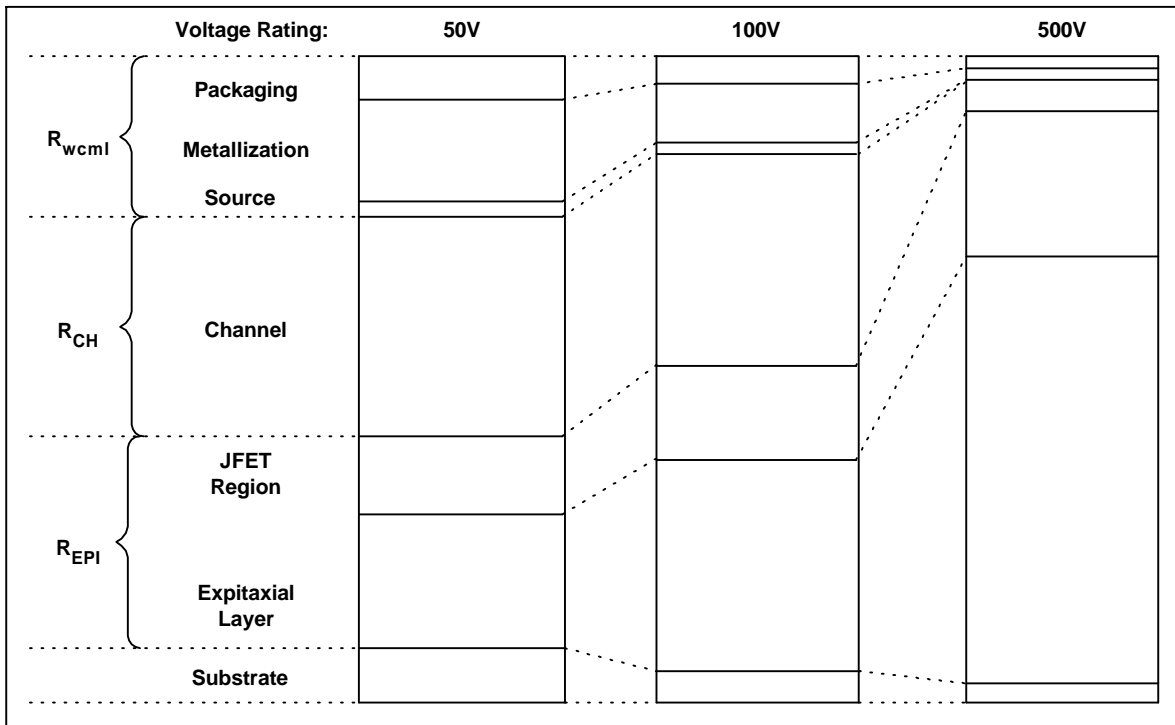


Figure 9. Relative Contributions to $R_{DS(on)}$ With Different Voltage Ratings.

The switching performance of a device is determined by the time required to establish voltage changes across capacitances. R_G is the distributed resistance of the gate and is approximately inversely proportional to active area. L_S and L_D are source and drain lead inductances and are around a few tens of nH. Typical values of input (C_{iss}), output (C_{oss}) and reverse transfer (C_{rss}) capacitances given in the data sheets are used by circuit designers as a starting point in determining circuit component values. The data sheet capacitances are defined in terms of the equivalent circuit capacitances as:

$$C_{iss} = C_{GS} + C_{GD}, C_{DS} \text{ shorted}$$

$$C_{rss} = C_{GD}$$

$$C_{oss} = C_{DS} + C_{GD}$$

Gate-to-drain capacitance, C_{GD} , is a nonlinear function of voltage and is the most important parameter because it provides a feedback loop between the output and the input of the circuit. C_{GD} is also called the Miller capacitance because it causes the total dynamic input capacitance to become greater than the sum of the static capacitances.

Figure 12 shows a typical switching time test circuit. Also shown are the components of the rise and fall times with reference to the V_{GS} and V_{DS} waveforms.

Turn-on delay, $t_{d(on)}$, is the time taken to charge the input capacitance of the device before drain current conduction can start. Similarly, turn-off delay, $t_{d(off)}$, is the time taken to discharge the capacitance after the after is switched off.

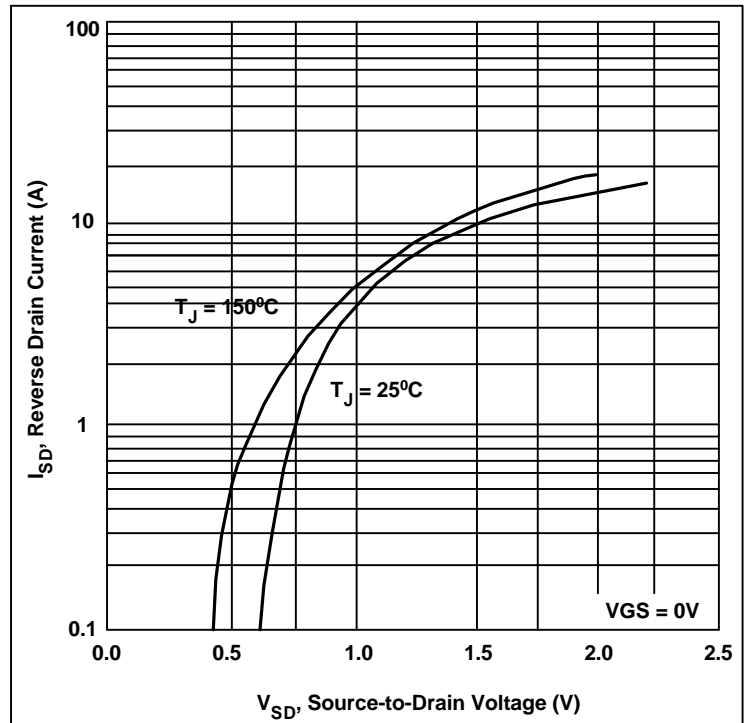


Figure 10. Typical Source-Drain (Body) Diode Forward Voltage Characteristics.

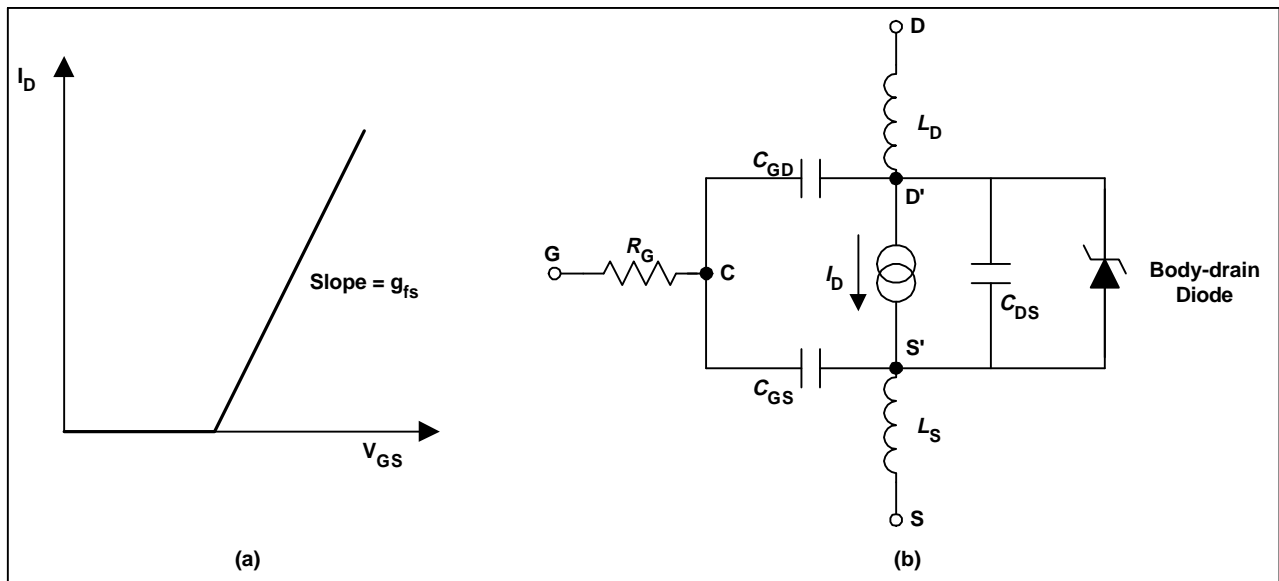


Figure 11. Power MOSFET (a) Transfer characteristics, (b) Equivalent Circuit Showing Components That Have Greatest Effect on Switching

GATE CHARGE

Although input capacitance values are useful, they do not provide accurate results when comparing the switching performances of two devices from different manufacturers. Effects of device size and transconductance make such comparisons more difficult. A more useful parameter from the circuit design point of view is the gate charge rather than capacitance. Most manufacturers include both parameters on their data sheets. Figure 13 shows a typical gate charge waveform and the test circuit. When the gate is connected to the supply voltage, V_{GS} starts to increase until it reaches V_{th} , at which point the drain current starts to flow and the C_{GS} starts to charge. During the period t_1 to t_2 , C_{GS} continues to charge, the gate voltage continues to rise and drain current rises proportionally. At time t_2 , C_{GS} is completely charged and the drain current reaches the predetermined current I_D and stays constant while the drain voltage starts to fall. With reference to the equivalent circuit model of the MOSFET shown in Figure 13, it can be seen that with C_{GS} fully charged at t_2 , V_{GS} becomes constant and the drive current starts to charge the Miller capacitance, C_{DG} . This continues until time t_3 .

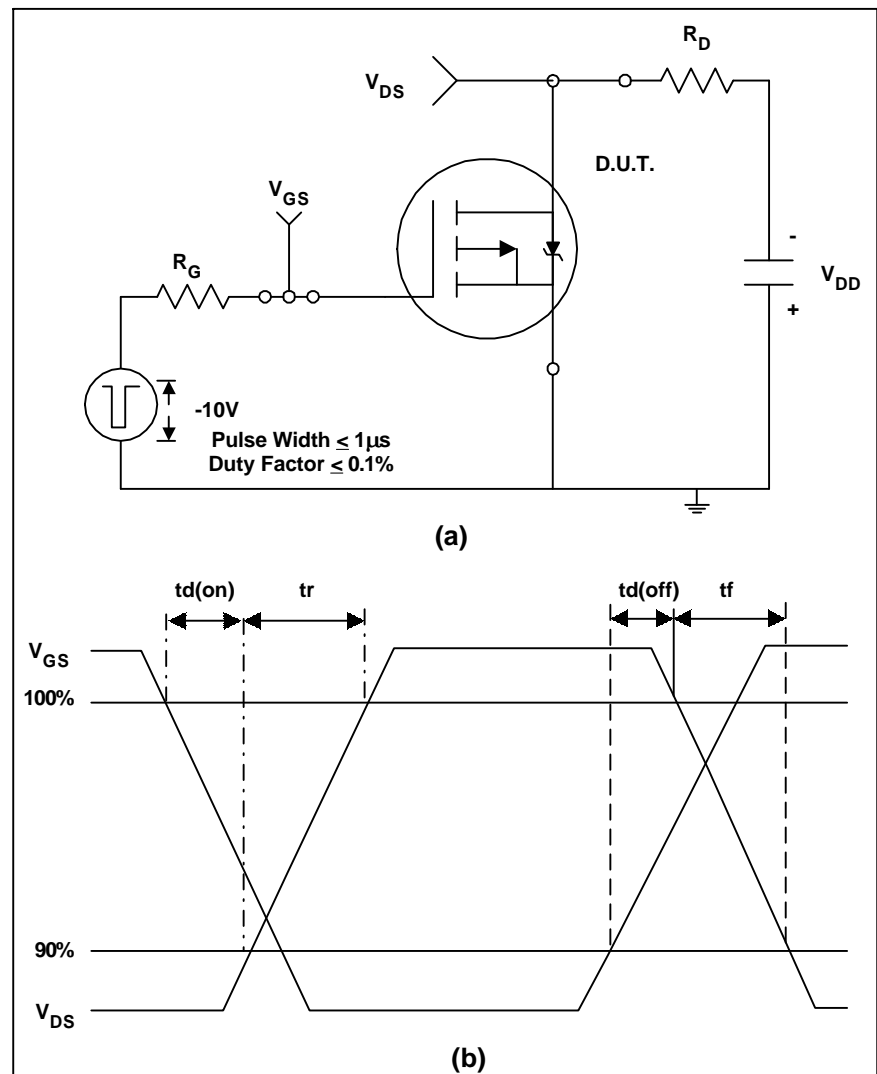


Figure 12. Switching Time Test (a) Circuit, (b) V_{GS} and V_{DS} Waveforms

Charge time for the Miller capacitance is larger than that for the gate to source capacitance C_{GS} due to the rapidly changing drain voltage between t_2 and t_3 (current = $C \, dv/dt$). Once both of the capacitances C_{GS} and C_{GD} are fully charged, gate voltage (V_{GS}) starts increasing again until it reaches the supply voltage at time t_4 . The gate charge ($Q_{GS} + Q_{GD}$) corresponding to time t_3 is the bare minimum charge required to switch the device on. Good circuit design practice dictates the use of a higher gate voltage than the bare minimum required for switching and therefore the gate charge used in the calculations is Q_G corresponding to t_4 .

The advantage of using gate charge is that the designer can easily calculate the amount of current required from the drive circuit to switch the device on in a desired length of time because $Q = CV$ and $I = C \, dv/dt$, the $Q = \text{Time} \times \text{current}$. For example, a device with a gate charge of 20nC can be turned on in $20\mu\text{sec}$ if 1mA is supplied to the gate or it can turn on in 20nsec if the gate current is increased to 1A . These simple calculations would not have been possible with input capacitance values.

dv/dt CAPABILITY

Peak diode recovery is defined as the maximum rate of rise of drain-source voltage allowed, i.e., dv/dt capability. If this rate is exceeded then the voltage across the gate-source terminals may become higher than the threshold voltage of the device, forcing the device into current conduction mode, and under certain conditions a catastrophic failure may occur. There are two possible mechanisms by which a dv/dt induced turn-on may take place. Figure 14 shows the equivalent circuit model of a power MOSFET, including the parasitic BJT. The first mechanism of dv/dt induced turn-on becomes active through the feedback action of the gate-drain capacitance, C_{GD} . When a voltage ramp appears across the drain and source terminal of the device a current I_1 flows through the gate resistance, R_G , by means of the gate-drain capacitance, C_{GD} . R_G is the total gate resistance in the circuit and the voltage drop across it is given by:

$$V_{GS} = I_1 R_G = R_G C_{GD} \frac{dv}{dt} \quad (3)$$

When the gate voltage V_{GS} exceeds the threshold voltage of the device V_{th} , the device is forced into conduction. The dv/dt capability for this mechanism is thus set by:

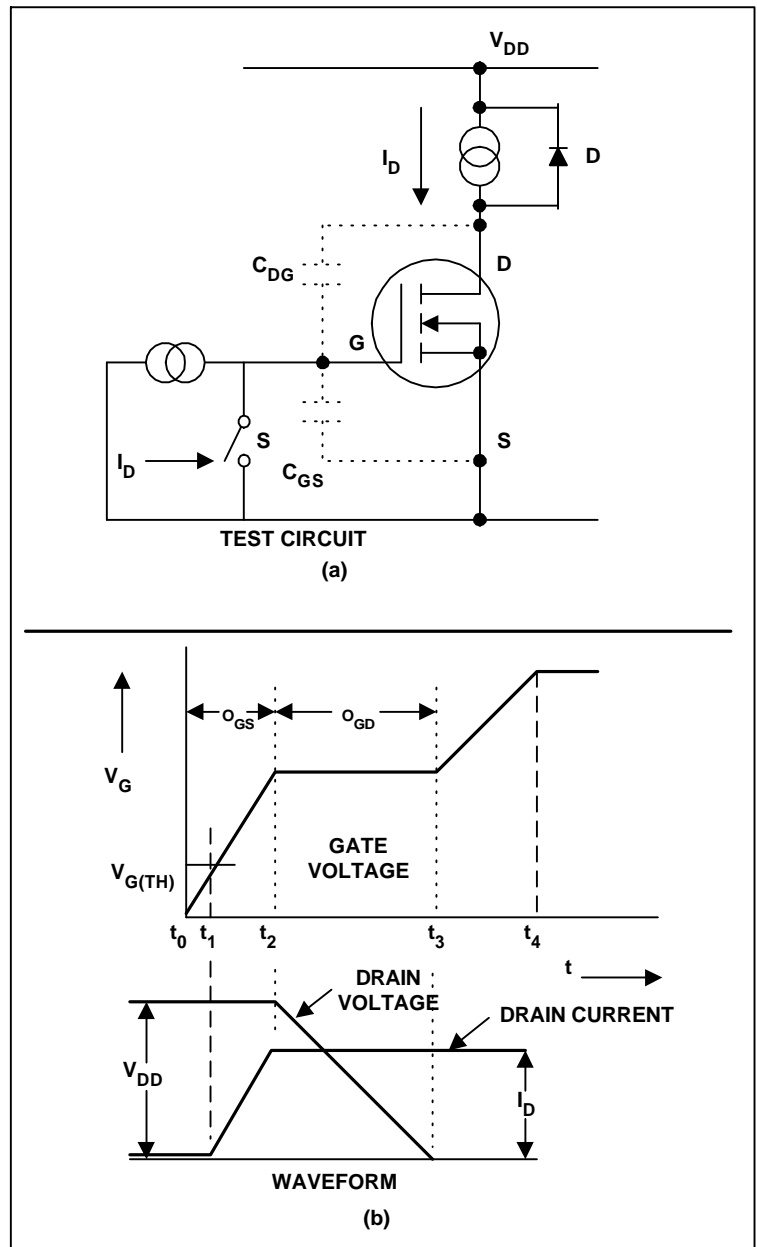


Figure 13. Gate Charge Test (a) Circuit, (b) Resulting Gate and Drain Waveforms.

$$\frac{dv}{dt} = \frac{V_{th}}{R_G C_{GD}} \quad (4)$$

It is clear that low V_{th} devices are more prone to dv/dt turn-on. The negative temperature coefficient of V_{th} is of special importance in applications where high temperature environments are present. Also gate circuit impedance has to be chosen carefully to avoid this effect.

The second mechanism for the dv/dt turn-on in MOSFETs is through the parasitic BJT as shown in Figure 15. The capacitance associated with the depletion region of the body diode extending into the drift region is denoted as C_{DB} and appears between

the base of the BJT and the drain of the MOSFET. This capacitance gives rise to a current I_2 to flow through the base resistance R_B when a voltage ramp appears across the drain-source terminals. With analogy to the first mechanism, the dv/dt capability of this mechanism is:

$$\frac{dv}{dt} = \frac{V_{BE}}{R_B C_{DB}} \quad (5)$$

If the voltage that develops across R_B is greater than about 0.7V, then the base-emitter junction is forward-biased and the parasitic BJT is turned on. Under the conditions of high (dv/dt) and large values of R_B , the breakdown voltage of the MOSFET will be limited to that of the open-base breakdown voltage of the BJT. If the applied drain voltage is greater than the open-base breakdown voltage, then the MOSFET will enter avalanche and may be destroyed if the current is not limited externally.

Increasing (dv/dt) capability therefore requires reducing the base resistance R_B by increasing the body region doping and reducing the distance current I_2 has to flow laterally before it is collected by the source metallization. As in the first mode, the BJT related dv/dt capability becomes worse at higher temperatures because R_B increases and V_{BE} decreases with increasing temperature.

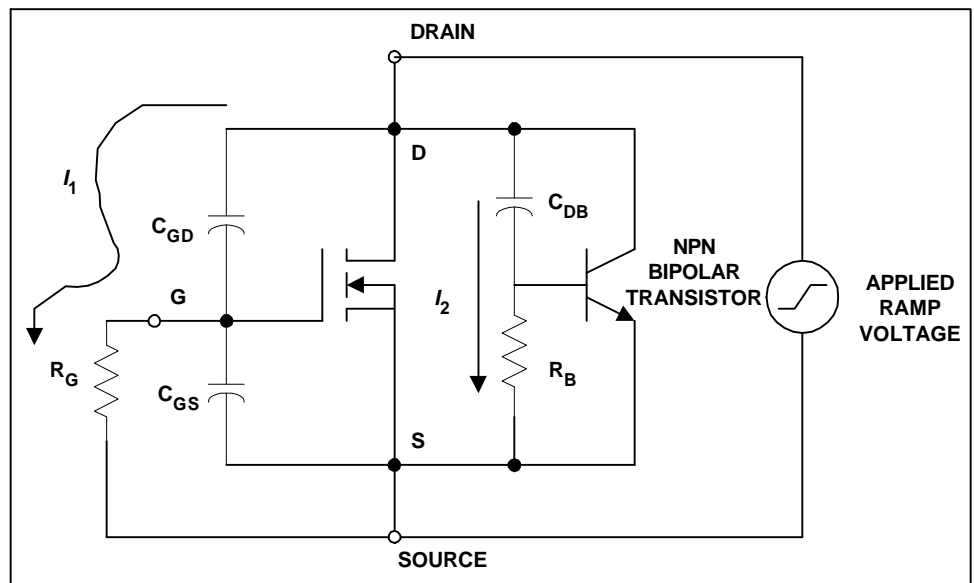


Figure 14. Equivalent Circuit of Power MOSFET Showing Two Possible Mechanisms for dv/dt Induced Turn-on.

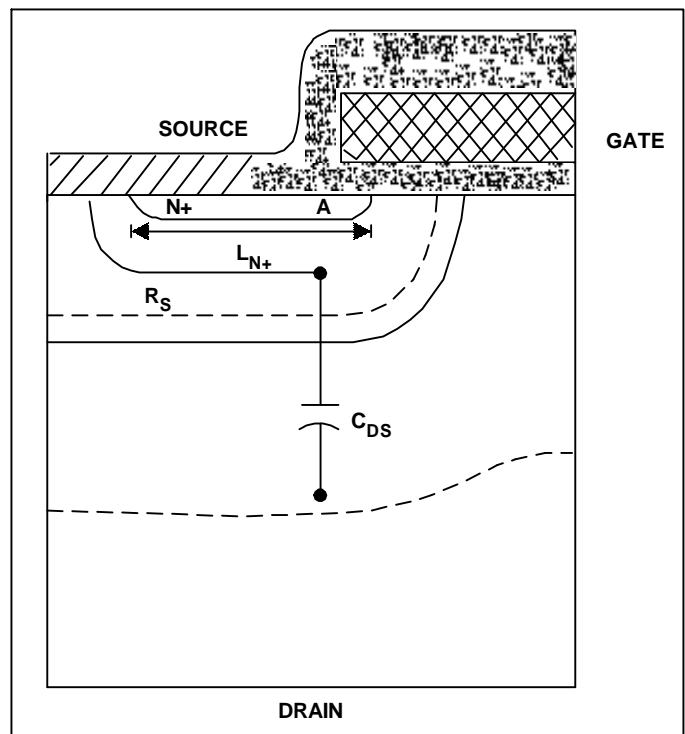


Figure 15. Physical Origin of the Parasitic BJT Components That May Cause dv/dt Induced Turn-on

References:

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