Understanding and Minimizing Ground Bounce

Fairchild
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FAIRCHILD SEMICONDUCTOR™

As system designers begin to use high performance logic families to increase system performance, they may run into new problems which previously did not raise concern when lower performance devices were utilized. These problems can generally be avoided by following a few simple rules. This application note discusses the subject of ground bounce with respect to high performance CMOS logic families and offers a set of simple guidelines that will eliminate system problems due to this phenomenon.

Ground bounce has been a concern to some system designers for many years. Its effects can be found in most bipolar and CMOS logic families. However, ground bounce has recently become a major issue. Although new advanced CMOS logic families have edge rates comparable to advanced bipolar logic devices, CMOS outputs swing almost from rail to rail while bipolar outputs swing from ground to approximately 3.0V. These edge rates, coupled with the greater voltage swings found in today's advanced CMOS logic devices, tend to generate more ground bounce noise than their bipolar counterparts.

In 1982,Fairchild Semiconductor, began to develop FACT™ (Fairchild Advanced CMOS Technology) logic incorporating more than three years of experience gained with FAST® (Fairchild Advanced Schottky TTL) logic into the groundwork. As a result, Fairchild was able to understand the important trade-offs associated with high performance in a logic family. In the bipolar world, these trade-offs were between speed and power; in the CMOS world, the trade-offs are between speed and ease of use. Utilizing experience gained from FAST products, the FACT family objectives were defined to provide the optimum solution, allowing greater system performance while minimizing system design problems. Using FACT devices does require more attention toward circuit design and board layout than older, slower technologies. The resulting advantages—low power and high performance—greatly outweigh these considerations.

DEFINING GROUND BOUNCE

As edge rates and drive capability increase in advanced logic families, the effects of intrinsic electrical characteristics become more pronounced. One of these intrinsic electrical characteristics is the inductance found in all leadframe materials.

Figure 1a shows a simple circuit model for a CMOS device in a leadframe driving a standard test load. The inductor L1 represents the intrinsic inductance in the ground lead of the package; inductor L2 represents the intrinsic inductance in the power lead of the package; inductor L3 represents the intrinsic inductance in the output lead of the package; the resistor R1 represents the output impedance of the device output, and the capacitor and resistor C_L and R_L represent the standard test load on the output of the device.

The three waveforms shown in *Figure 1b, c,* and *d* depict how ground bounce is generated. The first waveform shows the voltage (V) across the load as it is switched from a logic HIGH to a logic LOW. The output slew rate is dependent upon the characteristics of the output transistor, and the inductors L1 and L3, and C_L, the load capacitance. The second waveform shows the current that is generated as the capacitor discharges [$I = -C_L \bullet dV/dt$)]. The third waveform shows the voltage that is induced across the inductance in the ground lead due to the changing currents [$V_{GB} = L \bullet (dI/dt)$].

While these diagrams and figures are useful in explaining the origins of ground bounce, they are highly theoretical and idealistic. There are many second and third order effects which would need to be considered for a complete theoretical analysis. Considering these effects, though, would lead to highly complex second and third order differential equations which are difficult to solve. The purpose of this application note is to develop a fundamental understanding of ground bounce and to provide a useful set of design guide lines. Therefore, we will avoid these lengthy and complex theoretical discussions wherever possible.

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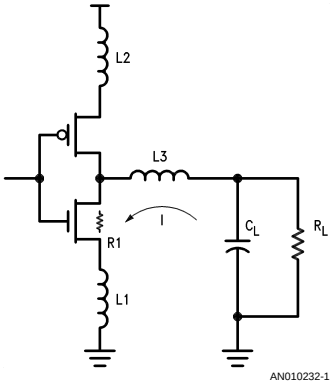
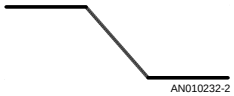
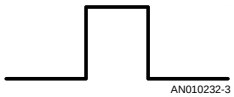


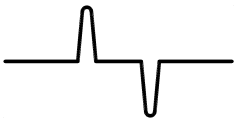
a. Output Model



b. Output Voltage (V)



c. $I = -C_L \bullet (dV/dt)$



d. $V_{GB} = L \bullet (dI/dt)$

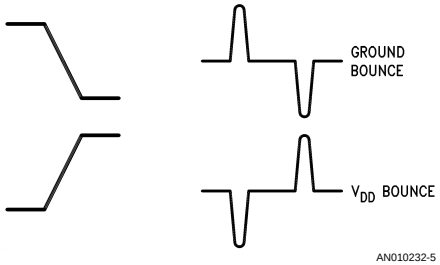
FIGURE 1. Ground Bounce Circuit Model

In order to change the output from a HIGH to a LOW, current must flow to discharge the load capacitance. This current, as it changes, causes a voltage to be generated across the inductances in the circuit. The formula for the voltage across an inductor is V = L • (dI/dt). This induced voltage creates what is known as ground bounce. Because the inductor is between the external system ground and the internal device ground, the induced voltage causes the internal ground to be at a different potential than the external ground. This shift in potential causes the device inputs and outputs to behave differently than expected because they are referenced to the internal device ground, while the devices which are either driving into the inputs or being driven by the outputs are referenced to the external system ground. External to the device, ground bounce causes input thresholds to shift and output levels to change. This situation is very similar to that of large systems where voltages can develop across expansive ground networks.

OTHER CAUSES OF GROUND BOUNCE

Although this discussion is limited to ground bounce generated during HIGH-to-LOW transitions, it should be noted that the ground bounce is also generated during LOW-to-HIGH transitions. This ground bounce is created by the large gate capacitances associated with the output transistors on the die. Because these gate capacitances are larger than the gate capacitances of earlier-stage transistors, more current is generated when they switch. The output buffer stages of CMOS devices are inverters; thus their inputs are switching HIGH-to-LOW when their outputs are switching LOW-to-HIGH. It is the currents associated with switching these inputs to the output transistors that generate ground bounce when the outputs switch LOW-to-HIGH. This LOW-to-HIGH ground bounce has a much smaller amplitude and therefore does not present the same concern.

We should also note that everything discussed here concerning ground bounce can be applied to the opposite effect, V_{DD} bounce. V_{DD} bounce is the inverse of ground bounce. As one would expect, there is an intrinsic inductance in the V_{DD} lead as well as the ground lead. The internal V_{DD} potential will collapse toward ground at the beginning of a LOW-to-HIGH transition and then bounce above the external V_{DD} potential at the end of the transition.



- V_{DD} bounce (droop) is the voltage drop across the package
- Inductance (to V_{DD}) is caused by charging load capacitances
- V_{DD} bounce is less of a concern than ground bounce because TTL-level inputs have greater high noise immunity

FIGURE 2. Ground Bounce/V_{DD} Bounce

In addition, V_{DD} bounce is generated during HIGH-to-LOW transitions for the same reasons that ground bounce is generated during LOW-to-HIGH transitions.

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We will not discuss V_{DD} bounce in this application note because its effects parallel those of ground bounce, and the system problems of V_{DD} bounce are typically of less concern than ground bounce. This is because TTL inputs have a greater input high noise margin that input low noise margin. For CMOS driving TTL, the input high noise margin approaches 3.5V, and for CMOS driving CMOS, the input high noise margin approaches 2.5V. In either case, the input high noise margin is 3 to 5 times greater than any expected V_{DD} bounce.

CONTRIBUTING FACTORS OF GROUND BOUNCE

While our circuit diagrams shown above are useful for explaining the origins of ground bounce, they are too idealistic to be used for modeling. In the real world, there are many other variables which affect the actual shape and amplitude of the induced voltage. To develop an accurate model, the resistor must be replaced with a model of the actual transistor. In addition, the period where the transistors are turning on and off would need to be taken into account. Including these variables, plus others, would lead to highly complex differential equations that are nearly impossible to solve except by the most advanced computer programs. Since theoretical analysis of ground bounce is difficult to perform, we will use empirical data to develop an understanding of ground bounce and how it is effected.

There are several factors which affect ground bounce: the number of outputs switching simultaneously; the location of the output pin; the location and type of load on the line; the V_{DD} voltage; the device technology; and the output and ground inductances. Each of these factors play a critical role in the generation of ground bounce.

GROUND BOUNCE DEMONSTRATION BOARD

In order to evaluate ground bounce and the factors which affect it, Fairchild designed a board which allowed side-by-side evaluation of ground bounce under varying conditions.

Figure 3 shows the functional block diagram of the board. A counter generates the changing data lines by counting from 0 to 127. The counter can also be configured to count down from 127 to 0 so that V_{DD} bounce may be evaluated. This changing data is clocked into an AC374 and then passed into both another AC374 and an AC244. This was done for two reasons.

First, the noise generated by the first AC374 represents gound bounce generated by a lightly-loaded circuit. Secondly, being able to choose between either the AC374 or the AC244 to drive the system bus allows us to evaluate both devices under heavy load conditions. The quiet output from these two devices drives a line that is connected to the clock inputs of eight 74 D-type flip-flops and two inverter inputs. Each flip-flop is configured so that if a valid clock was encountered, the Q output will go from a “0” to a “1”; each flip-flop acts as qlitch catcher, detecting any ground bounce noise which violates the flip-flop clock thresholds. Devices from several common logic families are connected to this quiet output so that the effect on different technologies can be evaluated.

The seven other outputs of the AC374 or the AC244 drive a 7-bit data bus. This data bus is loaded with fourteen devices, which represents a typical heavily-loaded system bus and allows us to evaluate ground bounce under these conditions.

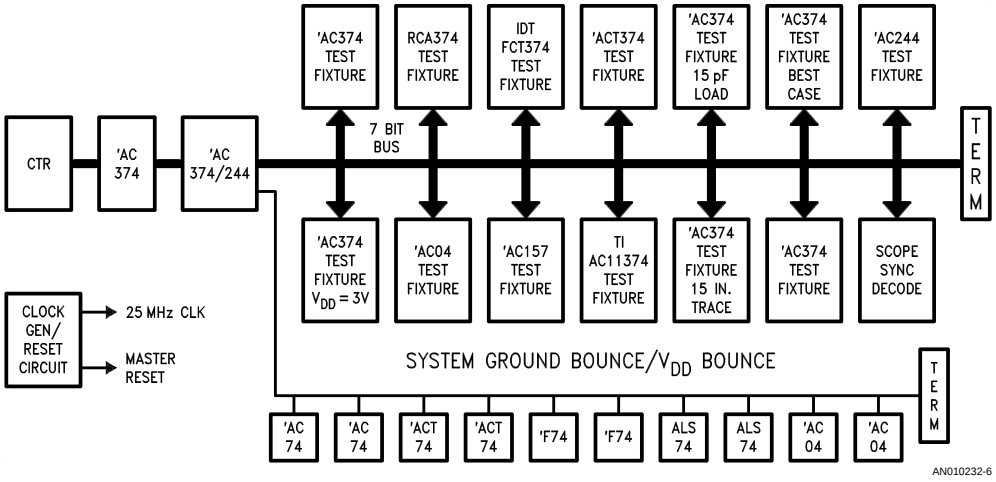

FIGURE 3. Ground Bounce Demonstration Board Block Diagram

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TABLE 1. Critical Signal Statistics

Signal	Length	CO	LO	RO	# Loads	C_L	Termination Type	Termination Type
DATA BUS	30 Inch	107 pF	565 nH	1.3Ω	14	70 pF	PARALLEL	50Ω
CLOCK (Note 1)	28 Inch	103 pF	445 nH	1.0Ω	16	80 pF	THEVENIN	71Ω/120Ω
GROUND BOUNCE	7.5 Inch	30 pF	117 nH	0.2Ω	10	50 pF	AC	26Ω/200Ω

Note 1: Clock generated from seven (7) stage ring oscillator ('AC240)—approximately 25 MHz

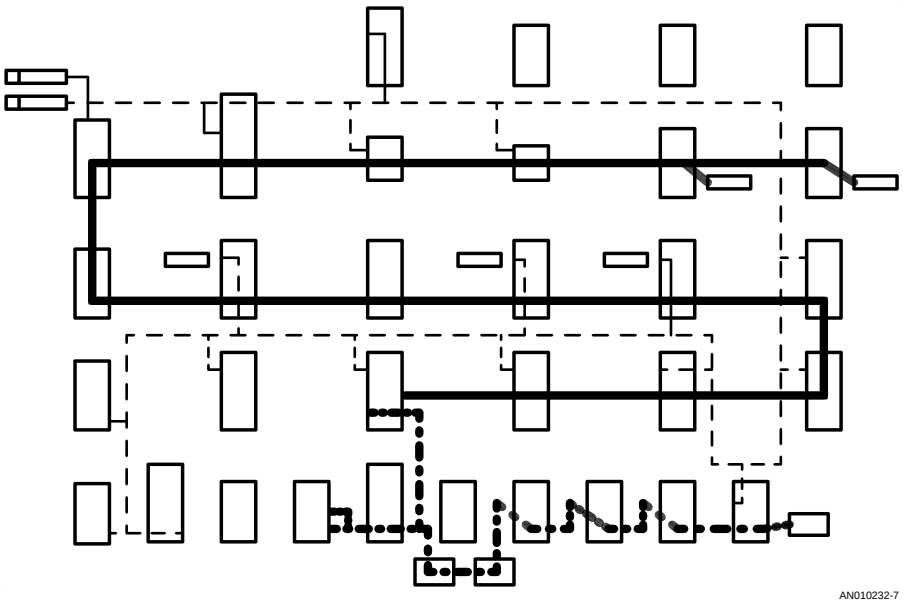

FIGURE 4. Critical Signal Paths

Each device on the bus is configured equivalent to a standard test fixture. Conditions such as output loading, load placement, power supply voltage, and quiet output pin location were varied to compare ground bounce under different conditions. Also, some device locations were populated with different device types and devices from other logic families to evaluate ground bounce across technologies.

Table 1 lists the important electrical characteristics for the critical signal paths. *Figure 4* shows the physical layout of the board and the critical paths. This board was used to generate the data and waveforms presented in this application note unless otherwise noted.

LEAD INDUCTANCE

The impact of the ground inductance on ground bounce seems to be obvious. For a given dI/dt value, the greater the inductance, the greater the ground bounce. While this would imply that reducing the ground inductance should reduce the ground bounce, this is not always the case. The explanation is fairly straightforward.

Ground bounce tends to limit the available AC current in CMOS outputs by reducing the voltage across the output impedance, and therefore, reduces the current that will flow. When the ground lead inductance is reduced, a corresponding increase in the output edge rate of the device occurs. This is due to the fact that by reducing the inductance in the ground lead we have increased the available AC current. This greater dI/dt tends to reduce any improvement that the reduced ground inductance may have generated.

Fairchild tested FACT to investigate the effect of ground inductance on ground bounce. This was accomplished by assembling die from the same manufacturing lot in plastic DIPs; some were assembled using the standard pinout and some were assembled with the ground and power pads connected to the center pins. When the data was analyzed, it was found that the die assembled with center pin V_{DD} and ground averaged approximately 10%–15% less ground bounce than the die assembled with the standard pinouts. Along with the small reduction in ground bounce, they also exhibited somewhat faster edge rates with corresponding decreases in propagation delays.

OTHER PACKAGES

The inductance in the ground lead is not the only inductance in the package; all of the output pins have an associated inductance. The inductances in the outputs also contribute to

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ground bounce, especially any oscillatory effects. While just reducing the ground or V_{DD} does not significantly reduce ground bounce, reducing the inductance in both the power leads and the outputs does reduce ground bounce.

Figure 5 outlines the effect that packaging has on ground bounce. In order to make the comparison as valid as possible, die from the same wafer were used. This was necessary because the effect of process variations on ground bounce is greater than the effect of packaging. It can be seen that packages with smaller power and signal lead inductances tend to reduce ground bounce. It is important to note that the difference between CDIP and LCC package ground lead inductance is approximately one order of magnitude (20 nH versus 2 nH), yet the difference in ground bounce is less than 35%.

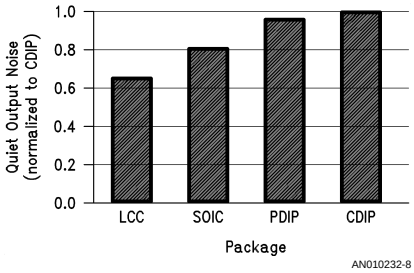

FIGURE 5. Noise vs Package Configuration

Reducing the ground lead inductance is not "the" solution to ground bounce problems. While a small reduction in ground bounce can be realized, additional problems, like increased crosstalk, may occur. A better solution is to reduce the inductance in all leads. Smaller packages, such as SOIC and LCC/PLCC packages, do reduce ground bounce over both standard and center-V_{DD}/ground-pinned DIP packages.

NUMBER OF OUTPUTS SWITCHING

The number of outputs switching simultaneously affects the amplitude of ground bounce. For a simple model, treat the output impedances of each active output as resistors and inductors in parallel. For resistors of equal value in parallel, the formula for the net resistance is R/n, where R is the output impedance of each transistor, and n is the number of resistors. Therefore, as more outputs switch at the same time, the output resistance is reduced and more ground bounce will be generated.

Again, it is very difficult to model this effect so we will rely on empirical results for our analysis. *Figure 6* illustrates the effect of increasing the number of outputs switching at the same time. We can see that as the number goes up, the amplitude and duration of the ground bounce pulse also increases. Therefore, devices that have fewer outputs will have less ground bounce.

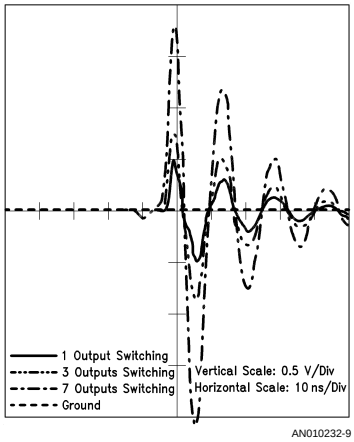

FIGURE 6. Number of Outputs Switching

Figure 7 shows the ground bounce generated by an AC157 when three of the four outputs are switching with standard test loads. Here we see only 475 mV of noise on the worst-case pin (pin furthest from the ground pin). This amplitude of ground bounce is not what we would expect in an actual system. As we will discuss later, a test fixture lumped load creates much more ground bounce than distributed system loads.

OUTPUT LOAD

The type and value of the output loading is one of the major variables that affect the amplitude of the ground bounce. *Figures 8, 9* and *Figure 10* show the effects of varying the load capacitance in a standard test fixture.

In *Figure 8*, the ground bounce amplitude peaks for a load capacitance of approximately 60–70 pF, and then drops off as the capacitance is increased. This drop off is caused by the filtering effect of the larger capacitors.

For *Figure 9*, only the load capacitors on the active outputs were varied. The load on the quiet output was maintained at 50 pF. The amplitude of the ground bounce amplitude increased with increased capacitive loading. However, the slope of the curve drops off as the capacitance increases.

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This is due to the amount of energy that is discharged from the capacitor during the time that the output transistor is turning on.

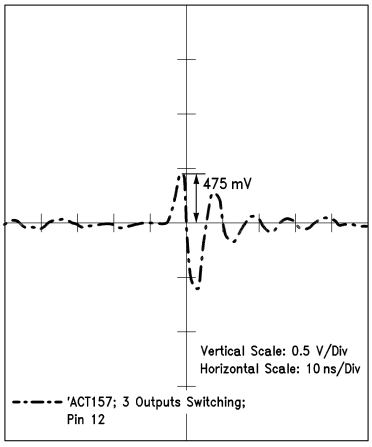
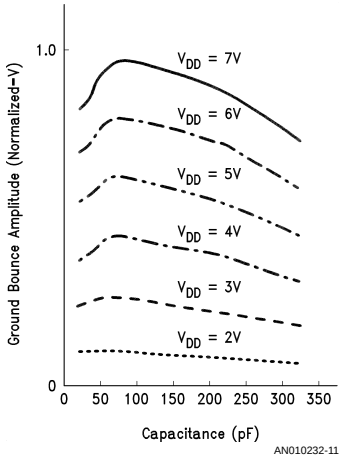


FIGURE 7. AC157 Quiet Output Noise

Smaller capacitors contain less energy than larger capacitors, and therefore, a larger change in the voltage across them will occur during the time that the output is turning on. Because of this, the size of the capacitance tends to limit the maximum amount of current sinking throughout the output and therefore, the amount of ground bounce. Larger capacitors, however, do not experience such a large change in voltage as the outputs turn on. For very large capacitances, there is almost no change in the voltage across them, and they behave much like a power supply. Under these conditions, the maximum amount of current that will sink through the outputs is limited by the outputs themselves. Increasing the capacitance does not increase the current and therefore, does not increase the ground bounce.

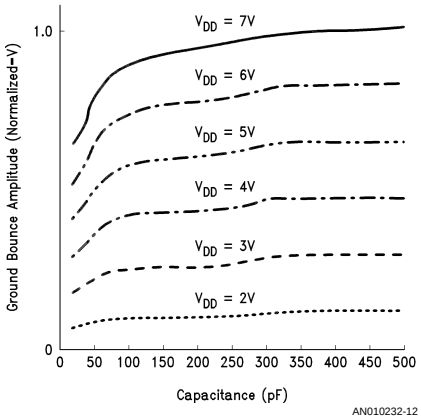
Figure 10 shows the effect of varying only the capacitive loading on the active output. Here, the filtering effect of the load can be observed clearly. As the load capacitance is increased, it filters the signal and reduces the amplitude of the ground bounce.

Because they generate more AC current during switching, capacitive loads tend to generate more ground bounce noise than resistive loads. Fortunately, most actual PCB traces will be long enough so that they react like an impedance and not lumped capacitive loads.



Quiet Output Switching Using AC241
7 Outputs Driving Lumped Capacitive Loads
Monitoring Pin 18.

FIGURE 8. Quiet Output Noise vs Capacitive Loading



Quiet Output Switching with AC241
7 Outputs Driving Lumped Capacitive Loads
Monitoring Pin 18

FIGURE 9. Fixed Quiet Load

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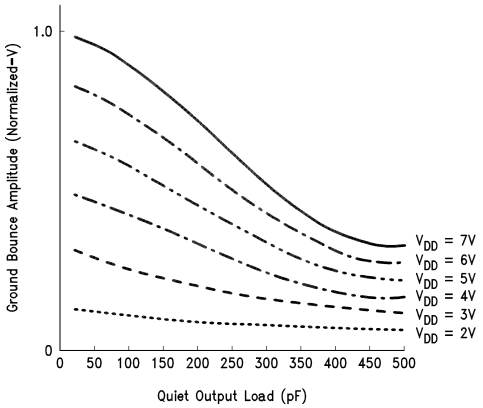
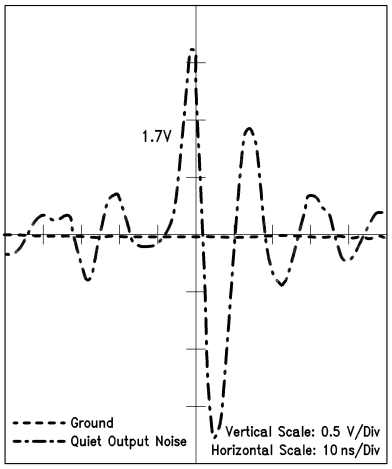


Ground Bounce Varying Quiet Output Load Only
Other 7 Loads are Standard 500Ω/50 pF

FIGURE 10. Fixed Active Load

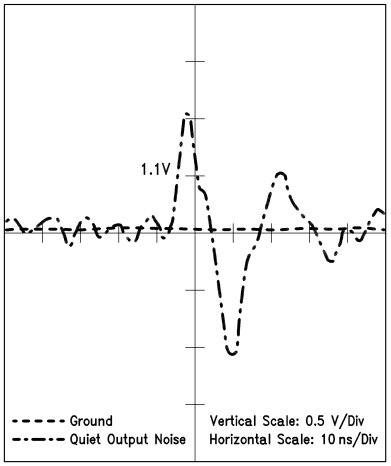
Figure 11 displays ground bounce when the device is loaded with standard 50 pF/500Ω test loads. Each load was connected directly to the output pin. Under these conditions, which are considered worst case, the measured ground bounce amplitude was 1.7V.



7 Outputs Switching V_{DD} = 5V
C_L = 50 pF
Worst-Case Output Pin

FIGURE 11. Standard Test Fixture

Figure 12 illustrates what happens when the test load is moved away from the device output. A standard test load was connected to the output via 15 inches of circuit trace. The amplitude of the ground bounce was reduced to 1.1V. While this loading is closer to an actual system trace than a test load, it still generates more ground bounce noise because of the lumped load that is still on the line.



7 Outputs Switching V_{DD} = 5V
C_L = 50 pF
Worst-Case Output Pin
15" PCB Trace Separating Load from Device

FIGURE 12. Test Fixture Emulating Transmission Line Effect

Figure 13 shows the ground bounce when the load capacitance is reduced to 5 pF. The ground bounce decreased to 1.3V. This circuit represents a short, lightly loaded line.

Figure 14 and *Figure 15* depict the ground bounce generated by the AC374 and AC244 driving the data bus on the board. This bus is over 30 inches long and has over 200 pF of capacitance load. The AC374 only generated 600 mV of ground bounce while the AC244 generated 500 mV. This circuit represents a typical system trace. These figures show the expected amplitudes of ground bounce in an actual system. *Figure 16* shows the ground bounce which was measured on a commercially available personal computer motherboard after a F244 was removed and replaced with an ACT244. For these results, the host processor was removed, and the inputs to the ACT244 were connected to the board clock source. The logic diagram for this line is represented in *Figure 17*. An address bus driver was chosen because of the length of the line and the number of loads on it. Here, the ground bounce amplitude was 1.1V. We can see that this signal line is connected to devices of many different technologies and functions, including LS and memory prod-

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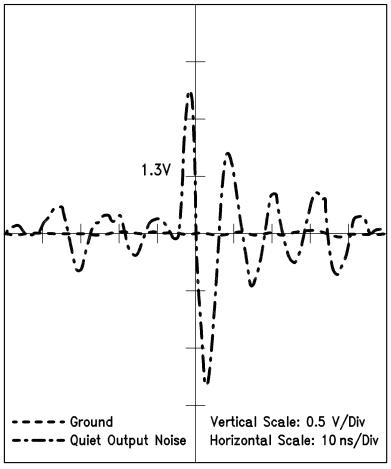
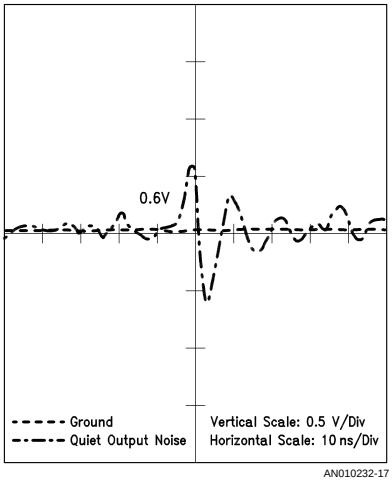
ucts. After the host processor was replaced, the system exhibited no performance degradation due to the device replacement.



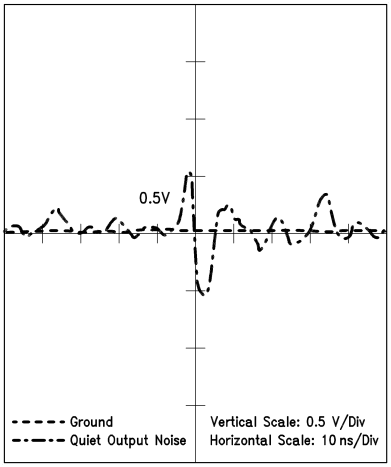
7 Outputs Switching V_{DD} = 5V
C_L = 5 pF
Worst-Case Output Pin
Open Circuit Output (5 pF Parasitic Capacitance)

FIGURE 13. Reduced Output Loading



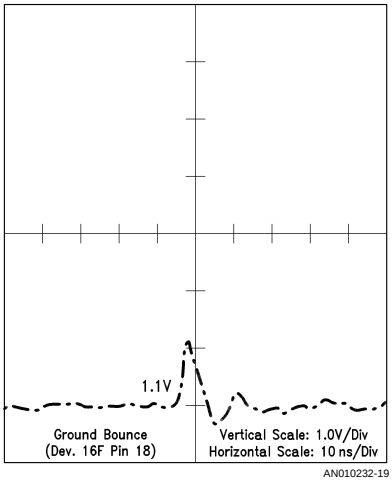
7 Outputs Switching V_{DD} = 5V
C_L = 50 pF
Worst-Case Output Pin;
Ten Loads on Quiet Output Heavy Load

FIGURE 14. System Quiet Output Noise—AC374



7 Outputs Switching V_{DD} = 5V
C_L = 50 pF
Worst-Case Output Pin;
Ten Loads on Quiet Output Heavy Load

FIGURE 15. System Quiet Output Noise—AC244



7 Outputs Switching V_{DD} = 5V
C_L = 50 pF
Worst-Case Output Pin
AC244 Driving 10 Distributed Loads on an Unterminated Address Bus Personal Computer Application

FIGURE 16. Quiet Output Noise in Personal Computer Application

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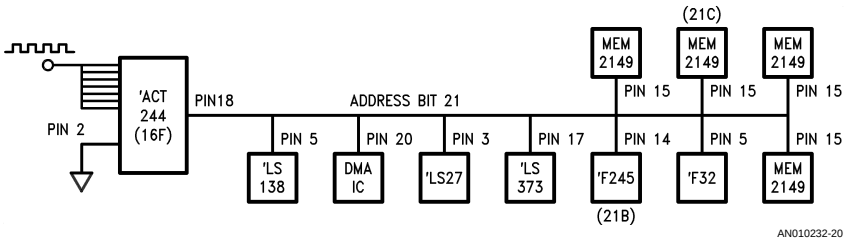
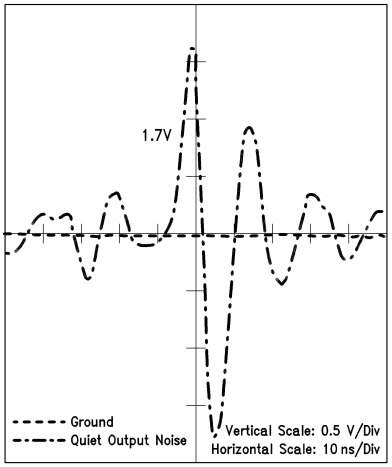


- Commercial PC Address Bus
- No Termination Resistors
- Approximately 50 pF Capacitance Loading
- Replaced F244 with ACT244
- With 7 Outputs Switching, Quiet Output Noise = 1.1V

FIGURE 17. PC Circuit Diagram

It can be seen from the previous figures that the type and location of the output loads have a major effect on ground bounce. It is also obvious that standard test loads generate the most ground bounce. Even reducing the capacitive load, or moving it away from the output still generates more noise than a typical application.

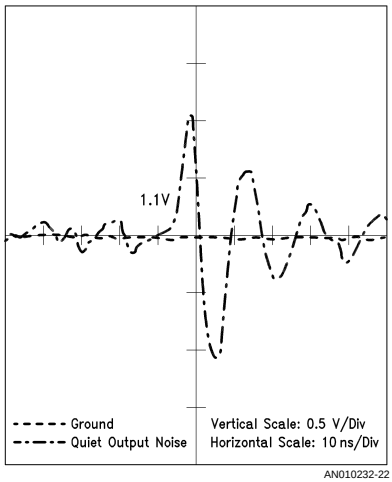


7 Output Switching V_{DD} = 5V
C_L = 50 pF
Standard Test Setup

**FIGURE 18. Quiet Output Noise—
Worst-Case Output Pin**

OUTPUT PIN LOCATION

The location of the output pin with respect to the device ground also affects the magnitude of ground bounce. Tests have shown that outputs located closer to the ground lead generally have 30% to 50% less noise than pins further away. The effects of pin location are portrayed in *Figure 18* and *Figure 19*. *Figure 18* shows the ground bounce on the worst-case pin, which is the one farthest away from ground. *Figure 19* shows the ground bounce on the best-case pin, the one closest to ground. By choosing outputs close to ground, the amount of ground bounce may be reduced by nearly half.



7 Outputs Switching V_{DD} = 5V
C_L = 50 pF

**FIGURE 19. Quiet Output Noise—
Best-Case Output Pin (Pin 9)**

POWER SUPPLY VOLTAGE EFFECTS

The value of V_{DD} also affects the amplitude of the ground bounce. By reducing the V_{DD} level, not only is the output voltage swing reduced, but also the amount of current that the output can deliver. Both of these tend to reduce ground bounce.

Figure 20 tabulates the results of varying both V_{DD} and load capacitance. All of these numbers were taken on a standard test fixture. Note that while the amplitude of the ground bounce changes linearly with voltage, it is not merely the ra-

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tio of the voltage levels. Reducing the V_{DD} by 40% (from 5.0V to 3.0V) reduces the ground bounce by almost 60%. Since the amplitude of the ground bounce decreases faster than the input threshold, there is a net gain in the noise margin.

Figure 21 represents the same results taken on the ground bounce demo board. The ground bounce was measured with V_{DD} = 3.0V. The amount of ground bounce was reduced to 800 mV, even with standard test loads. It should be pointed out that ACXXX devices can be used in a 5V TTL system with a V_{DD} of 3.3V ±0.3V. Under these conditions, the outputs will still drive an incident wave on a 75Ω transmission line for the commercial temperature range and 100Ω for the military temperature range. With V_{DD} equal to 3.3V, FACT ACXXX devices have TTL-compatible inputs and outputs.

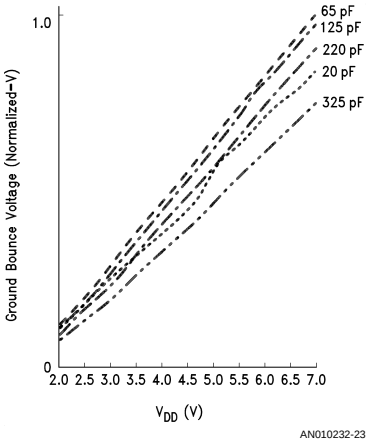


FIGURE 20. Quiet Output Noise vs Power Supply

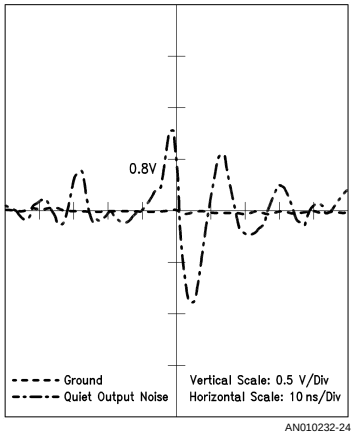
TEST FIXTURES VS REAL SYSTEMS

Because ground bounce is so dependent upon the load the device is driving, it has proven to be one characteristic of CMOS devices that does not correlate well between results taken on standard test fixtures and results seen in actual systems. This occurs for several reasons. First, the AC loading presented by standard text fixtures is not the same as the AC loading generated by a system load, and second, the standard test load creates a LCR tank circuit that tends to oscillate during edge transitions.

For these reasons, ground bounce data taken on test fixtures is useful for comparative analysis, but is not valid for predicting actual system performance.

AC LOADING EFFECTS

Standard text fixtures use 50 pF of capacitance and 500Ω of resistance to simulate a "typical load," as shown in *Figure 22*. It is possible to achieve good correlation between propagation delay data taken using these test loads and data taken in real systems. Unfortunately, this is not true for ground bounce. While this lumped load testing was adequate for older, slower technologies, it is not as useful for the newer, faster logic families. As edge rates go up, more and more circuit traces react like transmission lines, not lumped loads. For devices having edge rates of approximately 3 ns, traces longer than 6–8 inches will exhibit transmission line characteristics and cannot be treated as lumped loads.



7 Outputs Switching V_{DD} = 5V
C_L = 50 pF
Worst-Case Output Pin

FIGURE 21. Quiet Output Noise—V_{DD} = 3.0V

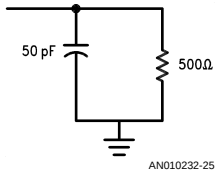


FIGURE 22. Standard Test Load

Figure 23 and *Figure 24* are models of a capacitive load and a transmission line load, respectively. In *Figure 23*, we replace the capacitor with a power supply. This simulates our circuit at the time when the output transistor has just turned on, and the full capacitor voltage is applied across the device. In *Figure 24*, the transmission line is replaced with a resistor to the power supply. This simulates the AC characteristics of the transmission line.

Comparing the two figures, we notice that while the capacitive load applies the full voltage directly to the device output, the transmission line acts like an additional resistance between the voltage and the device output. Clearly, one would expect more current to flow with the capacitive load than with the resistive load. Since the output transistor turns on just as fast in both cases, the capacitive load will create a greater dI/dt, causing more voltage to be induced across the ground lead inductance. Because of this, standard test fixtures tend to generate two to three times more ground bounce noise

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than system printed circuit traces. This is still true for traces that may have more capacitance than the 50 pF lumped load used in standard test fixtures.

LCR TANK EFFECTS

Referring back to *Figure 1a*, notice the LCR tank circuit that is formed by the load capacitance, parasitic inductances and output resistance. Imagine each edge transition as a single impulse into this tank circuit; it would be expected to oscillate. Theoretically, the frequency of the oscillation should be somewhere in the range around 1.3 GHz. Typically, oscillations are observed in the frequency range of 100 MHz to 200 MHz. There are several reasons for this discrepancy.

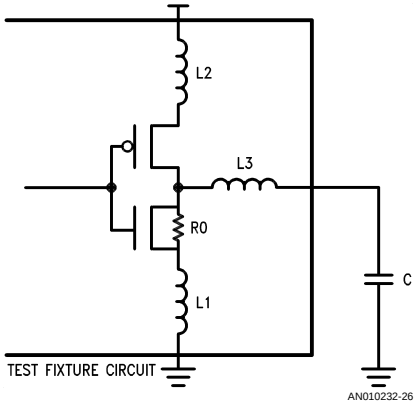
The output transistor does not behave like a pure resistance. The transistor tends to limit the available current to less than 160 mA to 180 mA. Additionally, there are other parasitic elements associated with the output transistor affecting the frequency of oscillation.

Because most circuit traces react like impedances and not capacitances, this type of oscillation is not seen when FACT devices drive typical circuit traces.

Figures 22, 23 and *Figure 24* highlight the differences between ground bounce in a standard test fixture and in a comparable PCB trace. The results of the test fixture *Figure 25* are much greater than the results of the PCB circuit trace *Figure 26*. This is due to the greater current requirements caused by the lumped capacitive load versus a distributed load.

The difference in oscillation between a standard test fixture and a typical circuit trace is also shown. Even though the circuit trace has more capacitance than the test fixture, it is not lumped at the output, but distributed along the circuit trace.

For these reasons, ground bounce data taken on test fixtures is useful for comparative analysis, but is not valid for predicting actual system performance.



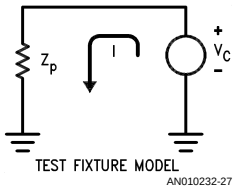
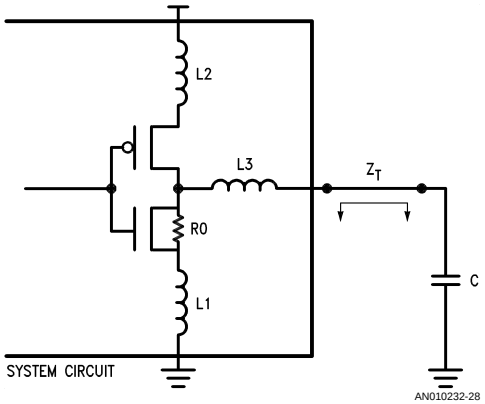


FIGURE 23. Test Fixture



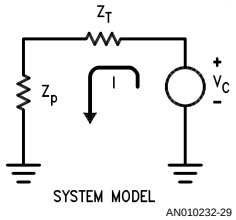


FIGURE 24. System Models

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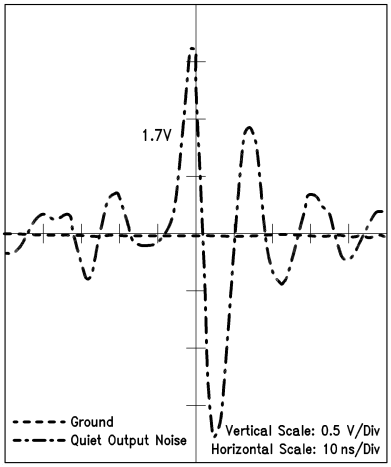
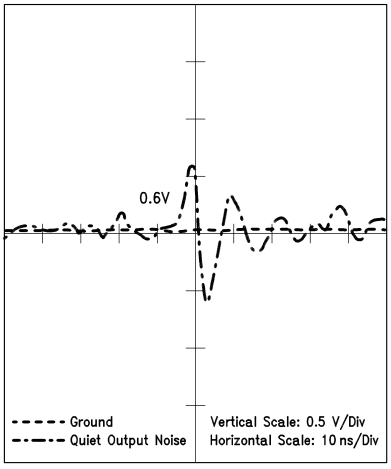


7 Outputs Switching V_{DD} = 5V C_L = 50 pF
Worst Case Output Pin; Ten Loads on Quiet Output

FIGURE 25. Quiet Output—Standard Test Fixture



7 Outputs Switching V_{DD} = 5V; Heavy Load
Worst-Case Output Pin; Ten Loads on Quiet Output

FIGURE 26. Quiet Output Noise—System Bus

MANIFESTATIONS OF GROUND BOUNCE

The problems associated with ground bounce occur because the induced voltage across the ground leads creates a voltage differential between the external system ground and the internal device ground. This voltage affects both inputs and outputs, although differently.

The difference between the external and internal grounds must be taken into account to arrive at the actual input threshold. Noise on either the internal ground or V_{DD} will cause the input thresholds to change. CMOS input thresholds are generally 50% of the voltage across the input structure, i.e., if V_{DD} is 5.0V, then the input threshold will be 2.5V.

Now, if the ground bounces positively 1.0V, the net voltage across the input structure will be reduced to 4.0V. This will cause the input threshold to shift up to 3.0V (1.0V of ground rise + 50% x 4.0V). Conversely, if the ground bounces negatively 1.0V, the input threshold will drop down to 2.0V (−1.0V + 50% x 6.0V). If during this time a quiet input is held between 2.0V and 3.0V, the input structure will detect a change of state.

Regarding the outputs, the effect is somewhat different. Any output that is LOW is essentially tied to the internal ground through a very low impedance: approximately 10–12Ω. Therefore, any output will tend to follow the internal ground as it shifts with respect to the external ground. This causes any LOW outputs to also shift with respect to external ground.

There are four predominant manifestations of ground bounce which we will discuss: 1) altered device states, where a device assumes a state that is not intended or expected, 2) undershoot noise on active signals, 3) propagation delay degradation, and 4) noise on quiet (static) outputs.

ALTERED DEVICE STATES

Of these four symptoms, the most critical is altered device states. Altered device states occur when a device assumes a state that is not intended or expected by the system designer. The results can range from glitches on the outputs to permanently-altered data in registers or counters. Ground bounce can cause these types of problems when it is great enough to cause an external signal to be sensed incorrectly in the device.

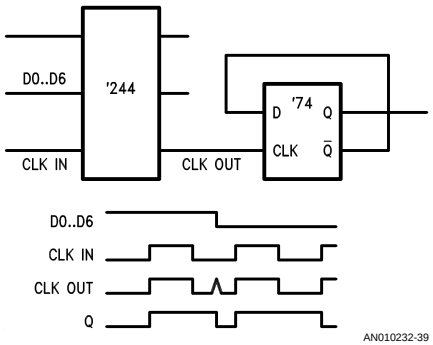


FIGURE 27. Example of Ground Bounce

In CMOS devices, the input thresholds are generally a percentage of the voltage across the input structure. Generally, the input levels are 50% for CMOS level inputs and 30% for TTL-level inputs. As the internal ground and power levels shift with respect to the external power and ground planes, the input thresholds will also shift. If the shift is great enough to cause the input threshold to go above an external HIGH signal (so that the input signal looks LOW) or below an external LOW signal (so that the input looks HIGH), the input will detect a change of state. Depending upon the input type, several results can occur.

If the input is a synchronous one, such as the data input into a D-type flip-flop, then the device should not be affected. If the input is combinatorial, or the data input to a transparent latch, the output may glitch.

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The effects may be more damaging if the input is asynchronous, such as a clock, preset, set, load, or clear. With these inputs, data in the internal counters or registers may be corrupted. Most likely, this type of data corruption can usually cause a system to fail, or generate invalid results.

FACT devices are characterized during initial device evaluation to ensure that the device will not exhibit this problem.

PROPAGATION DELAY DEGRADATION

Propagation delay degradation is a phenomenon familiar to most system designers. As more than one output on a single device is switched, the propagation delay, as measured to the input threshold level, will become longer. To understand how this happens with CMOS devices, consider *Figure 28*; any voltage developed across the inductor L1 will reduce the voltage across the output impedance R1. This, in turn reduces the current through R1. Since the rate of voltage change across the load capacitance is directly related to the current available, a decrease in current reduces the rate at which the output voltage changes, i.e., the edge rate slows down. This, in turn, slows down the propagation delay because more time is required for the output to go from one rail to the input threshold. As additional outputs are switching simultaneously, the voltage across the inductor increases, and the current available to charge or discharge the load capacitance will be less.

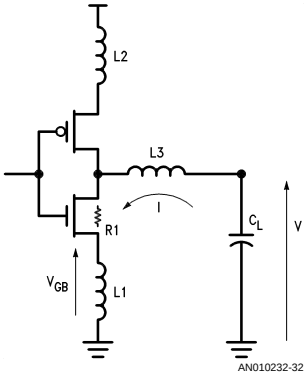

FIGURE 28. Output Model

Figure 29 illustrates the effects of multiple output switching on the propagation delay of a FACT device. Here we see that as more outputs switch, the edge rate of those outputs drops off.

While it is not possible to test this type of parameter in an ATE environment, National understands its importance to system designers. Since this type of measurement can be made in a bench environment, FACT devices are evaluated during initial device characterization to insure that this propagation delay degradation is less than 250 ps per additional output switched.

UNDERSHOOT ON ACTIVE SIGNALS

Undershoot noise on active signals is generally created by impedance mismatches in transmission lines. Yet, it can also be created by ground bounce. *Figure 30* shows the voltage that is generated across the inductor during the edge transition. While at the beginning of the transition the ground bounce is positive, at the end it is negative. This is due to the currents turning off as the output reaches the end of its voltage swing.

Unfortunately, the negative ground bounce occurs when the output is finishing its transition. The output will follow the internal ground as a quiet output would. This results in the output undershooting and then returning to ground.

Undershoot amplitudes are generally slightly less than the associated ground bounce. This undershoot noise will generally not be a problem because most standard logic families have input structures, such as clamp diodes, that tend to damp it out. However, some specialized devices, exemplified by dynamic RAMs, may be sensitive to undershoots greater than −2.0V.

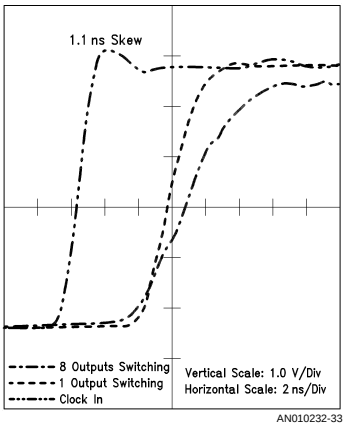

FIGURE 29. Propagation Delay vs Number of Outputs Switching

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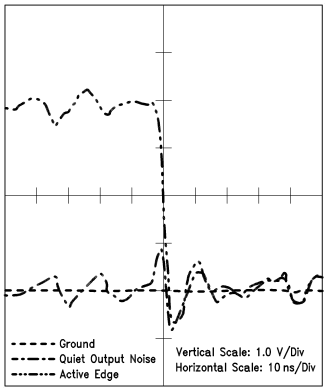

FIGURE 30. Quiet Output Noise Concurrent with Active Edge

QUIET OUTPUT NOISE

Quiet, or static, output noise is usually the symptom of ground bounce that is first noticed by system designers. As pointed out earlier, quiet output noise occurs because LOW outputs tend to follow internal ground. If there is a shift between the external and internal grounds, it will appear as noise on a quiet output. The effects of this noise can range from noise on the output signals to system failure. If the noise is great enough to cross the input threshold on the next device on the line, this next device may react.

The reaction, of course, will depend upon the type of input. If the input is synchronous, the ground bounce noise will not propagate through the input into the device. If the input is combinatorial or asynchronous, output glitches or corrupted counters or registers may result. In order to predict the effects of this noise, it is necessary to consider some typical applications.

As shown earlier, ground bounce amplitude is dependent upon the number of outputs switching. Therefore, devices which have fewer outputs will have less noise. Because of this, our discussions will be limited to octal devices and their applications.

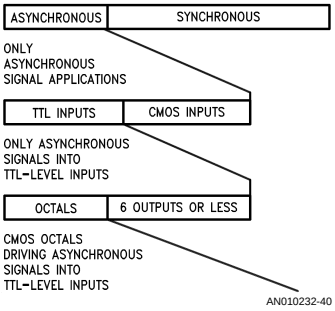

FIGURE 31. Application Segments

SYNCHRONOUS DATA/ADDRESS BUSSES

One of the largest application segments for octal devices is driving/receiving data and address busses. In these bus applications, the receiver is usually synchronous and latches in the data on a clock edge. In *Figure 30*, notice that the quiet output noise exists only when the active outputs are switching. In addition, both quiet and active outputs achieve this stable and valid state within the propagation delay time specified in the FACT Data Book.

During the time that the data or address is latched in (when the data is expected to remain stable and valid) the quiet outputs are as stable and valid as the active outputs. Therefore, valid data will always be clocked in, and in these systems, no additional work is required to achieve maximum system performance and reliability.

ASYNCHRONOUS CONTROL LINES

A much smaller application segment is driving asynchronous signals. Octal devices, like the 240 series, offer eight buffers in a 20-pin package. This feature can be useful to the system designer trying to reduce board size and part count. It is in these applications that problems are most likely to occur. However, there are several factors that work in the designer's favor.

It is important to look at the type of input that is being driven. CMOS-level inputs have much greater low noise margins than TTL-level inputs. Standard CMOS inputs have input

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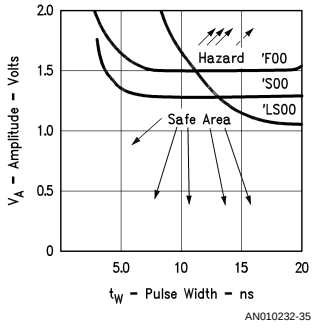
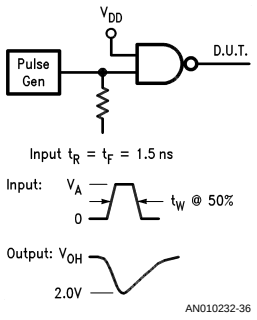
thresholds set to 50% of V_{DD}. This means that if V_{DD} equals 5.0V, there is 2.5V of low noise margin. Test results show that the ground bounce will never be this great in a system. In addition, as noted above, the actual ground bounce noise expected in a real system is less than the AC noise margins of most TTL families.

Finally, it is very important to note that the duration of the ground bounce noise spike is short (tyically 2–3 ns @ 0.8V). Typically, AC noise margins increase with decreasing pulse width. This is more pronounced in slower technologies. *Figure 32* shows the typical low level input noise thresholds of FAST, Schottky, and Low Power Schottky. For pulse width typically seen with ground bounce noise, the AC noise margins of FAST and Schottky approach 2.0V and 1.5V respectively. Even LS devices, which have the lowest input thresholds, have AC noise margins that exceed 2.0V for pulse Low Level Noise Immunity widths as great as 8 ns. For ground bounce type noise pulses, with widths of 2–3 ns, the LS AC thresholds are well above 2.0V.



(a)



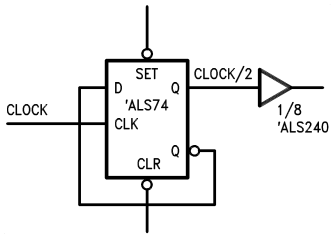
(b)

FIGURE 32. AC Noise Thresholds

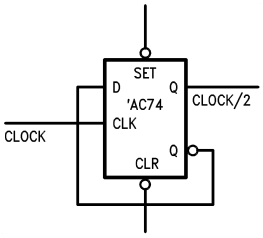
There are also several design techniques under the system designer's control which can be used to minimize ground bounce noise, thereby eliminating ground bounce-induced problems.

The first factor that should be considered, in many cases, is that the need for a buffer can be eliminated. This is due to the fact that all FACT logic devices feature the same 24 mA output stages. A quick example will help to clarify this. For the example, a divide-by-2 clock generator drives a clock onto a large processor board. *Figure 32a* shows the circuit built with ALS devices while *Figure 32b* shows the same circuit built with FACT devices. The difference is obvious: the ALS circuit required a buffer to drive the clock line because the ALS74 does not have enough output drive to drive the line. On the other hand the AC74 has the same drive capability as the AC240, so adding the buffer is redundant. In addition, the output of the AC74 is double buffered to isolate the internal logic from noise on the outputs. Removing an additional propagation delay gains performance advantages besides board space and part count savings. If it is not possible to remove the buffer, the designer can still insure minimum noise on the output. This can be accomplished with several methods, some of which are discussed here.

Board-level timing analysis may show that not all of the outputs can switch at the same time. Under these conditions, the worst-case ground bounce will be reduced *Figure 6*. As mentioned earlier, outputs closer to the ground pin may have up to 50% less noise than outputs further away. Therefore, asynchronous lines should be driven from outputs closer to the device ground pin whenever possible.



(a)



(b)

FIGURE 33. Example Circuits

Some other methods, which may be more difficult to implement, include reducing the power supply voltage or using two power supply voltages. Running the system V_{DD} lower (closer to 4.5V) will reduce the ground bounce noise levels of the CMOS devices while not affecting the input thresholds of the TTL devices. In addition, as we stated earlier, the V_{DD}value for the CMOS devices can be lowered to 3.3V. This reduces the ground bounce by 60% while maintaining TTL-compatible inputs and outputs. For a small number of CMOS devices, a standard zener diode regulated circuit may be used. For larger numbers of devices, a second (3.3V) power plane may be added.

Take a moment to summarize the material covered thus far. While at first glance, the problems associated with quiet output noise may seem to be the most precarious to system designers, there are many issues that affect them. First, a large

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percentage of the octal applications are synchronous busses. In these applications, quiet output noise will not be a problem.

It is the smaller segment of asynchronous applications that are most suspect. Fortunately, only octal devices generate enough ground bounce noise to be of serious concern. Secondly, if the inputs are CMOS, the input noise margins are greater than any ground bounce. If the inputs are TTL, the ground bounce will generally be less than the TTL AC input noise margins. Additionally, designers have several techniques available to reduce the ground bounce. These include: a) use logic devices that provide buffer-type drive capability, thereby eliminating the need for these octal buffers (all FACT devices have the same 24 mA outputs); b) do not have all of the outputs on an octal device switch simultaneously; c) select outputs closer to the ground pin for driving asynchronous inputs, and d) reduce the V_{DD} level. Any or all of these may be used to eliminate the possibility of system failures due to quiet output noise in the small number of octal applications where these problems might occur. Most applications require no special precautions.

The major points of concern regarding ground bounce:

Ground bounce occurs because of the parasitic inductances found in all conductors.

Ground bounce causes shifts in input thresholds and noise on outputs.

There are many factors which affect the amplitude of the ground bounce:

- Number of outputs switching simultaneously: More outputs mean more ground bounce.
- Type of output load: Lumped capacitive loads generate 2 to 3 times more gorund bounce than system traces. Increasing the capacitive load increases ground bounce to approximately 60–70 pF. Beyond 70 pF, ground bounce drops off due to the filtering effect of the load. Moving the load away from the output reduces the ground bounce.
- Location of the output pin: Outputs closer to the ground pin exhibit less ground bounce than those further away.
- Voltage: Lowering V_{DD} reduces the ground bounce.
- Test fixtures: Standard test fixtures generate 30 to 50% more ground bounce than a typical system since they use capacitive loads which increase the AC load and form LCR tank circuits that oscillate.

Ground bounce produces several symptoms:

- Altered device states. FACT logic does not exhibit this symptom.
- Propagation delay degradation. FACT devices are characterized not to degrade more than 250 ps per additional output switching.
- Undershoot on active outputs. The worst-case undershoot will be approximately equal to the worst-case quiet output noise.
- Quiet output noise: FACT's worst case quiet output noise has been measured to be around 500–1100 mV in real system applications.

DESIGN RULES

From this, we can develop a simple set of rules that will protect any system from problems associated with ground bounce. This set of design rules listed below is recommended to ensure reliable system operation by providing the optimum power supply connection to the devices. Most designers will recognize these guidelines. These guidelines are the same ones as those they have been using for years for the advanced bipolar logic families.

Use multi-layer boards with V_{DD} and ground planes, with the device power pins soldered directly to the planes, to insure the lowest power line impedances possible.

Use decoupling capacitors for every device, usually 0.10 µF should be adequate. These capacitors should be located as close to the ground pin as possible.

Avoid using sockets or wirewrap boards.

Avoid connecting capacitors directly to the outputs.

In addition, observing either one of the following rules is sufficient to avoid running into any of the problems associated with ground bounce.

Use caution when driving asynchronous TTL-level inputs from CMOS octal outputs.

Use caution when running control lines (set, reset, load, clock, chip select) which are glitch sensitive through the same device that drive data or address lines.

While it is desirable to avoid the above conditions, there are simple precautions available which can minimize ground bounce noise. These are:

Locate these outputs as close to the ground pin as possible.

Use the lowest V_{DD} as possible or split the power supply.

Use board design practices which reduce any additive noise sources, such as crosstalk, reflections, etc.

Ground bounce is an unwanted noise source that is found in most logic families available today. Due to increased edge rates and voltage swings, ground bounce can be more of a problem with new Advanced CMOS logic families. National, with the vast experience in high performance logic design gained from its leadership position with the FAST family, defined FACT logic so that high performance problems, as exemplified by ground bounce, were minimized while not sacrificing performance. By following the simple design guidelines outlined, designers can use FACT logic to maximize system performance while ensuring their systems are free from the problems associated with ground bounce.

Book
Extract
End

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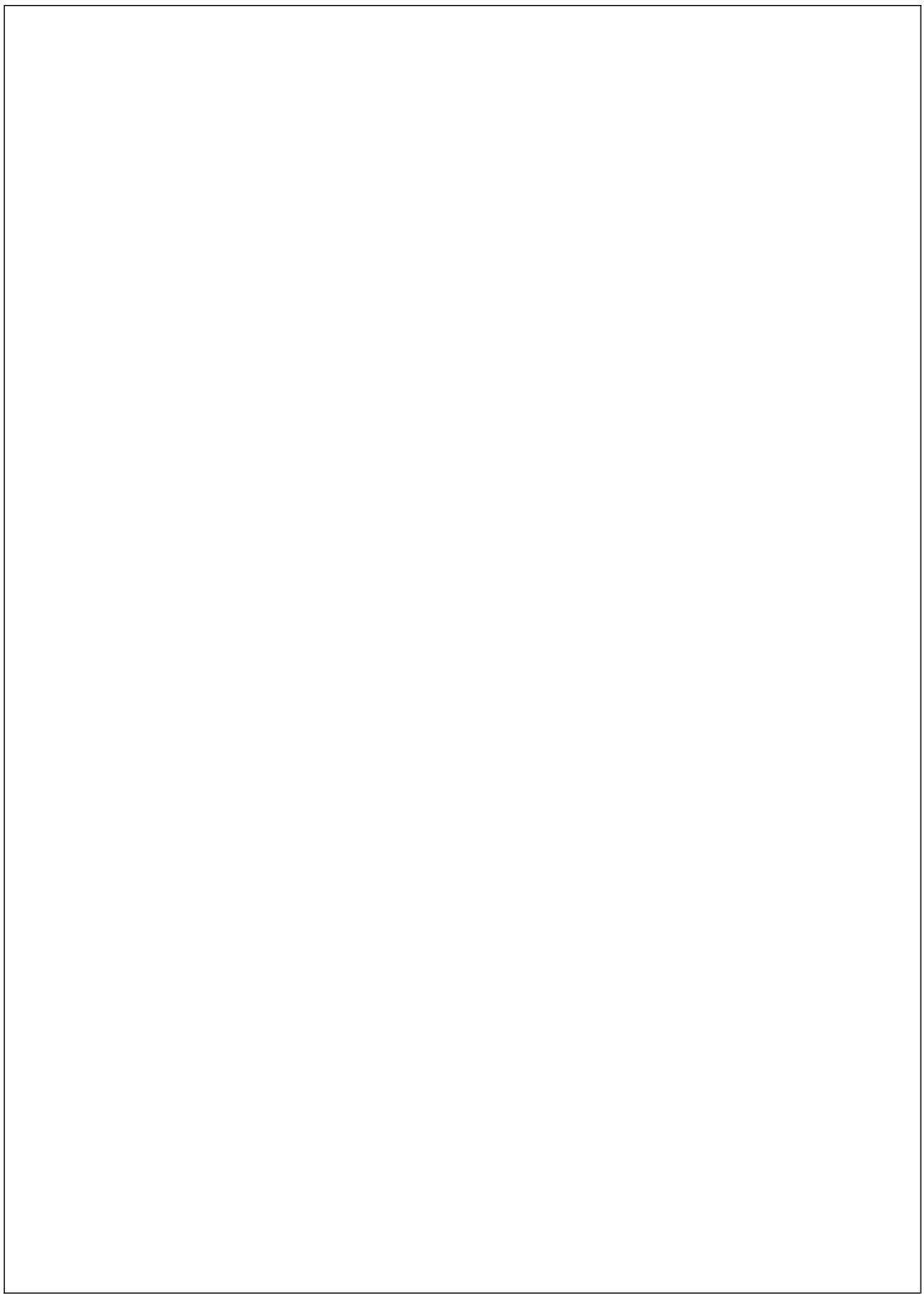

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Fairchild Semiconductor Corporation
Americas
Customer Response Center
Tel: 1-888-522-5372

Fairchild Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 8 141-35-0
English Tel: +44 (0) 1 793-85-68-56
Italy Tel: +39 (0) 2 57 5631

Fairchild Semiconductor Hong Kong Ltd.
13th Floor, Straight Block,
Ocean Centre, 5 Canton Rd.
Tsimshatsui, Kowloon
Hong Kong
Tel: +852 2737-7200
Fax: +852 2314-0061

National Semiconductor Japan Ltd.
Tel: 81-3-5620-6175
Fax: 81-3-5620-6179

www.fairchildsemi.com

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