Transmission-Line Effects Influence High-Speed CMOS

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Unlike low-power, metal-gate CMOS, high-speed 54HC/74HC devices readily drive long cable runs and backplanes. While the family maintains CMOS's traditional noise immunity, you must watch transmission-line effects in such applications.

Because of 54HC/74HC high-speed CMOS's short propagation delays and fast rise and fall times, you must understand its transmission-line behavior when driving lines as short as even a foot or two, whether those lines are coaxial cables, twisted pairs or backplanes. Moreover, the devices' fast edge rates increase the likelihood of crosstalk among interconnecting cables.

Despite the need, however, to take design precautions that minimize adverse effects related to high-speed operation, 54HC/74HC logic—unlike slower metal-gate CMOS—includes many features that suit it to driving transmission lines. For example, its symmetrical push-pull outputs result in stiff logic levels, and its high output drive allows fast bit rates.

Another advantage of high-speed-CMOS designs is that they don't prove to be as difficult as those based on other high-speed logic families. In general, high-speed CMOS doesn't require the detailed attention to pc-board layout and transmission-line characteristics that Schottky TTL or ECL designs do. Furthermore, controlling unwanted reflections is easier in the CMOS designs, because 54HC/74HC devices' electrostatic-protection diodes tend to clamp the reflected voltages to the power-supply levels.

MISMATCHES CREATE REFLECTIONS

Transmission-line effects come into play when signal-line lengths are so long that the signal delay down the line and back becomes longer than the waveform's rise or fall time. Mismatches between the line's characteristic impedance and either the driver's output or the receiver's input impedance create signal-line reflections. These in turn cause overshoot and undershoot, which can reduce noise margins and cause excessive delay. *Figure 1* shows various transmission media and their impedances.

A 54HC/74HC device's output rise and fall times can be as short as 5 ns, and transmission-line effects can become noticeable when lines longer than a foot or two are driven. The length of the signal line at which transmission-line ringing should be considered is:

$$\text{MAXIMUM LINE LENGTH} = \frac{\text{OUTPUT RISE/FALL TIME}}{2(\text{DELAY PER UNIT LENGTH})}$$

The signal delay per unit of line length (t_{PD}) depends on the line's characteristic impedance and the load on the line. For a typical pc-board trace with a groundplane,

$$t_{PD} = 1.017\sqrt{0.47\,\epsilon_R + 0.67}\ \text{ns/ft},$$

where ϵ_R is the relative dielectric constant. Loading the trace with inputs to other gates alters the t_{PD}.

$$t_{PD}\,(\text{ALTERED}) = t_{PD}\sqrt{1 + \frac{C_{IN}}{C_O}},$$

where C_{IN} is the total input capacitance associated with the line, and C_O is the line capacitance per unit of length.

If you know the characteristics of the transmission line, you can use these equations to find the signal-transit time. This time is typically between 1.5 and 2.4 ns/ft for an unloaded line.

In addition to the line's transit time, you need to find its characteristic impedance:

$$Z_O = L_O/C_O,$$

where L_O and C_O are the wire's inductance and capacitance per unit of length. When a 54HC/74HC device drives a transmission line (*Figure 2*), the driver's output looks into the equivalent line impedance. When the output switches, the signal propagated is the result of the voltage divider created by the line and the driver's impedance.

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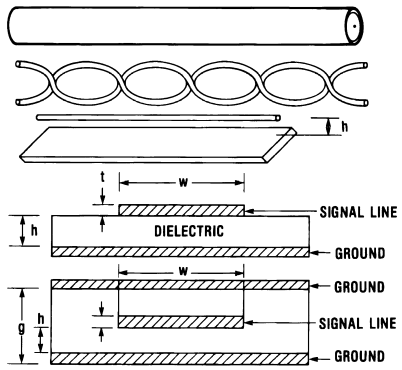

COAXIAL CABLE	$Z_o = 50, 75, 125\Omega$
TWISTED PAIR	$Z_o = 50$ TO 100Ω
WIRE OVER GROUND	$Z_o = \frac{60}{\sqrt{\epsilon_R}} \ln\left(\frac{4h}{d}\right)$ TYPICALLY $Z_o = 120$ TO 200Ω
MICROSTRIPLINE	$Z_o = \frac{87}{\sqrt{\epsilon_R + 1.41}} \ln\left(\frac{5.98}{0.8w + t}\right)$ TYPICALLY $Z_o + 50$ TO 100Ω
STRIPLINE	$Z_o = \frac{60}{\sqrt{\epsilon_R}} \ln\left[\frac{4b}{0.67\pi w(0.8 + \frac{t}{w})}\right]$ $\frac{w}{(b-t)} < 0.35$ AND $t/b < 0.25$ TYPICALLY $Z_o = 30$ TO 80Ω

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FIGURE 1. By using the impedances for various types of signal-transmission lines, you can determine the amount of ringing you'll experience. (Note that ϵ_R is the relative dielectric constant.)

If the line's electrical length is long compared with the signal's rise time, the mismatch of the line and the CMOS input creates a reflection when the signal reaches the other end of the line. The reflection's magnitude depends on the incident signal's voltage (V_{INC}) and the reflection coefficient (p), where

$$\rho = \frac{R_{IN} - Z_O}{R_{IN} + Z_O}.$$

The reflected signal is therefore

$$V_R = V_D (1 + r).$$

HIGH INPUT IMPEDANCE DOUBLES REFLECTION

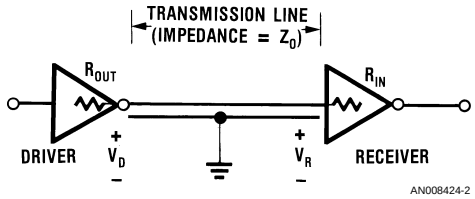

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FIGURE 2. When a high-speed CMOS driver/receiver pair communicates over distances longer than a foot or two, transmission-line effects come into play.

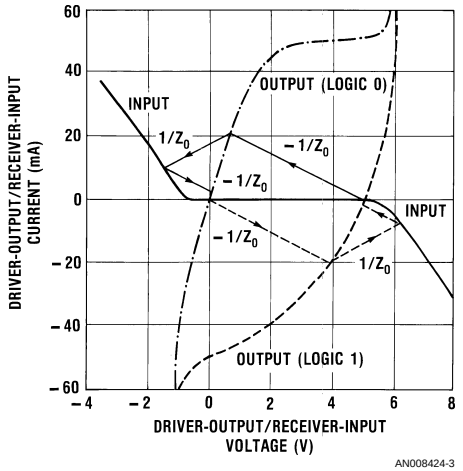

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FIGURE 3. This plot of input and output transfer functions for standard 54HC/74HC high-speed CMOS logic includes the effects of input-protection and parasitic diodes. It provides the basis for a graphic method of determining ringing and overshoot.

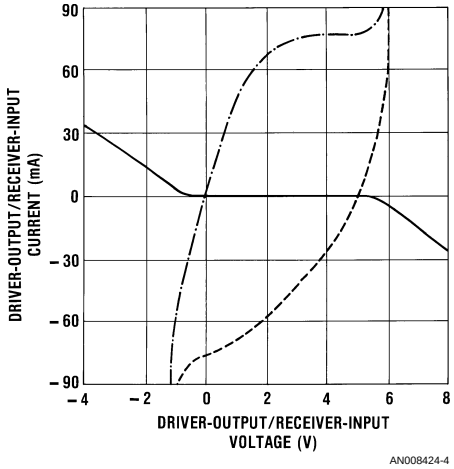


FIGURE 4. Bus-output drivers in the 54HC/74HC high-speed CMOS family exhibit different input and output transfer functions than do the standard parts whose characteristics are shown in *Figure 3*.

Because a 54HC/74HC device's input impedance is high compared with the line's (r = 1.0), the reflected voltage at the receiver doubles. This reflection propagates back to the driver, where another reflection is generated (depending on the driver's output impedance). Typical 54HC/74HC output impedances result in reflection coefficients of −0.3 to −0.7.

A simplified analysis based on the preceding equations, however, fails to take into account nonlinearity in a 54HC/74HC gate's output impedance. Also, the input of a 54HC/74HC gates has diodes to V_{CC} and ground; these diodes clamp the reflected signal as it tries to exceed the supply level.

A load-line graphic technique overcomes these drawbacks. Illustrating the technique, *Figure 3* and *Figure 4* plot the input and output characteristics for a standard and a bus-driver 54HC/74HC IC at V_{CC} = 5V. These plots include the effect of the input and output diodes. With these curves, you can approximately determine the ringing for various line impedances when one 54HC/74HC gates drives another.

An example based on a High-to-Low transition on a 200Ω line illustrates how to use the graphs. Starting at the quiescent 5V, 0A point on the logic-One output's curve (*Figure 3*), draw a load line with a slope of $-1/Z_O$ to the logic-Zero output's curve. The voltage at this intersection is the initial output voltage that drives the line after the transition. Then draw a line with a $+1/Z_O$ slope to the input curve. This intersection yields the signal's voltage, including the reflection, when it reaches the receiver. Next, draw another line back to the logic-Zero output curve. This intersection indicates the voltage at the driver when the reflection returns. This process continues until the zigzag load line converges on the 0V, 0A intersection.

Figure 5 plots the *Figure 3* example's voltages vs propagation delay. *Figure 6* shows real-world waveforms for a 74HC00 device driving another gate through a wire poised above a groundplane (Z_O = 200Ω). Notice that the driver's output level swings further toward the opposite logic level than the graphic method initially predicts, resulting in slightly more-ringing at the receiver as well. This additional ringing is due to either a lower output impedance or a slightly higher line impedance than that used in the paper analysis.

Although line reflections aren't a problem for most designs, you may have to reduce ringing for certain applications, such as those including long cables, backplanes and sensitive circuits that can't tolerate radiated noise and crosstalk. You can use several techniques to reduce ringing. One solution is to use series-terminating resistors (*Figure 7a*). Series termination places a resistor in series with the driver's output to match the output impedance of the driver to that of the line. This procedure eliminates overshoot at the receiver's end of the line but slows down the output signal, and it won't work with buses or backplanes.

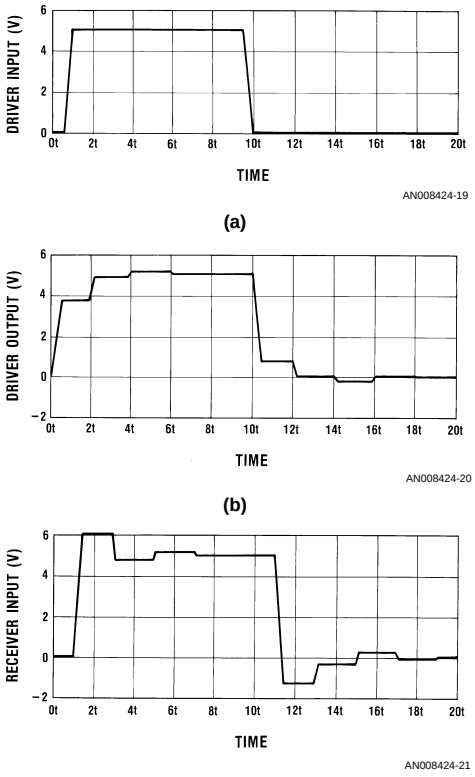


FIGURE 5. Using the plots shown in *Figure 3* and *Figure 4* along with the graphic method described in the text, you can construct the driver (b) and receiver (c) waveforms resulting from an input (a).

PARALLEL TERMINATIONS CAN OVERLOAD CMOS

Parallel termination (*Figure 7 (b)* and *Figure 7 (c)*) connects a resistor at the receiver's end of the line to either V_{CC} or ground or to a voltage divider between V_{CC} and ground. The

resistor value (or the equivalent resistance of the resistor pair) should match the line's impedance. Normally, a system backplane has one termination per signal line. Some very-high-speed buses, however, can include two termination networks at each end of the backplane for each line.

One problem with parallel termination is that the termination consumes large amounts of power, negating the reason for choosing 54HC/74HC devices to begin with. Moreover, because the termination network must match the line's impedance, parallel termination can overload a 54HC/74HC device's outputs and prevent them from driving the bus to a valid logic level.

Consider, for example, a 150Ω TTL bus with a single termination and the equivalent of a 150Ω termination resistor connected to a 3.5V supply. The worst-case output impedance of a 54HC/74HC bus driver is 100Ω. The dc output voltage for the 54HC/74HC driving a TTL bus to a low level would be V_{OUT} = 3.5V (100Ω/250Ω) = 1.2V, which is too high to represent a valid logic-Zero output. You can use such dc-termination schemes only if a 54HC/74HC device can pull the termination network to within 0.5V of the supply rails (HCT parts work between 0.4 and 2.4V).

Aside from such brute-force power considerations, a subtle problem arises from reflections in certain cases. If the line is long enough to exhibit a significant delay down the line, the ability of the receiving logic element to switch on the original incident-wave front becomes important. If the incident wave isn't of the proper magnitude, the receiver must wait for the reflection before sensing the change at its input. The voltage at the receiver equals the driver's output voltage divided across the driver's output impedance and the line's characteristic impedance. 54HC/74HC gates typically have 40 to 50Ω output impedances, so 54HC/74HC receivers switch on the incident-wave transitions if the line impedances are greater than 150Ω typically.

In general, when replacing LS components with 54HC/74HC units, avoid driving buses with a termination network whose equivalent impedance is less than 500Ω (worst case) terminated to V_{CC} or ground, or 250Ω terminated to 3V.

The TTL termination's impedance isn't the only problem involved in substituting 54HC/74HC parts for TTL. For example, consider the voltages that the termination networks are tied to. Usually, TTL termination networks look like their equivalent impedance tied between 2.5 and 3.5V. Consequently, when these TTL buses are in the high-impedance state, they float toward these voltages, causing the 54HC/74HC circuits to draw I_{CC} currents that are large compared with the currents generated when the bus is terminated to V_{CC} or ground. Also note that some logic errors might develop because the 2.5 to 3.5V range is not a valid 54HC/74HC logic level.

Using the termination network shown in *Figure 7 (d)*, which couples the signal to the termination network with a small capacitor, avoids this problem. The capacitor blocks the DC currents while acting as a short circuit during signal transitions. This termination scheme doesn't draw any DC power, although it does draw additional AC (dynamic) power. Furthermore, if the bus goes to a high-impedance state, the termination capacitors hold the bus at the last logic level for a short time (perhaps a millisecond), avoiding excessive I_{CC} currents. If the bus has the potential to float for long periods, you might have to add large-value pull-up resistors to ensure that bus leakages don't cause spurious behavior.

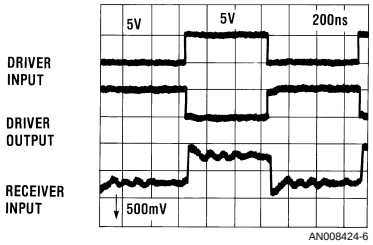


FIGURE 6. A high-speed CMOS device driving another gate through a 28-gauge wire poised above a groundplane (Z_o = 200Ω) exhibits higher ringing and overshoot than predicted in *Figure 5*, thus indicating a lower output impedance or higher line impedance than that used in the prediction.

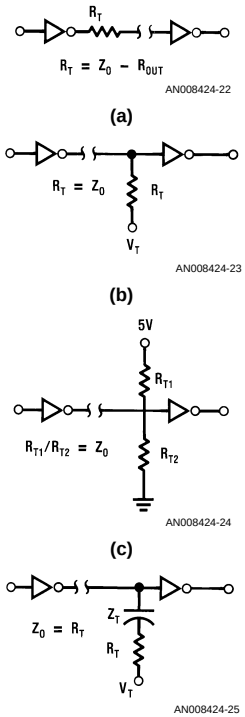


FIGURE 7. The three termination techniques shown here in (a), (b), and (c) work best for conventional TTL. For high-speed CMOS, (d) might provide the best solution.

These considerations apply to 54HC/74HC outputs. 54HC/74HC inputs interface easily to any type of bus or transmission line that meets the 54HC/74HC input-voltage requirements.

Eliminating troublesome reflections only handles problems involving a single transmitter/receiver pair. Seldom, however,

do transmitter/receiver pairs exist in isolation; they more commonly occur in groups, and the possibility of crosstalk always exists. Parasitic mutual inductance and capacitance associated with system interconnections cause crosstalk.

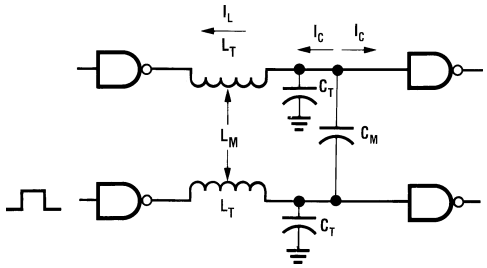


FIGURE 8. Ringing and overshoot from impedance mismatches aren't the only problems you can encounter in applying high-speed CMOS. Parasitic coupling arising from distributed capacitance and inductance of parallel wires or pc-board traces can cause crosstalk.

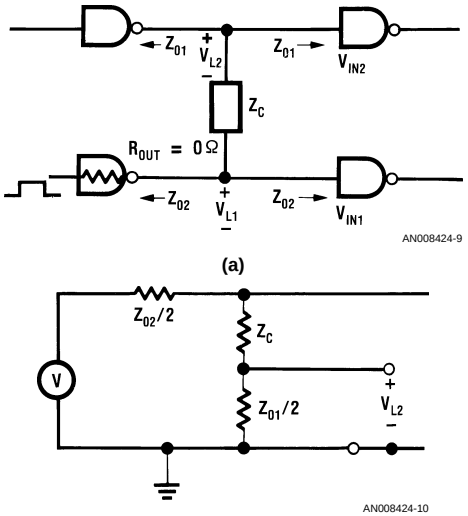


FIGURE 9. This simplified representation (a) of *Figure 8*'s parasitic coupling impedances yields the equivalent circuit shown in (b).

Figure 8 and *Figure 9* illustrate these inductances and capacitances. Their magnitudes depend on the length, spacing, amount of shielding and type of wiring used. Generally, crosstalk isn't necessarily a concern unless two or more signal lines run in parallel over long distances. Even when using long signal runs, 54HC/74HC devices' noise immunity eases the requirements for crosstalk minimization.

Although you can analyze crosstalk by finding the current coupling caused by distributed capacitance and inductance, the simpler approach based on *Figure 9*'s scheme suffices. *Figure 9 (a)*shows two signal lines with an impedance of Z_{O1} and Z_{O2} coupled by Z_C. At the point of coupling, the signal voltage V_{L2} induced into the second line is essentially due to the voltage divider formed by Z_{O1}, Z_{O2} and Z_C (b). The voltage V_{L1} results from V_{OUT} of the first inverter driving the voltage divider formed by the second inverter's R_{OUT} and Z_{O1}. If the driving gate's output impedance is small, then V_{OUT} = V_{LI} = V_{CC} and Z_{O1} = Z_{O2} = Z_O. Then the equivalent impedance model of (b) leads to

$$V_{L2} = \frac{Z_{O2}/2}{Z_C + \left(\frac{Z_{O1}}{2}\right) + \left(\frac{Z_{O2}}{2}\right)} \times V_{OUT} = \frac{1}{2}\frac{Z_O}{Z_C + Z_O} V_{CC}.$$

When the signal reaches the receiver, the reflection causes the signal's level to double, and V_{IN} = 2(V_{L2}).

Qualitatively, you can see that crosstalk increases as Z_C decreases. Z_C in turn decreases with increasing coupling length (decreasing the spacing between the two connectors) and poor shielding. Lowering Z_O decreases crosstalk but not as dramatically as changing Z_C does. Notice that as Z_C becomes small (which indicates a lot of cross coupling), changing Z_O has little effect with respect to reducing crosstalk. However, adding shielding to the cable both lowers Z_O and raises Z_C and consequently proves effective in reducing crosstalk.

Figures *Figure 10*, *Figure 11* and *Figure 12* illustrate crosstalk effects for several conductor configurations. *Figure 10* shows the relative coupling between two pc-board traces alone and also with various guarding schemes. *Figure 11* illustrates oscilloscope traces of a 1-MHz signal in a 2 meter bundled cable with various numbers of wires connected to ground. Notice the dramatic reduction in crosstalk between two wires when a third wire is grounded in the cable. *Figure 12* shows the same schemes for various configurations of wire in a ribbon cable. Here, the lowest crosstalk comes from separating the two signal lines by a ground cable. The most crosstalk occurs when the two cables are adjacent to each other and no other cable is grounded.

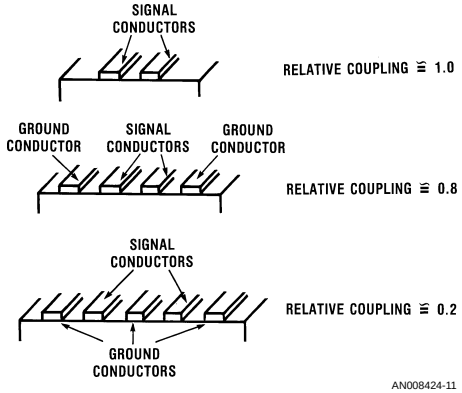
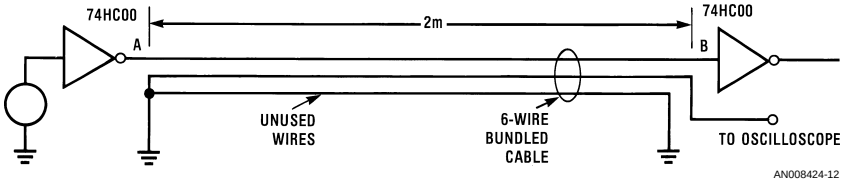
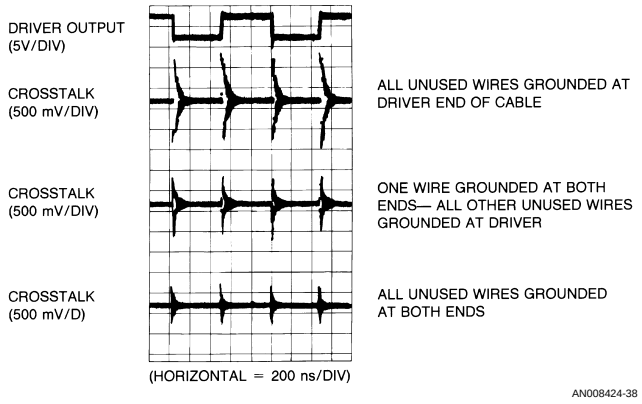


FIGURE 10. Grounding scheme can significantly reduce crosstalk. For example, separating pc-board signal conductors with grounded ones reduces relative coupling from 1 to 0.2.

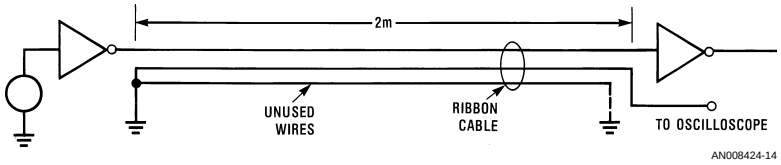


(a)

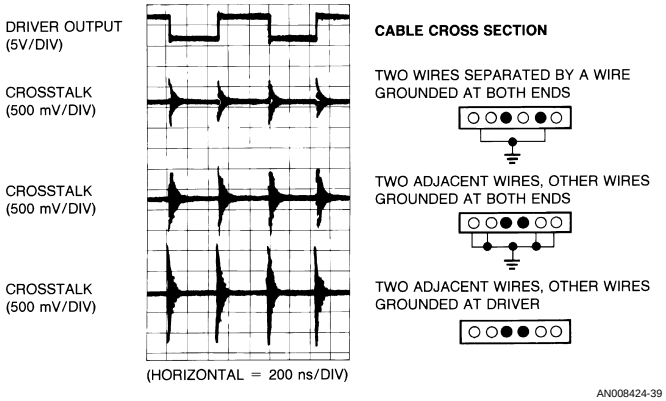


(b)

FIGURE 11. The effectiveness of guarding techniques in reducing crosstalk isn't limited to pc boards, as results based on a 6-wire bundled-cable test circuit illustrate (a). Grounding unused wires at both ends yields the best performance (b).



(a)



(b)

FIGURE 12. To reduce crosstalk between two conductors in a ribbon cable, separating the signal-carrying conductors with ones grounded at both ends proves to be effective.

LOW VOLTAGES INCREASE DELAYS

Although the bulk of the applications for high-speed CMOS involve a 5V power supply, some applications can use 2V—the low end of 54HC/74HC devices' power-supply operating range. At 2V, a 54HC/74HC device has approximately one-third to one-fifth the output drive and about three to five times the circuit delays and transition times of the same ICs powered by 5V supplies. At V_{CC} = 2V, output transition times are about 30 nsec, which tends to ease signal-line routing and termination requirements. Because rise and fall times are so long, reflections and ringing are insignificant. Crosstalk and general signal-line to signal-line noise coupling are also reduced by a factor of three to five, limiting internally generated noise coupling. However, by using a lower supply voltage, the dc noise immunity is approximately halved, and overall immunity to external noise is reduced.

Thus, for 2V designs, transmission-line noise and ringing are essentially eliminated, and crosstalk is reduced by a factor of two (when device noise-immunity reduction is included). Designing with high-speed CMOS at 2V can best be described as almost identical to trying to design with older CMOS logic at 5V.

REFERENCES

1. Blood, W. R. Jr., *MECL System Design Handbook,* Motorola Semiconductor Inc, 1980.

2. Blakeslee, T. R., *Digital Design with Standard MSI and LSI,* 2nd edition, John Wiley and Sons, New York, 1979.

3. *Designing With TTL Integrated Circuits,* Texas Instruments Staff, McGraw Hill, New York, 1971.

4. *MM54HC/74HC High-Speed CMOS Handbook,* Fairchild Semiconductor Corp, 1983.

5. "Fairchild's Process Enhancements Eliminate the CMOS SCR Latchup Problem in 54HC/74HC Logic," Application Note *AN-399* , Fairchild Semiconductor Corp, 1983.

6. "DC Electrical Characteristics of High-Speed CMOS," Application Note *AN-319* , Fairchild Semiconductor Corp, 1983.

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