APPLICATION NOTE

AN165
Integrated operational amplifier theory

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PHILIPS

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INTRODUCTION

The operational amplifier was first introduced in the early 1940s. Primary usage of these vacuum tube forerunners of the ideal gain block was in computational circuits. They were fed back in such a way as to accomplish addition, subtraction, and other mathematical functions.

Expensive and extremely bulky, the operational amplifier found limited use until new technology brought about the integrated version, solving both size and cost drawbacks.

Volumes upon volumes have been and could be written on the subject of op amps. In the interest of brevity, this application note will cover the basic op amp as it is defined, along with test methods and suggestive applications. Also, included is a basic coverage of the feedback theory from which all configurations can be analyzed.

THE PERFECT AMPLIFIER

The ideal operational amplifier possesses several unique characteristics. Since the device will be used as a gain block, the ideal amplifier should have infinite gain. By definition also, the gain block should have an infinite input impedance in order not to draw any power from the driving source. Additionally, the output impedance would be zero in order to supply infinite current to the load being driven. These ideal definitions are illustrated by the ideal amplifier model of Figure 1.

Further desirable attributes would include infinite bandwidth, zero offset voltage, and complete insensitivity to temperature, power supply variations, and common-mode input signals.

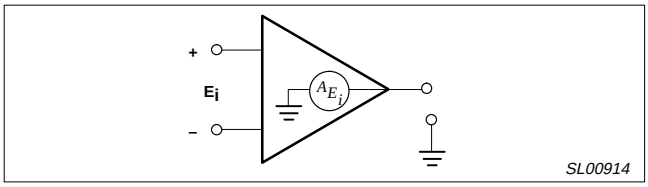

Figure 1. Ideal Operational Amplifier

Keeping these parameters in mind, further contemplation produces two very powerful analysis tools. Since the input impedance is infinite, there will be no current flowing at the amplifier input nodes. In addition, when feedback is employed, the differential input voltage reduces to zero. These two statements are used universally as beginning points for any network analysis and will be explored in detail later on.

THE PRACTICAL AMPLIFIER

Tremendous strides have been made by modern technology with respect to the ideal amplifier. Integrated circuits are coming closer and closer to the ideal gain block. In bipolar devices, for instance, input bias currents are in the pA range for FET input amplifiers while offset voltages have been reduced to less than 1mV in many cases.

Any device has limitations however, and the integrated circuit is no exception. Modern op amps have both voltage and current limitations. Peak-to-peak output voltage, for instance, is generally limited to one or two base-emitter voltage drops below the supply voltage, while output current is internally limited to approximately 25mA. Other limitations such as bandwidth and slew rates are also present, although each generation of devices improves over the previous one.

DEFINITION OF TERMS

Earlier, the ideal operational amplifier was defined. No circuit is ideal, of course, so practical realizations contain some sources of error. Most sources of error are very small and therefore can usually be ignored. It should be noted that some applications require special attention to specific sources of error.

Before the internal circuitry of the op amp is further explored, it would be beneficial to define those parameters commonly referenced.

INPUT OFFSET VOLTAGE

Ideal amplifiers produce 0V out for 0V input. But, since the practical case is not perfect, a small DC voltage will appear at the output, even though no differential voltage is applied. This DC voltage is called the input offset voltage, with the majority of its magnitude being generated by the differential input stage pictured in Figure 2.

An operational amplifier's performance is, in large part, dependent upon the first stage. It is the very high gain of the first stage that amplifies small signal levels to drive remaining circuitry. Coincidentally, the input current, a function of beta, must be as small as possible. Collector current levels are thus made very low in the input stage in order to gain low bias currents. It is this input stage which also determines DC parameters such as offset voltage, since the amplified output of this stage is of sufficient voltage levels to eclipse most subsequent error terms added by the remaining circuitry. Under balanced conditions, the collector currents of Q1 and Q2 are perfectly matched, hence we may say:

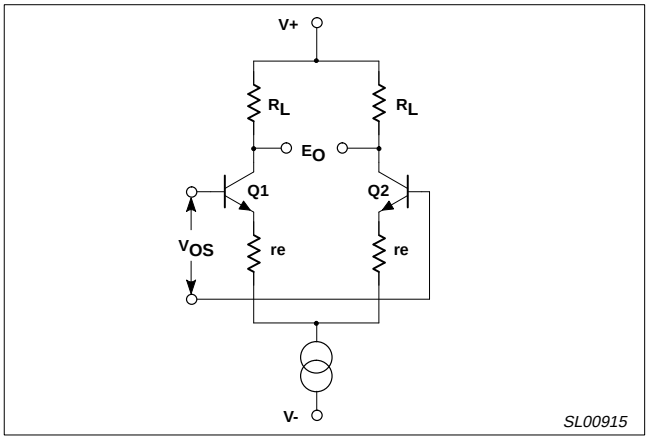

Figure 2. Differential Input Stage

$$E_{OS}=I_{C2}R_L-I_{C1}R_L=0 \quad (1)$$

In practice, small differences in geometries of the base-emitter regions of Q1 and Q2 will cause E_{OS} not to equal 0. Thus, for balance to be restored, a small DC voltage must be added to one V_{BE} or

$$V_{OS}=V_{BE}1-V_{BE}2 \quad (2)$$

where the V_{BE} of the transistor is found by

$$V_{BE} = \frac{kT}{q} \ln\left(\frac{I_E}{I_S}\right) \quad (3)$$

Reference is made to the input when talking of offset voltage. Thus, the classic definition of input offset voltage is

"that differential DC voltage required between inputs of an amplifier to force its output to zero volts.'

Offset voltage becomes a very useful quantity for the designer because many other sources of error can be expressed in terms of V_{OS}. For instance, the error contribution of input bias current can be expressed as offset voltages appearing across the input resistors.

INPUT OFFSET VOLTAGE DRIFT

Another related parameter to offset voltage is V_{OS} drift with temperature. Present-day amplifiers usually possess V_{OS} drift levels in the range of 5μV/°C to 40μV/°C. The magnitude of V_{OS} drift is directly related to the initial offset voltage at room temperature. Amplifiers exhibiting larger initial offset voltages will also possess higher drift rates with temperature. A rule of thumb often applied is that the drift per °C will be 3.3μV for each millivolt of initial offset. Thus, for tighter control of thermal drift, a low offset amplifier would be selected.

INPUT BIAS CURRENT

Referring to Figure 3, it is apparent that the input pins of this op amp are base inputs. They must, therefore, possess a DC current path to ground in order for the input to function. Input bias current, then, is "the DC current required by the inputs of the amplifier to properly drive the first stage.'

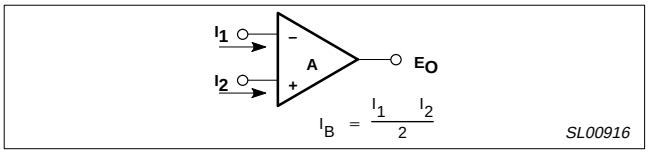

Figure 3. Input Bias Current

The magnitude of I_{BIAS} is calculated as the average of both currents flowing into the inputs and is calculated from

$$I_B = \frac{I_1 \quad I_2}{2} \tag{4}$$

Bias current requirements are made as small as possible by using high beta input transistors and very low collector currents in the first stage. The trade-off for bias current is lower stage gain due to low collector current levels and lower slew rates. The effect upon slew rate is covered in detail under the compensation section.

INPUT OFFSET CURRENT

The ideal case of the differential amplifier and its associated bias current does not possess an input offset current. Circuit realizations always have a small difference in bias currents from one input to the other, however. This difference is called the input offset current. Actual magnitudes of offset current are usually at least an order of magnitude below the bias current. For many applications this offset may be ignored but very high gain, high input impedance amplifiers should possess as little I_{OS} as possible because the difference in currents flowing across large impedances develops substantial offset voltages. Output voltage offset due to I_{OS} can be calculated by

$$V_{OUT}=A_{CI}(I_{OS}R_S) \tag{5}$$

Hence, high gain and high input impedances magnify directly to the output, the error created by offset current. Circuits capable of nulling the input voltage and current errors are available and will be covered later in this chapter.

INPUT OFFSET CURRENT DRIFT

Of considerable importance is the temperature coefficient of input offset current. Even though the effects of offset are nulled at room temperature, the output will drift due to changes in offset current over temperature. Many popular models now include a typical specification for I_{OS} drift with values ranging in the 0.5nA/°C area. Obviously, those applications requiring low input offset currents also require low drift with temperature.

INPUT IMPEDANCE

Differential and common-mode impedances looking into the input are often specified for integrated op amps. The differential impedance is the total resistance looking from one input to the other, while common-mode is the common impedance as measured to ground. Differential impedances are calculated by measuring the change of bias current caused by a change in the input voltage.

COMMON-MODE RANGE

All input structures have limitations as to the range of voltages over which they will operate properly. This range of voltages impressed upon both inputs which will not cause the output to misbehave is called the common-mode range. Most amplifiers possess common-mode ranges of ±12V with supplies of ±15V.

COMMON-MODE REJECTION RATIO

The ideal operational amplifier should have no gain for an input signal common to both inputs. Practical amplifiers do have some gain to common-mode signals. The classic definition for common-mode rejection ratio of an amplifier is the ratio of the differential signal gain to the common-mode signal gain expressed in dB as shown in equation 6a.

$$\text{CMRR (dB)} = 20 \log \frac{e_O \; e_I}{e_O \; e_{CM}} \tag{6a}$$

The measurement CMRR as in 6a requires 2 sets of measurements. However, note that if e_o in equation 6a is held constant, CMRR becomes:

$$\text{CMRR (dB)} = 20 \log \frac{e_{CM}}{e_I} \tag{6b}$$

A new alternate definition of CMRR based on 6b is the ratio of the change of input offset voltage to the input common-mode voltage change producing it.

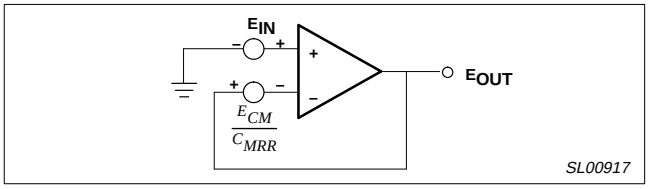

Figure 4. Effects of CMRR on Voltage-Follower

Figure 4 illustrates the application of the equivalent common-mode error generator to the voltage-follower circuit. The gain of the

voltage-follower with error contributions caused by both finite gain and finite common-mode rejection ratio is shown in equation 7.

$$\frac{e_O}{e_{IN}} = \frac{1 \quad 1\ CMRR}{1 \quad 1\ A} \tag{7}$$

where A equals open-loop gain and is frequency-dependent.

AC PARAMETERS

Parameter definition has, up to this point, been dealing primarily with DC quantities of voltages currents, etc. Several important AC, or frequency-dependent parameters will now be discussed.

An ideal gain block was defined earlier as one which would provide infinite gain and bandwidth. Real circuits approximate infinite open-loop gain with low frequency gains in excess of 100dB. The very high gains achieved with present designs are possible only by cascading stages. Although providing very high open-loop gain, the cascading of stages results in the need for frequency compensation in closed-loop configurations and reduces the open-loop.

LARGE-SIGNAL BANDWIDTH

The large-signal or power bandwidth of an amplifier refers to its ability to provide its maximum output voltage swing with increasing frequency. At some frequency the output will become slew rate limited and the output will begin to degrade. This point is defined by

$$f_{PL} = \frac{SLEW\ RATE}{2\pi \quad E_{OUT}} \tag{8}$$

where f_{PL} is the upper power bandwidth frequency and E_{OUT} is the peak output swing of the amplifier.

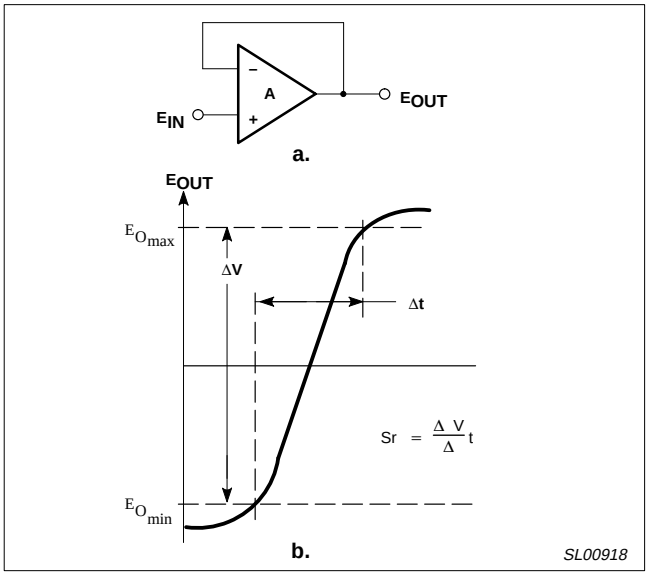

Figure 5. Amplifier Slew Rate Limitations

SLEW RATE

The maximum rate of change of the output in response to a step input signal is termed slew rate. Deviation from the ideal is caused by the limitation in frequency response of the amplifier stages and the phase compensation technique used. Summing node and amplifier output capacitances must be kept to a minimum to guarantee getting the maximum slew rate of the operational amplifier. Circuit board layout must also be of high frequency quality. Power supplies should be adequately bypassed at the pins, with both low and high frequency components, to avoid possible ringing. A selection of a proper capacitor in parallel with the feedback resistor may be necessary. Too small a value could result in excessive ringing and too large a value will decrease frequency response. In general, the worst case slew rate is in the unity gain non-inverting mode (see Figure 5a). Specifications of slew rate should always reflect this worst case condition with the maximum required compensation network.

FREQUENCY RESPONSE

Distributed capacitances and transit times in semiconductors cause an upper frequency limit or pole for each gain stage. Monolithic PNP transistors, used for level shifting, possess poor upper frequency characteristics. Cascaded gain stages, used to approach the highest gain, subtract from the maximum frequency response. As shown in Figure 6, the open-loop frequency

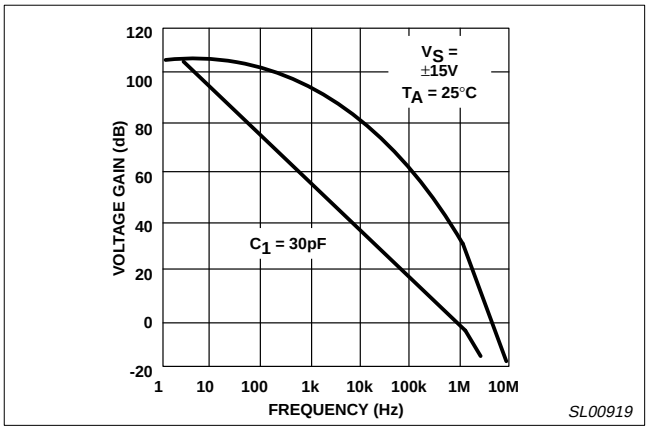

Figure 6. Open-Loop Voltage Gain as a Function of Frequency

response of the op amps shown crosses unity gain at approximately 10MHz. Closed-loop response is unstable without compensation, however, so typical unity gain frequencies are readjusted by the effects of phase compensation, in this case 1MHz.

From Figure 6, it is also apparent that an amplifier has a trade-off between gain and bandwidth. Higher gains are achieved at the expense of bandwidth. This trade-off is a constant figure called the gain bandwidth product.

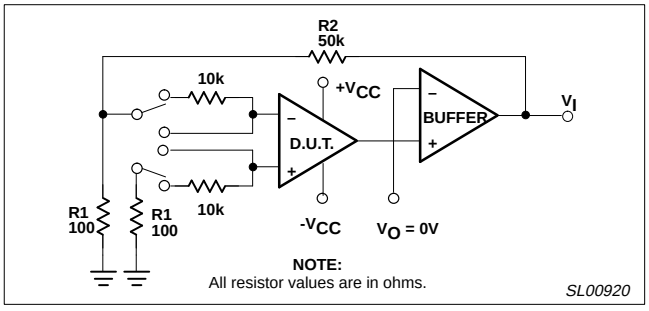

Figure 7. Circuit Diagram Used for CMRR Measurement

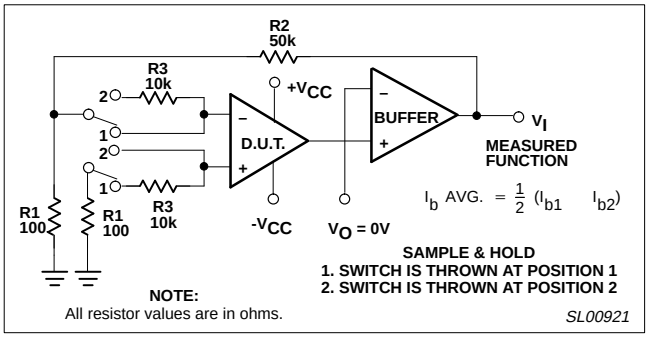

Figure 8. Circuit Diagram Used for Average Bias Current Measurement

TEST METHODS

Product testing of integrated circuits uses automatic test equipment. Large computer-controlled test decks test all data sheet limits in a matter of milliseconds. Each parameter is tested in a specific circuit configuration defined by the test hardware.

A typical simplified op amp test configuration is depicted by Figure 9. Units may be classed
in several categories according to selected parameters. Even failures may be classified categorically, depending upon their mode of failure.

Figures 7, 8, 10 and 11 illustrate the general test setups commonly used to measure CMRR, average bias current, offset voltage and current, and open-loop gain, respectively.

In general, the following parameters are tested under the following conditions.

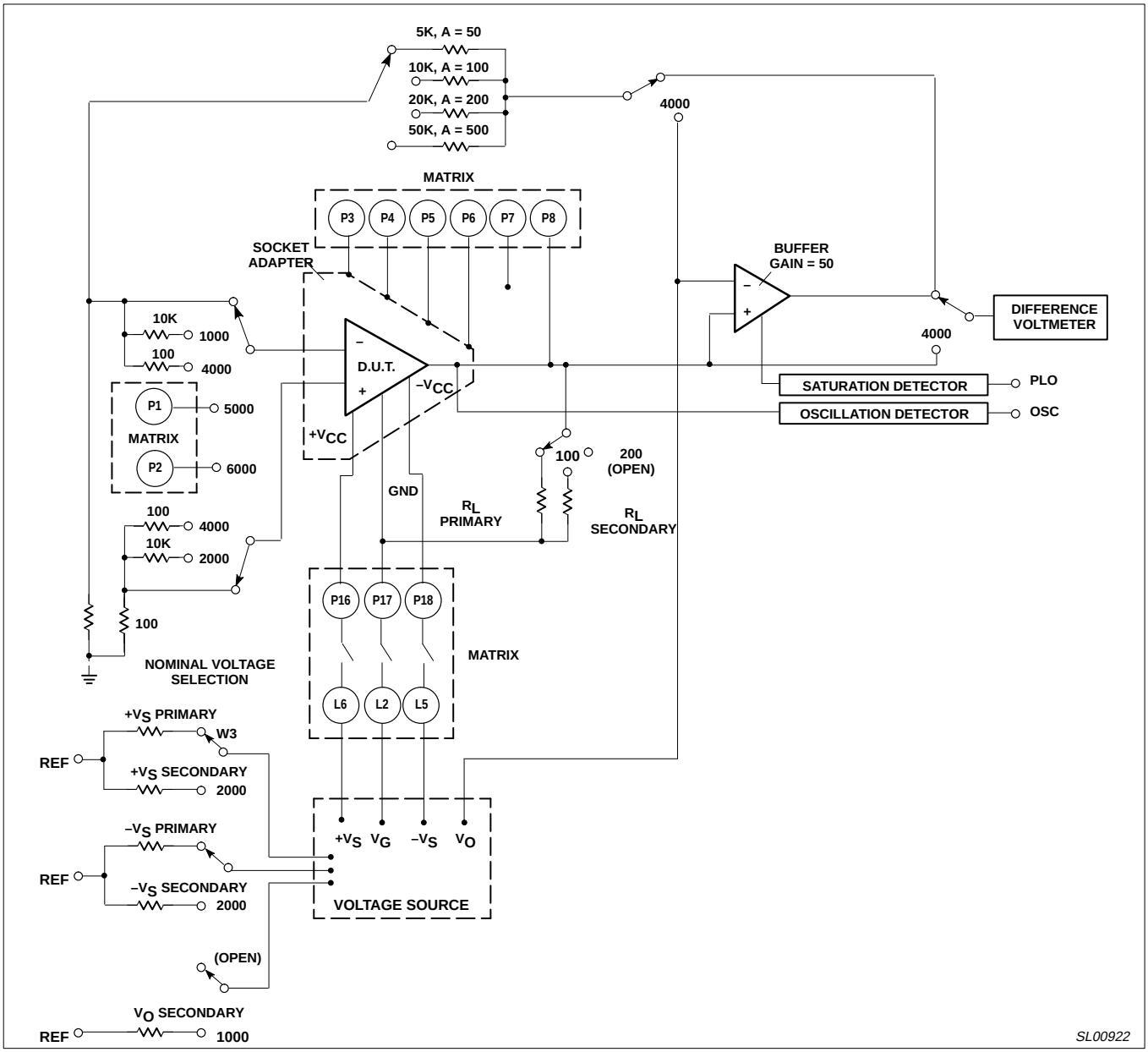

Figure 9. A Typical Op Amp Test Circuit (Simplified)

COMMON-MODE REJECTION

The test setup for CMRR is given in Figure 7. Resistor values are chosen to provide sufficient sensitivity and accuracy for the device type being tested and the voltage measuring equipment being used.

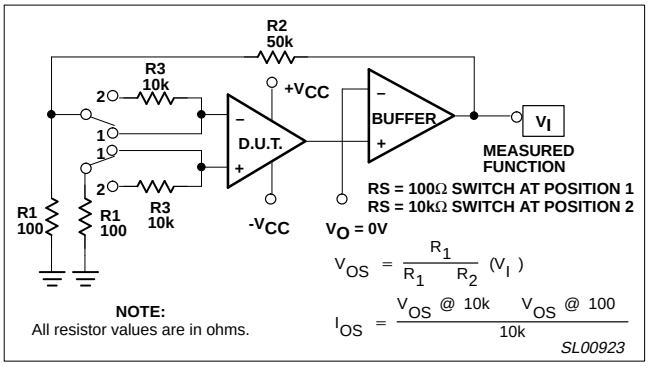

Figure 10. Circuit Diagram Used for Offset Voltage and Offset Current

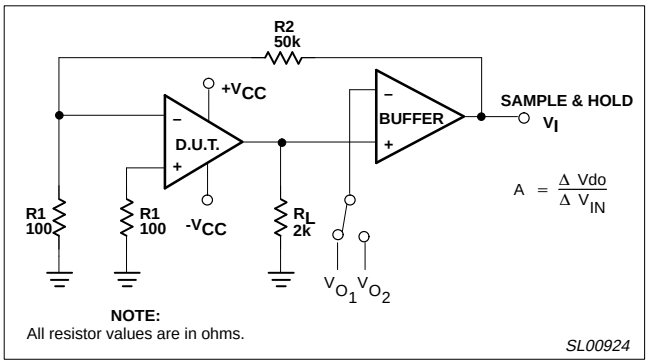

Figure 11. Circuit Diagram Used for Large-Signal Open-Loop Gain Measurement

The positive common-mode input voltage within the range V_{CM1} is algebraically subtracted from all supply voltages and from V_O. Then V_1 is measured (V_{11}). The most negative common-mode voltage within the range, V_{CM2}, is then subtracted from all the supply voltages and V_O, and V_1 is again measured (V_{12}).

Then

$$CMRR=(R1+R2)/R1(V_{CM1}-V_{CM2})/V_{11}-V_{12} \quad (9)$$

This operation is equivalent to swinging both inputs over the full common-mode range, and holding the output voltage constant, but it makes the V_1 measurement much simpler.

BIAS CURRENT

Bias current is measured in the configuration of Figure 8.

With switches at position 1 and V_O=0V, measure V_{11}. Move switches to position 2

and again measure V_{12}. Calculate I_{BIAS} (average), by

$$I_{B1} = \frac{R_1}{R1\quad R2}\left(\frac{V1}{R3}\right) \quad (10a)$$

$$I_{B2} = \frac{R_1}{R1\quad R2}\left(\frac{V1}{R3}\right) \quad (10b)$$

$$I_{BIAS(avg)} = \frac{I_{B1}\quad I_{B2}}{2} = \frac{R1}{R1\quad R2}\,\frac{V_{11}\quad V_{12}}{2R3} \quad (10c)$$

OFFSET VOLTAGE

Figure 10 is used for both offset voltage and current. With V_O at 0V and the switches selecting the source impedance of 100Ω, the offset voltage is measured at V_1 and is equal to

$$V_{OS} = \frac{R1V_1}{R1\quad R2} \quad (11)$$

OFFSET CURRENT

Offset current is measured by calculation of offset voltage change with a change in source impedance. With switches in position 1, measure V_{12}. Calculate the contribution of I_{OS} by

$$I_{OS} = V_{12}\quad \frac{V_I}{R3} \quad (12)$$

SIGNAL GAIN

The signal gain of operational amplifiers is most commonly specified for the full output swing.

This is referred to as large signal voltage gain and can be measured by the circuit of Figure 11. Usually specified under a specific load determined by R_L, a signal equal to the maximum swing of the output voltage is applied to V_O in both positive and negative directions. V_{11} and V_{12} are measured values of V_1 and V_O=maximum positive and maximum negative signals, respectively. The gain of the device under test then becomes

$$A_{VO} = \left(\frac{R1\quad R2}{R1}\right)\left(\frac{V_{O1}\quad V_{O2}}{V_{11}\quad V_{12}}\right) \quad (13)$$

SLEW RATE

Many other parameters are checked automatically by similar means. Only the most important ones have been covered here. Of great interest to the designer are other parameters which do not necessarily carry minimum or maximum limits. One such parameter is slew rate. The configuration used to measure slew rate depends upon the intended application. Worst case conditions arise in the unity gain non-inverting mode.

Figure 12 shows a typical bench setup for measuring the response of the output to a step input. The input step frequency should be of a frequency low enough for the output of the op amp to have sufficient time to slew from limit to limit. In addition, V_{IN} must be less

than absolute maximum input voltage and the waveform should have good rise and fall times. The slew rate is then calculated from the slope of the output voltage versus time or

$$SR = \frac{\Delta\ V_{OUT}}{\Delta} T \text{ in } V\quad s \quad (14)$$

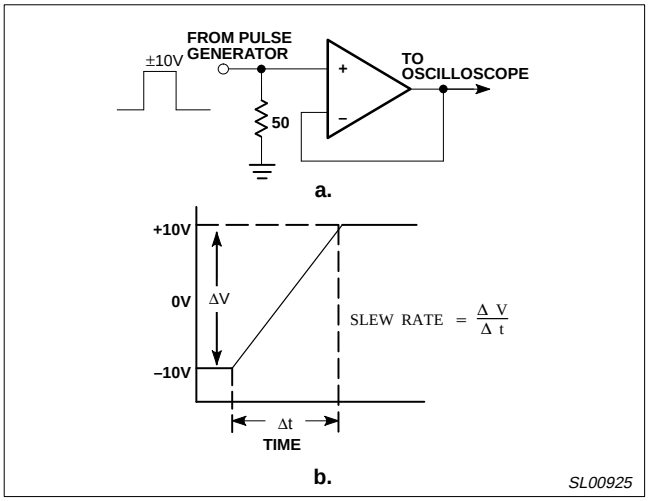

Figure 12. Measuring Slew

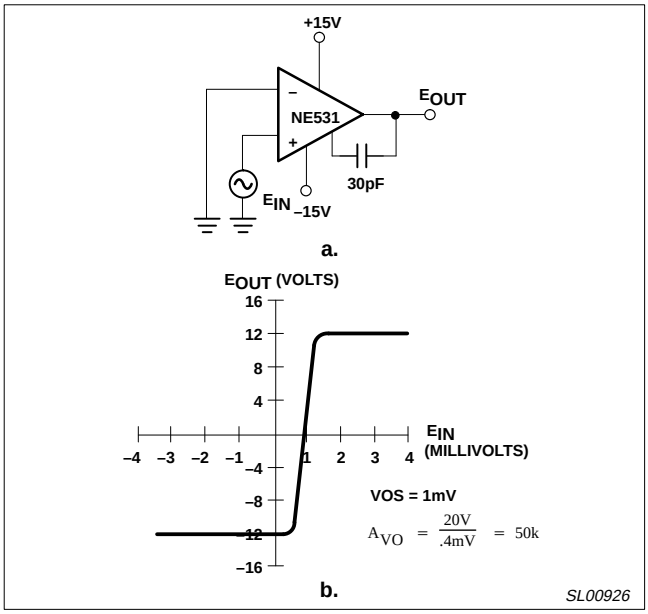

Figure 13. Transfer Curve of 531

OP AMP CURVE TRACER

Two of the most important parameters of linear integrated circuits having differential inputs are voltage gain and input offset voltage. These parameters may be read directly from a plot of the transfer characteristic of the device. This memo will describe a very simple curve tracer which, when used with an oscilloscope, will display the transfer characteristic of most Philips Semiconductors linear devices.

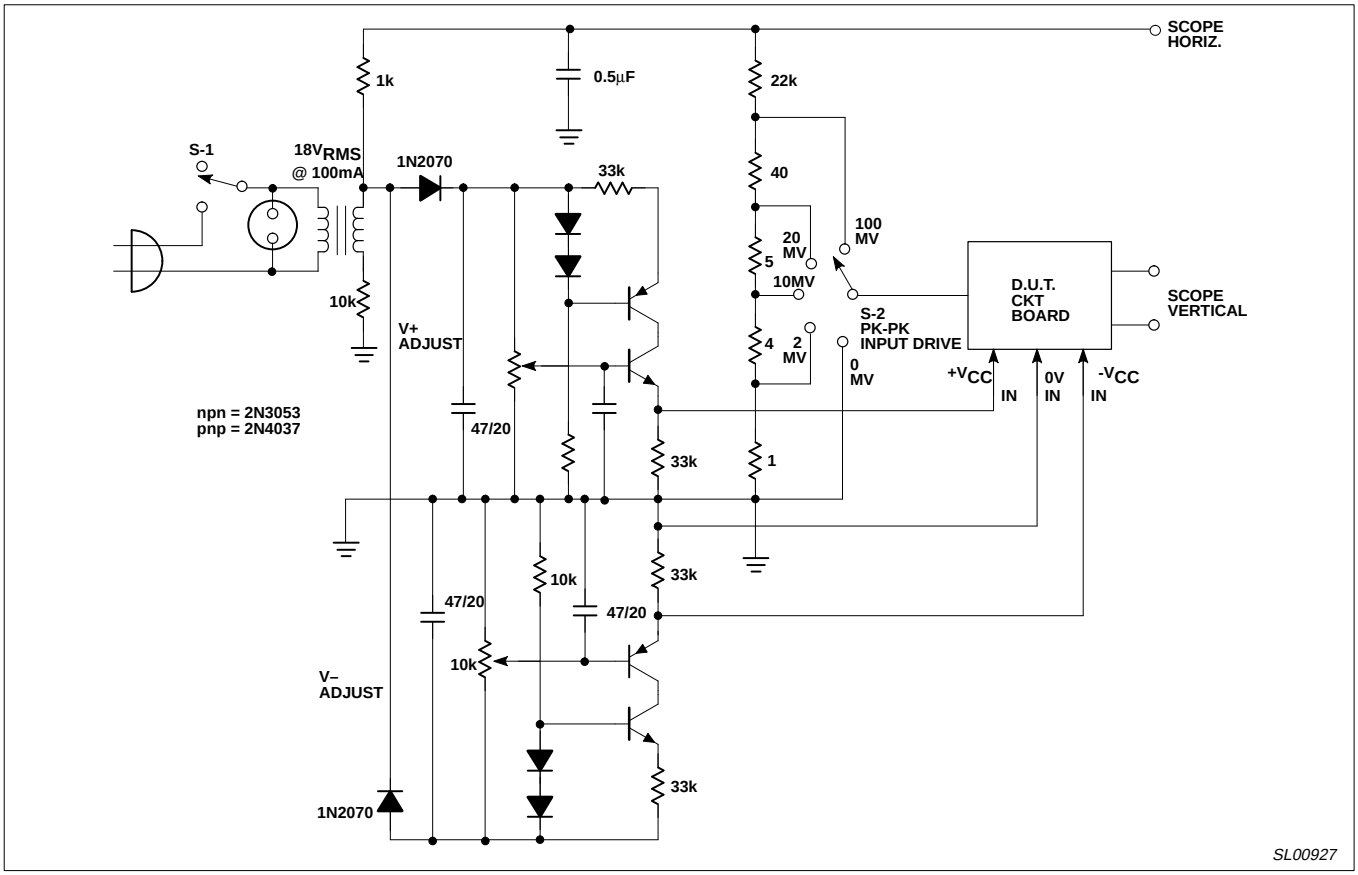

Figure 14. Curve Tracer Schematic

Figure 13 shows the transfer characteristics of a typical linear device, the Philips Semiconductors NE531. Note that the unit saturates at approximately +12V and -12V and exhibits a linear transfer characteristic between -10V and +10V.

From the slope of this linear portion of the transfer characteristic, and from the point and +10V where it crosses the E_{IN} axis, the voltage gain and offset voltage may be determined. It can be seen that the voltage gain of the device under test, (DUT), is 50,000 and its input offset voltage is 1.0mV.

A simple circuit to display the curves of Figure 13 on an oscilloscope is shown in Figure 14. A 60Hz, $44V_{P-P}$ sinewave is applied to the horizontal input of oscilloscope and an attenuated version of the sinewave is applied to the input of the DUT.

The output of the DUT drives the vertical input of the scope. For providing V+ and V- to the DUT, the tester uses two simple adjustable regulators, both current-limited at 25mA. Input drive to the DUT may be selected by means of S-2 as shown.

To use the curve tracer, first preset the V+ and V- supplies with an accurate meter. The supply voltages are somewhat dependent on AC line regulation and should be checked periodically. The horizontal gain of the scope may be set to give a convenient readout of the peak-to-peak DUT input signal corresponding to the setting of S-2. As some devices have two outputs, a second output line (vertical 2) has been provided for these devices. The transfer function of such devices will be inverted to that of Figure 13.

Simplicity and low cost are the two major attributes of this tester. It is not intended to perform highly rigorous tests for all devices. It is, however, a reasonably accurate means of determining the gains and offset voltages of most amplifiers. It will, in addition, indicate the transfer curves of comparators and sense amplifiers with equivalent accuracies.

AMPLIFIER DESIGN

Linear operational amplifier ICs were introduced soon after the appearance of the first digital integrated circuits. The performance of these early devices, however, left much to be desired until the introduction of the 709 device. Even with its lack of short-circuit protection and its complicated compensation requirements, the 709 gained real acceptance for the IC op amp. The 709 was designed using a three-stage approach requiring both input and output stage compensation. In addition, the output stage was not short-circuit proof and the input stage latched-up under certain conditions, requiring external protection.

Much better designs soon were introduced. Among the contenders were the 741, 748, 101, and 107 devices. All were general purpose devices with single capacitor compensation, (some were internally-compensated), and all heralded input and output overstress protection. The basic design has two gain stages. By rolling off the frequency response of one of these (the second stage), so that the overall gain is unity at a frequency below the point where excess phase becomes significant, the device can be stabilized for all feedback configurations. Further, by making the first stage a voltage-to-current converter, with a small g_M and the second stage a current-to-voltage converter with a high r_M, the second stage can be rolled off at 6dB octave with a small value capacitor in

the order of 30pF, which can then be built into the device itself. This concept is shown in Figure 15.

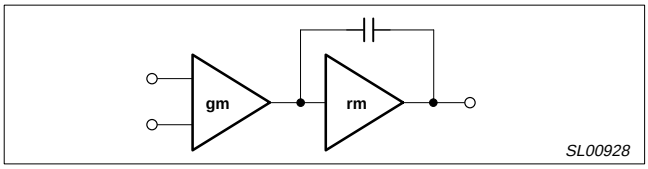

Figure 15. Basic Two-Stage Op Amp Design

The frequency and phase response of the PNP devices in the first stage dictate a roll-off in the second stage to give a loop gain of unity at about 1.0MHz. For the unity gain feedback configuration, this implies an open-loop gain of unity at this frequency. The capacitor C_C controls this parameter by looking much smaller than r_M at frequencies above a few cycles, giving a clean 6dB/octave roll-off over 5 decades.

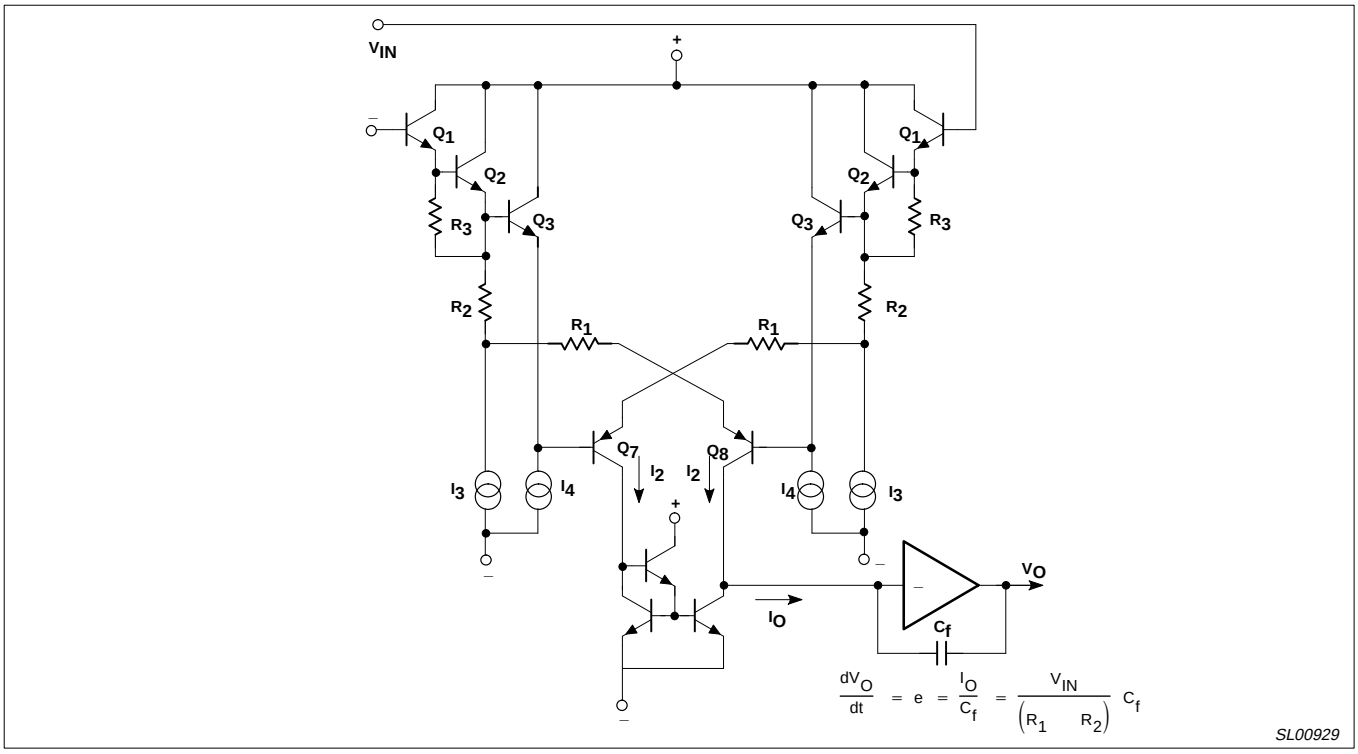

Figure 16. Input Structure of 531

The overall gain at frequencies where the impedance of C_C dominates r_m is given by

$$A_{V(sigma)} = \frac{QI_{S1}}{4kT} \quad \frac{1}{C_C} \qquad (15)$$

Substituting the value given, we find that a capacitance of C_C=30pF gives a unity gain frequency of about 1.0MHz.

First-stage large signal current also defines the slew rate for a specific compensation technique. It is this current which must charge and discharge the C_C by the expression

$$SR = \frac{dV}{dT} = \frac{I_{LS}}{C_C} \qquad (16)$$

where I_{LS} is the largest signal current of the input stage. Obviously, the slew rate can be improved by increasing the first-stage collector current. This would, however, reflect directly upon the bias current by increasing it.

Two serious limitations, then, of these devices for diverse applications are input bias current and slew rate. Both may be overcome with small changes of the input structure to yield higher performance devices.

Reducing the input bias current becomes a matter of raising the transistor beta of the first stage. Several current designs boasting very low input currents use what is termed super beta input devices. These transistors have betas of 1,500 to 7,000. Bias currents under 2nA can be achieved in this way. Even though the B_{VCEO} of such transistors can be as low as 1V, the lower breakdowns are accounted for in the input stage by rearranging the bias technique. Bandwidths and slew rates suffer only slightly as a result of the lower current levels.

The second limitation of 741 devices is slew rate. As previously mentioned, the rate of change is dictated by the compensation capacitance as charged by the large signal current of the first stage. By altering the large signal g_M of the first stage as depicted by Figure 18, the slew rate can be dramatically increased.

The additional current supplied during large signal swings by current source I_4 causes the first-stage transfer function to change as shown in Figure 19. The compensation capacitor is returned to the output of the NE531 structure because the output driving source must be capable of supplying the increased current to charge the capacitor.

Large-signal bandwidths with this input structure will be essentially the same as the small-signal response. Full bandwidth possibilities of this configuration are still limited by the beta and f_t of the lateral PNP devices used for collector loads in the first stage. Even so, the

slew rate of the NE531 and NE538 is a factor of 40 better than general purpose devices.

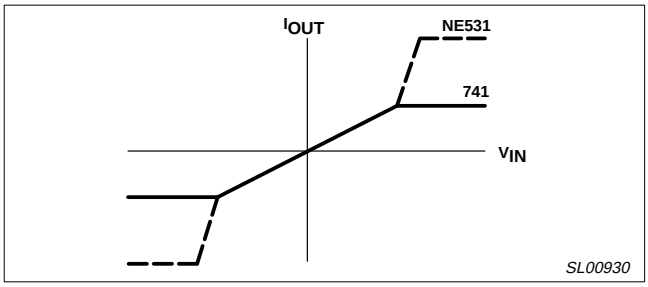

Figure 17. Voltage/Current Curves of First Stage