National Semiconductor

April 1995

LM1972
µPot™ 2-Channel 78dB Audio Attenuator with Mute

General Description

The LM1972 is a digitally controlled 2-channel 78dB audio attenuator fabricated on a CMOS process. Each channel has attenuation steps of 0.5dB from 0dB–47.5dB, 1.0dB steps from 48dB–78dB, with a mute function attenuating 104dB. Its logarithmic attenuation curve can be customized through software to fit the desired application.

The performance of a µPot is demonstrated through its excellent Signal-to-Noise Ratio, extremely low (THD+N), and high channel separation. Each µPot contains a mute function that disconnects the input signal from the output, providing a minimum attenuation of 96dB. Transitions between any attenuation settings are pop free.

The LM1972's 3-wire serial digital interface is TTL and CMOS compatible; receiving data that selects a channel and the desired attenuation level. The Data-Out pin of the LM1972 allows multiple µPots to be daisy-chained together, reducing the number of enable and data lines to be routed for a given application.

Key Specifications

- Total Harmonic Distortion + Noise: 0.003% (max)
- Frequency response: 100 kHz (−3dB) (min)
- Attenuation range (excluding mute): 78dB (typ)
- Differential attenuation: ±0.25dB (max)
- Signal-to-noise ratio (ref. 4 Vrms): 110dB (min)
- Channel separation: 100dB (min)

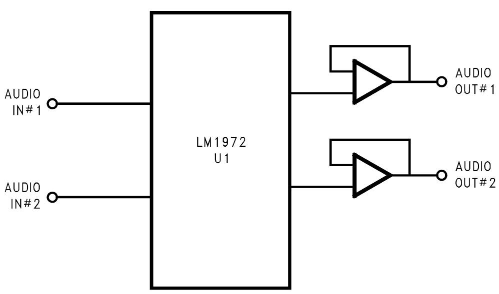
Features

- 3-wire serial interface
- Daisy-chain capability
- 104dB mute attenuation
- Pop and click free attenuation changes

Applications

- Automated studio mixing consoles
- Music reproduction systems
- Sound reinforcement systems
- Electronic music (MIDI)
- Personal computer audio control

Typical Application

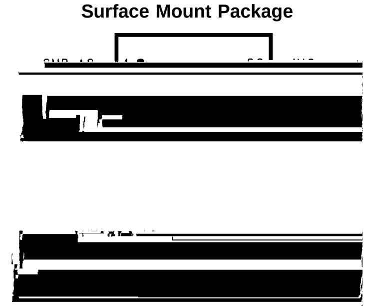


DS011978-1

FIGURE 1. Typical Audio Attenuator Application Circuit

Connection Diagram

Dual-In-Line Plastic or Surface Mount Package



DS011978-2

Top View
Order Number LM1972M or LM1972N
See NS Package Number M20B or N20A

µPot™ and Overture™ are trademarks of National Semiconductor Corporation.

 DS011978

Absolute Maximum Ratings (Notes 2, 1)

If Military/Aerospace specified devices are required, please contact the National Semiconductor Sales Office/ Distributors for availability and specifications.

Supply Voltage (V_{DD}–V_{SS})	15V
Voltage at Any Pin	V_{SS} − 0.2V to V_{DD} + 0.2V
Power Dissipation (Note 3)	150 mW
ESD Susceptability (Note 4)	2000V
Junction Temperature	150˚C
Soldering Information	
N Package (10 sec.)	+260˚C
Storage Temperature	−65˚C to +150˚C

Operating Ratings (Note 1) (Note 2)

	T_{MIN}	T_A	T_{MAX}
Temperature Range			
$T_{MIN} \le T_A \le T_{MAX}$	0˚C	$\le T_A$	≤ +70˚C
Supply Voltage (V_{DD} − V_{SS})			4.5V to 12V

Electrical Characteristics (Note 1) (Note 2)

The following specifications apply for all channels with V_{DD} = +6V, V_{SS} = −6V, V_{IN} = 5.5 Vpk, and f = 1 kHz, unless otherwise specified. Limits apply for T_A = 25˚C. Digital inputs are TTL and CMOS compatible.

Symbol	Parameter	Conditions	LM1972 Typical (Note 5)	LM1972 Limit (Note 6)	Units (Limits)
I_S	Supply Current	Inputs are AC Grounded	2	**4**	mA (max)
THD+N	Total Harmonic Distortion plus Noise	V_{IN} = 0.5 Vpk @ 0dB Attenuation	0.0008	0.003	% (max)
XTalk	Crosstalk (Channel Separation)	0dB Attenuation for V_{IN} V_{CH} measured @ −78dB	110	100	dB (min)
SNR	Signal-to-Noise Ratio	Inputs are AC Grounded @ −12dB Attenuation A-Weighted	120	110	dB (min)
A_M	Mute Attenuation		104	96	dB (min)
	Attenuation Step Size Error	0dB to −47.5dB		±0.05	dB (max)
		−48dB to −78dB		±0.25	dB (max)
	Absolute Attenuation Error	Attenuation @ 0dB	0.03	0.5	dB (min)
		Attenuation @ −20dB	19.8	19.0	dB (min)
		Attenuation @ −40dB	39.5	39.0	dB (min)
		Attenuation @ −60dB	59.3	57.5	dB (min)
		Attenuation @ −78dB	76.3	74.5	dB (min)
	Channel-to-Channel Attenuation	Attenuation @ 0dB, −20dB, −40dB, −60dB		±0.5	dB (max)
	Tracking Error	Attenuation @ −78dB		±0.75	dB (max)
I_{LEAK}	Analog Input Leakage Current	Inputs are AC Grounded	10.0	100	nA (max)
R_{IN}	AC Input Impedance	Pins 4, 20, V_{IN} = 1.0 Vpk, f = 1 kHz	40	20	kΩ (min)
				60	kΩ (max)
I_{IN}	Input Current	@ Pins 9, 10, 11 @ 0V $<V_{IN}<$ 5V	1.0	±100	nA (max)
f_{CLK}	Clock Frequency		3	2	MHz (max)
V_{IH}	High-Level Input Voltage	@ Pins 9, 10, 11		2.0	V (min)
V_{IL}	Low-Level Input Voltage	@ Pins 9, 10, 11		0.8	V (max)
	Data-Out Levels (Pin 12)	V_{DD}=6V, V_{SS}=0V		0.1	V (max)
				5.9	V (min)

Note 1: All voltages are measured with respect to GND pins (1, 3, 5, 6, 14, 16, 19), unless otherwise specified.

Note 2: *Absolute Maximum Ratings* indicate limits beyond which damage to the device may occur. Operating Ratings indicate conditions for which the device is functional, but do not guarantee specific performance limits. *Electrical Characteristics* state DC and AC electrical specifications under particular test conditions which guarantee specific performance limits. This assumes that the device is within the Operating Ratings. Specifications are not guaranteed for parameters where no limit is given, however, the typical value is a good indication of device performance.

Note 3: The maximum power dissipation must be derated at elevated temperatures and is dictated by T_{JMAX}, θ_{JA}, and the ambient temperature T_A. The maximum allowable power dissipation is PD = (T_{JMAX} − T_A)/θ_{JA} or the number given in the Absolute Maximum Ratings, whichever is lower. For the LM1972, T_{JMAX} = +150˚C, and the typical junction-to-ambient thermal resistance, when board mounted, is 65˚C/W.

Note 4: Human body model, 100 pF discharged through a 1.5 kΩ resistor.

Note 5: Typicals are measured at 25˚C and represent the parametric norm.

Note 6: Limits are guaranteed to National's AOQL (Average Output Quality Level).

Electrical Characteristics (Note 1) (Note 2) (Continued)

Pin Description

Signal Ground (3, 19): Each input has its own independent ground, GND1 and GND2.

Signal Input (4, 20): There are 2 independent signal inputs, IN1 and IN2.

Signal Output (2, 17): There are 2 independent signal outputs, OUT1 and OUT2.

Voltage Supply (13, 15): Positive voltage supply pins, V_{DD1} and V_{DD2}.

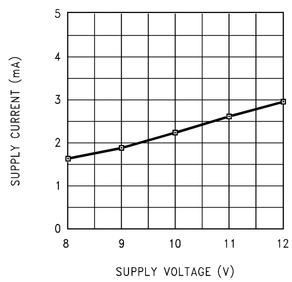
Voltage Supply (7, 18): Negative voltage supply pins, V_{SS1} and V_{SS2}. To be tied to ground in a single supply configuration.

AC Ground (1, 5, 6, 14, 16): These five pins are not physically connected to the die in any way (i.e., No bondwires). These pins must be AC grounded to prevent signal coupling between any of the pins nearby. Pin 14 should be connected to pins 13 and 15 for ease of wiring and the best isolation, as an example.

Logic Ground (8):

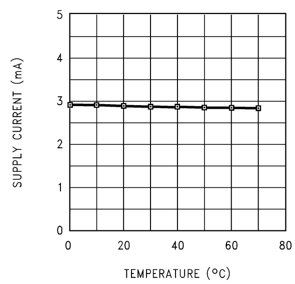
Typical Performance Characteristics

Supply Current vs Supply Voltage



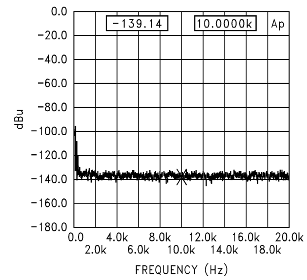
DS011978-15

Supply Current vs Temperature



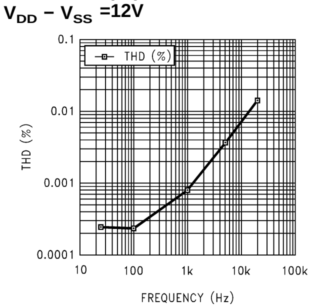
DS011978-16

Noise Floor Spectrum by FFT Amplitude vs Frequency



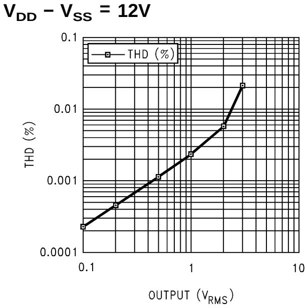
DS011978-17

THD vs Freq by FFT $V_{DD} - V_{SS}$ =12V



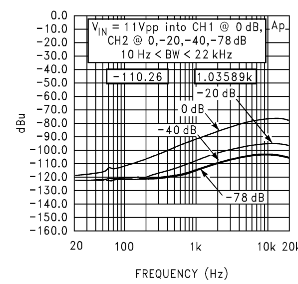
DS011978-18

THD vs V_{OUT} at 1 KHz by FFT $V_{DD} - V_{SS}$ = 12V



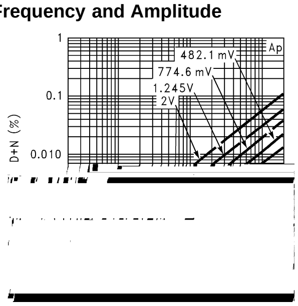
DS011978-19

Crosstalk Test



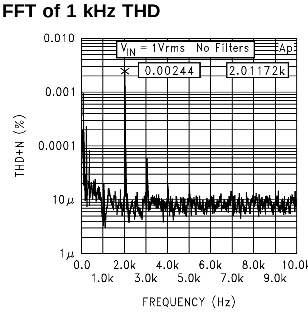
DS011978-20

THD + N vs Frequency and Amplitude



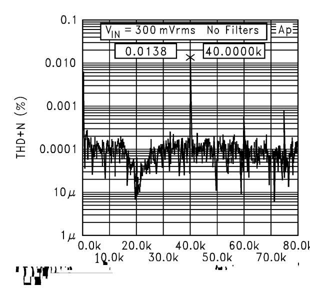
DS011978-21

FFT of 1 kHz THD



DS011978-22

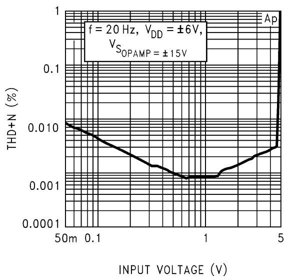
FFT of 20 kHz THD



DS011978-23

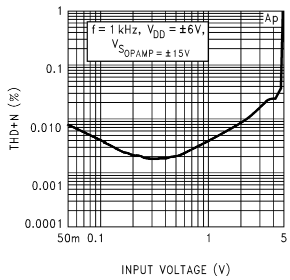
Typical Performance Characteristics (Continued)

THD + N vs Amplitude



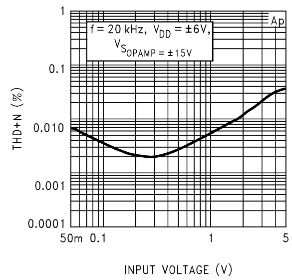
DS011978-24

THD + N vs Amplitude



DS011978-25

THD + N vs Amplitude



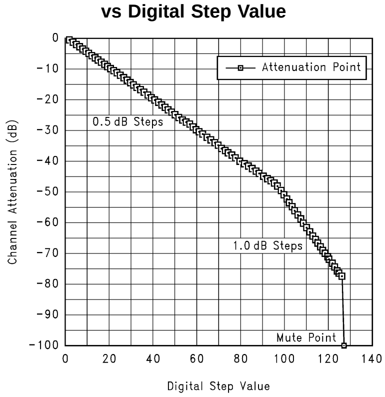
DS011978-26

Application Information

ATTENUATION STEP SCHEME

The fundamental attenuation step scheme for the LM1972 µPot is shown in *Figure 3*. This attenuation step scheme, however, can be changed through programming techniques to fit different application requirements. One such example would be a constant logarithmic attenuation scheme of 1dB steps for a panning function as shown in *Figure 4*. The only restriction to the customization of attenuation schemes are the given attenuation levels and their corresponding data bits shown in *Table 1*. The device will change attenuation levels only when a channel address is recognized. When recognized, the attenuation level will be changed corresponding to the data bits shown in *Table 1*. As shown in *Figure 6*, an LM1972 can be configured as a panning control which separates the mono signal into left and right channels. This circuit may utilize the fundamental attenuation scheme of the LM1972 or be programmed to provide a constant 1dB logarithmic attenuation scheme as shown in *Figure 4*.

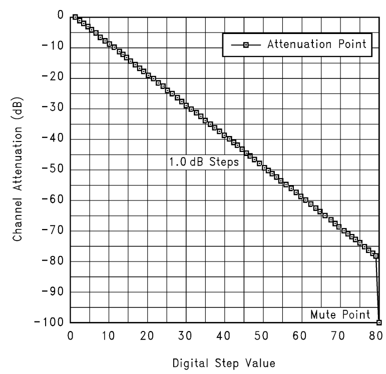
LM1972 Channel Attenuation vs Digital Step Value



DS011978-6

FIGURE 3. LM1972 Attenuation Step Scheme

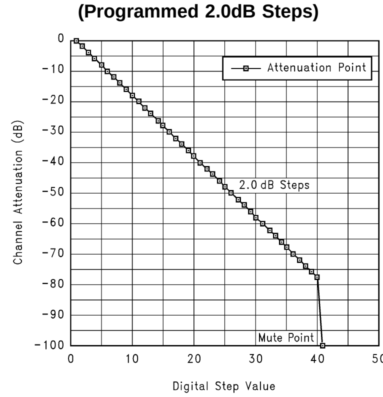
LM1972 Channel Attenuation vs Digital Step Value (Programmed 1.0dB Steps)



DS011978-7

FIGURE 4. LM1972 1.0dB Attenuation Step Scheme

LM1972 Channel Attenuation vs Digital Step Value (Programmed 2.0dB Steps)



DS011978-8

FIGURE 5. LM1972 2.0dB Attenuation Step Scheme

Application Information (Continued)

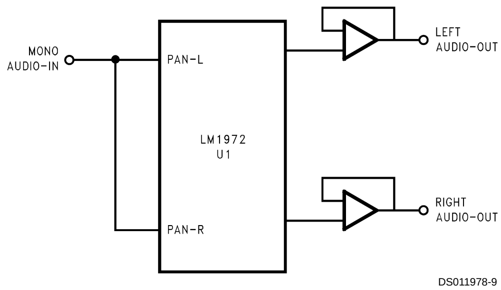


FIGURE 6. Mono Panning Circuit

INPUT IMPEDANCE

The input impedance of a µPot is constant at a nominal 40 kΩ. To eliminate any unwanted DC components from propagating through the device it is common to use 1 µF input coupling caps. This is not necessary, however, if the dc offset from the previous stage is negligible. For higher performance systems, input coupling caps are preferred.

OUTPUT IMPEDANCE

The output of a µPot varies typically between 25 kΩ and 35 kΩ and changes nonlinearly with step changes. Since a µPot is made up of a resistor ladder network with a logarithmic attenuation, the output impedance is nonlinear. Due to this configuration, a µPot cannot be considered as a linear potentiometer, but can be considered only as a logarithmic attenuator.

It should be noted that the linearity of a µPot cannot be measured directly without a buffer because the input impedance of most measurement systems is not high enough to provide the required accuracy. Due to the low impedance of the measurement system, the output of the µPot would be loaded down and an incorrect reading will result. To prevent loading from occurring, a JFET input op amp should be used as the buffer/amplifier. The performance of a µPot is limited only by the performance of the external buffer/amplifier.

MUTE FUNCTION

One major feature of a µPot is its ability to mute the input signal to an attenuation level of 104dB as shown in *Figure 3*. This is accomplished internally by physically isolating the output from the input while also grounding the output pin through approximately 2 kΩ.

The mute function is obtained during power-up of the device or by sending any binary data of 01111111 and above (to 11111111) serially to the device. The device may be placed into mute from a previous attenuation setting by sending any of the above data. This allows the designer to place a mute button onto his system which could cause a microcontroller to send the appropriate data to a µPot and thus mute any or all channels. Since this function is achieved through software, the designer has a great amount of flexibility in configuring the system.

DC INPUTS

Although the µPot was designed to be used as an attenuator for signals within the audio spectrum, the device is capable of tracking an input DC voltage. The device will track DC voltages to a diode drop above each supply rail.

One point to remember about DC tracking is that with a buffer at the output of the µPot, the resolution of DC tracking will depend upon the gain configuration of that output buffer and its supply voltage. It should also be remembered that the output buffer's supply voltage does not have to be the same as the µPot's supply voltage. This could allow for more resolution when DC tracking.

SERIAL DATA FORMAT

The LM1972 uses a 3-wire serial communication format that is easily controlled by a microcontroller. The timing for the 3-wire set, comprised of DATA-IN, CLOCK, and LOAD/SHIFT is shown in *Figure 2*. *Figure 9* exhibits in block diagram form how the digital interface controls the tap switches which select the appropriate attenuation level. As depicted in *Figure 2*, the LOAD/SHIFT line is to go low at least 150 ns before the rising edge of the first clock pulse and is to remain low throughout the transmission of each set of 16 data bits. The serial data is comprised of 8 bits for channel selection and 8 bits for attenuation setting. For both address data and attenuation setting data, the MSB is sent first and the 8 bits of address data are to be sent before the 8 bits of attenuation data. Please refer to *Figure 7* to confirm the serial data format transfer process.

TABLE 1. LM1972 Micropot Attenuator Register Set Description

MSB: LSB	
Address Register (Byte 0)	
0000 0000	Channel 1
0000 0001	Channel 2
0000 0010	Channel 3
Data Register (Byte 1)	
Contents	**Attenuation Level dB**
0000 0000	0.0
0000 0001	0.5
0000 0010	1.0
0000 0011	1.5
: : : : :	: :
0001 1110	15.0
0001 1111	15.5
0010 0000	16.0
0010 0001	16.5
0010 0010	17.0
: : : : :	: :
0101 1110	47.0
0101 1111	47.5
0110 0000	48.0
0110 0001	49.0
0110 0010	50.0
: : : : :	: :
0111 1100	76.0
0111 1101	77.0
0111 1110	78.0
0111 1111	100.0 (Mute)
1000 0000	100.0 (Mute)
: : : : :	: :

Application Information (Continued)

TABLE 1. LM1972 Micropot Attenuator Register Set Description (Continued)

MSB:	**LSB**
Data Register (Byte 1)	
1111 1110	100.0 (Mute)
1111 1111	100.0 (Mute)

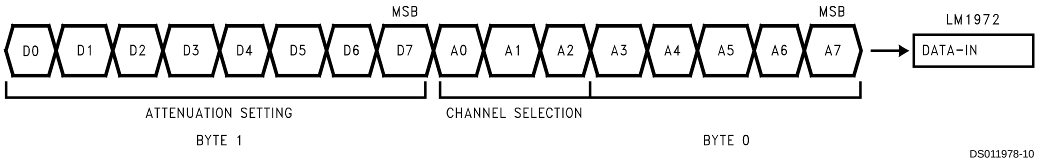


FIGURE 7. Serial Data Format Transfer Process

µPot SYSTEM ARCHITECTURE

The µPot's digital interface is essentially a shift register, where serial data is shifted in, latched, and then decoded. As new data is shifted into the DATA-IN pin, the previously latched data is shifted out the DATA-OUT pin. Once the data is shifted in, the LOAD/SHIFT line goes high, latching in the new data. The data is then decoded and the appropriate switch is activated to set the desired attenuation level for the selected channel. This process is continued each and every time an attenuation change is made. Each channel is updated, only, when that channel is selected for an attenuator change or the system is powered down and then back up again. When the µPot is powered up, each channel is placed into the muted mode.

µPot LADDER ARCHITECTURE

Each channel of a µPot has its own independent resistor ladder network. As shown in *Figure 8*, the ladder consists of multiple R1/R2 elements which make up the attenuation scheme. Within each element there are tap switches that select the appropriate attenuation level corresponding to the data bits in *Table 1*. It can be seen in *Figure 8* that the input impedance for the channel is a constant value regardless of which tap switch is selected, while the output impedance varies according to the tap switch selected.

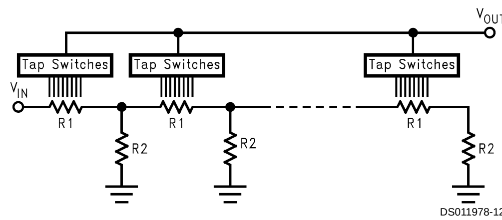


FIGURE 8. µPot Ladder Architecture

DIGITAL LINE COMPATIBILITY

The µPot's digital interface section is compatible with either TTL or CMOS logic due to the shift register inputs acting upon a threshold voltage of 2 diode drops or approximately 1.4V.

DIGITAL DATA-OUT PIN

The DATA-OUT pin is available for daisy-chain system configurations where multiple µPots will be used. The use of the daisy-chain configuration allows the system designer to use only one DATA and one LOAD/SHIFT line per chain, thus simplifying PCB trace layouts.

In order to provide the highest level of channel separation and isolate any of the signal lines from digital noise, the DATA-OUT pin should be terminated through a 2 kΩ resistor if not used. The pin may be left floating, however, any signal noise on that line may couple to adjacent lines creating higher noise specs.

Application Information (Continued)

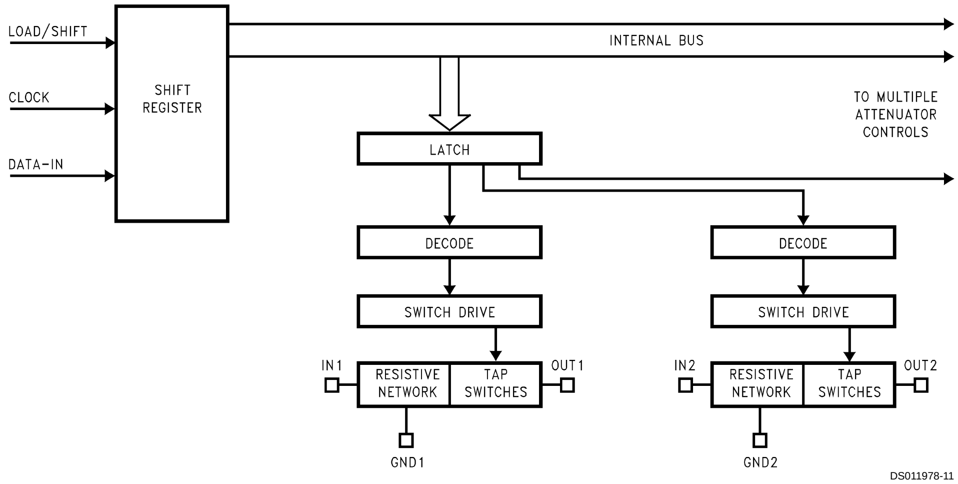


FIGURE 9. µPot System Architecture

DAISY-CHAIN CAPABILITY

Since the µPot's digital interface is essentially a shift register, multiple µPots can be programmed utilizing the same data and load/shift lines. As shown in *Figure 11*, for an n-µPot daisy-chain, there are 16n bits to be shifted and loaded for the chain. The data loading sequence is the same for n-µPots as it is for one µPot. First the LOAD/SHIFT line goes low, then the data is clocked in sequentially while the preceding data in each µPot is shifted out the DATA-OUT pin to the next µPot in the chain or to ground if it is the last µPot in the chain. Then the LOAD/SHIFT line goes high; latching the data into each of their corresponding µPots. The data is then decoded according to the address (channel selection) and the appropriate tap switch controlling the attenuation level is selected.

CROSSTALK MEASUREMENTS

The crosstalk of a µPot as shown in the **Typical Performance Characteristics** section was obtained by placing a signal on one channel and measuring the level at the output of another channel of the same frequency. It is important to be sure that the signal level being measured is of the same frequency such that a true indication of crosstalk may be obtained. Also, to ensure an accurate measurement, the measured channel's input should be AC grounded through a 1 µF capacitor.

CLICKS AND POPS

So, why is that output buffer needed anyway? There are three answers to this question, all of which are important from a system point of view.

The first reason to utilize a buffer/amplifier at the output of a µPot is to ensure that there are no audible clicks or pops due to attenuation step changes in the device. If an on-board bipolar op amp had been used for the output stage, its requirement of a finite amount of DC bias current for operation would cause a DC voltage "pop" when the output impedance of the µPot changes. Again, this phenomenon is due to the fact that the output impedance of the µPot is changing with step changes and a bipolar amplifier requires a finite amount of DC bias current for its operation. As the impedance changes, so does the DC bias current and thus there is a DC voltage "pop".

Secondly, the µPot has no drive capability, so any desired gain needs to be accomplished through a buffer/non-inverting amplifier.

Third, the output of a µPot needs to see a high impedance to prevent loading and subsequent linearity errors from ocurring. A JFET input buffer provides a high input impedance to the output of the µPot so that this does not occur.

Clicks and pops can be avoided by using a JFET input buffer/amplifier such as an LF412ACN. The LF412 has a high input impedance and exhibits both a low noise floor and low THD+N throughout the audio spectrum which maintains signal integrity and linearity for the system. The performance of the system solution is entirely dependent upon the quality and performance of the JFET input buffer/amplifier.

LOGARITHMIC GAIN AMPUFIER

The µPot is capable of being used in the feedback loop of an amplifier, however, as stated previously, the output of the µPot needs to see a high impedance in order to maintain its high performance and linearity. Again, loading the output will change the values of attenuation for the device. As shown in *Figure 10*, a µPot used in the feedback loop creates a logarithmic gain amplifier. In this configuration the attenuation levels from *Table 1*, now become gain levels with the largest possible gain value being 78dB. For most applications 78dB of gain will cause signal clipping to occur, however, because of the µPot's versatility the gain can be controlled through programming such that the clipping level of the system is never obtained. An important point to remember is that when in mute mode the input is disconnected from the output. In this configuration this will place the amplifier in its open loop gain state, thus resulting in severe comparator action. Care should be taken with the programming and design of this type of circuit. To provide the best performance, a JFET input amplifier should be used.

Application Information (Continued)

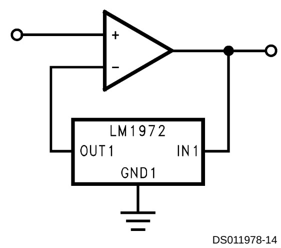


FIGURE 10. Digitally-Controlled Logarithmic Gain Amplifier Circuit

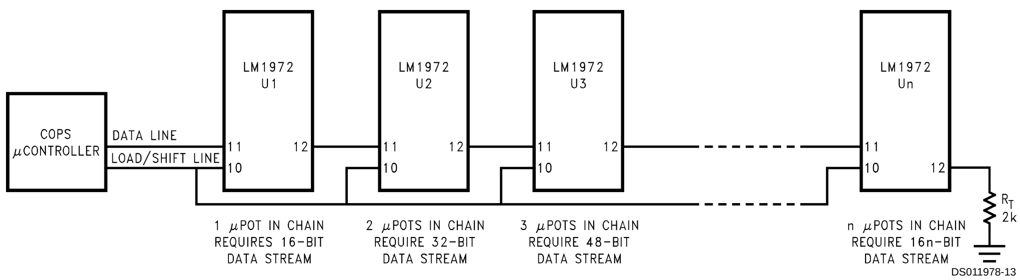
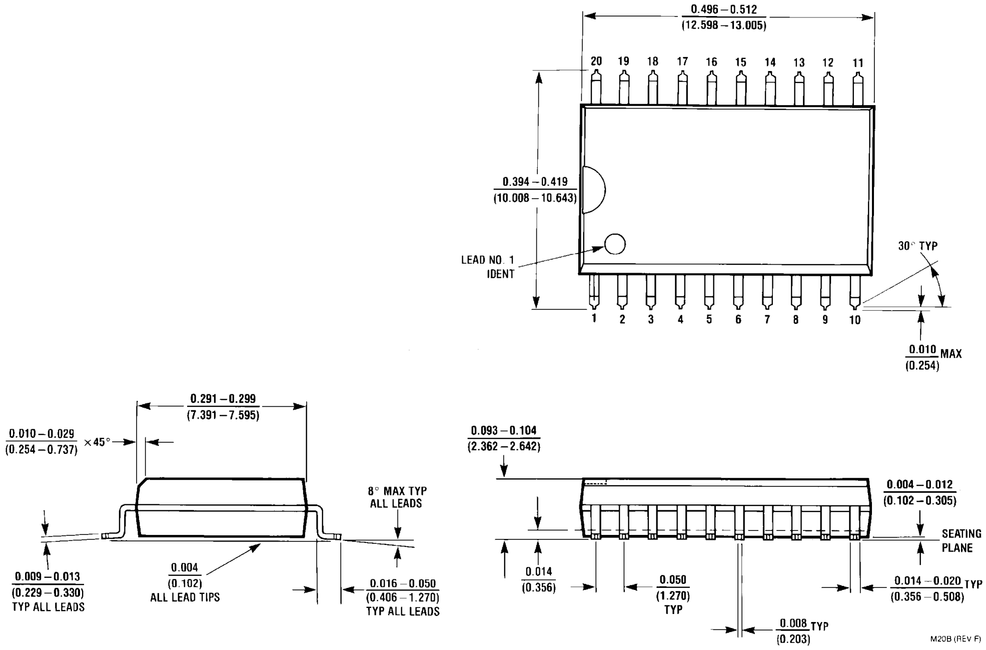
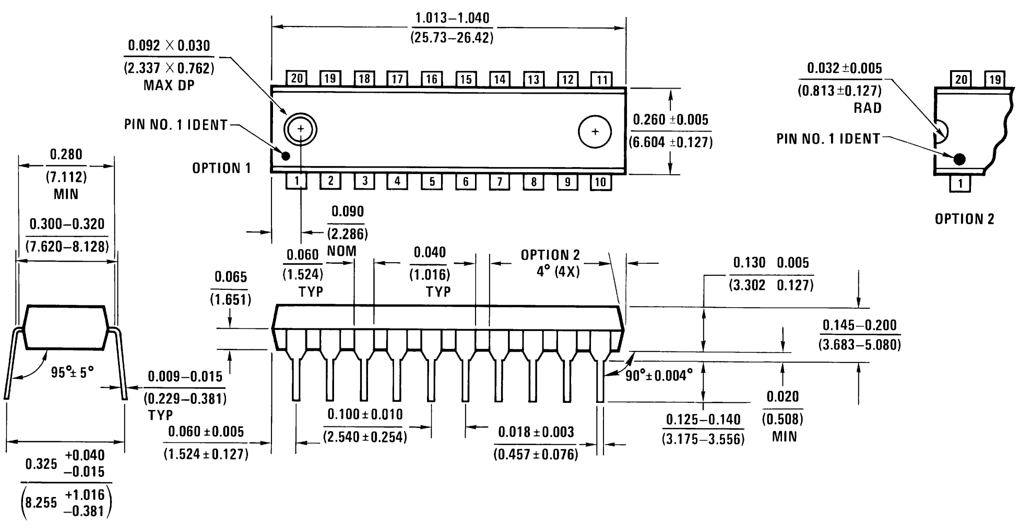


FIGURE 11. n-µPot Daisy-Chained Circuit

Physical Dimensions inches (millimeters) unless otherwise noted



Surface Mount Package
Order Number LM1972M
NS Package Number M20B



Dual-In-Line Plastic Package
Order Number LM1972N
NS Package Number N20A

Notes

National Semiconductor Corporation
Americas
Tel: 1-800-272-9959
Fax: 1-800-737-7018
Email: support@nsc.com

www.national.com

National Semiconductor Europe
Fax: +49 (0) 1 80-530 85 86
Email: europe.support@nsc.com
Deutsch Tel: +49 (0) 1 80-530 85 85
English Tel: +49 (0) 1 80-532 78 32
Français Tel: +49 (0) 1 80-532 93 58
Italiano Tel: +49 (0) 1 80-534 16 80

National Semiconductor Asia Pacific Customer Response Group
Tel: 65-2544466
Fax: 65-2504466
Email: sea.support@nsc.com

National Semiconductor Japan Ltd.
Tel: 81-3-5639-7560
Fax: 81-3-5639-7507