ANALOG DEVICES

AN-224
APPLICATION NOTE

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Input/Output Level Shifting with the AD7769

by John Wynne

The AD7769 contains a fast, 8-bit sampling ADC with two input channels and two 8-bit DACs with output buffer amplifiers. See Figure 1. A unique feature of the device is the input and output signal conditioning circuitry (U.S. Patent No. 4,990,916) which allows the analog input and output signal voltages to be referred to a level other than analog ground. The input range and offset of the ADC and the output swing and offset of the DACs may be adjusted independently by the application of ground-referenced, positive control voltages; V_{BIAS}(ADC), V_{SWING}(ADC) for the ADC inputs and V_{BIAS}(DAC) and V_{SWING}(DAC) for the DAC outputs.

For example, with V_{BIAS}(ADC) = 6 V and V_{SWING}(ADC) = 2 V, the ADC can convert, with full 8-bit resolution, input signals which swing 2 V above and below 6 V. Note that both input channels have the same range. Similarly for the DACs, with V_{BIAS}(DAC) = 5 V and V_{SWING}(DAC) = 3 V, the output voltage of the DACs will swing from 3 V above to 3 V below 5 V. Again both DACs will have the same range.

However, there may be certain applications where the two input signals to be converted have different bias voltage levels or different signal swing ranges. Similarly, it may be necessary to generate DAC output signals which have different bias voltage levels or signal swing ranges. This application note suggests some simple circuits for these situations. Table I summarizes the level shifting operations possible and relates them to particular figures. Voltages $V_{LEVEL\ IN}$ and $V_{LEVEL\ OUT}$ refer to bias voltage levels which are different to V_{BIAS}(ADC) and V_{BIAS}(DAC), respectively. Similarly $V_{SWING\ IN}$ and $V_{SWING\ OUT}$ refer to voltages swings which are different to V_{SWING}(ADC) and V_{SWING}(DAC), respectively. Note that there are two different circuits when changing the signal swing levels at either the input or output. The choice of circuit depends on whether the swing level is being stepped up or stepped down.

	Condition	Circuit
Input Level Shifting	$V_{LEVEL\ IN} \neq V_{BIAS}$(ADC)	Figure 2
	$V_{SWING\ IN} < V_{SWING}$(ADC)	Figure 3
	$V_{SWING\ IN} > V_{SWING}$(ADC)	Figure 4
Output Level Shifting	$V_{LEVEL\ OUT} \neq V_{BIAS}$(DAC)	Figure 5
	$V_{SWING\ OUT} > V_{SWING}$(DAC)	Figure 6
	$V_{SWING\ OUT} < V_{SWING}$(DAC)	Figure 7

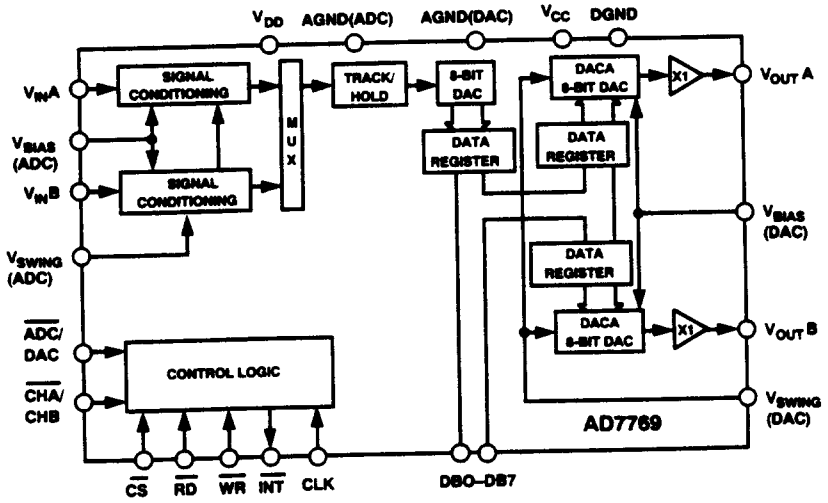

Figure 1. AD7769 Block Diagram

Input Level Shifting Circuits

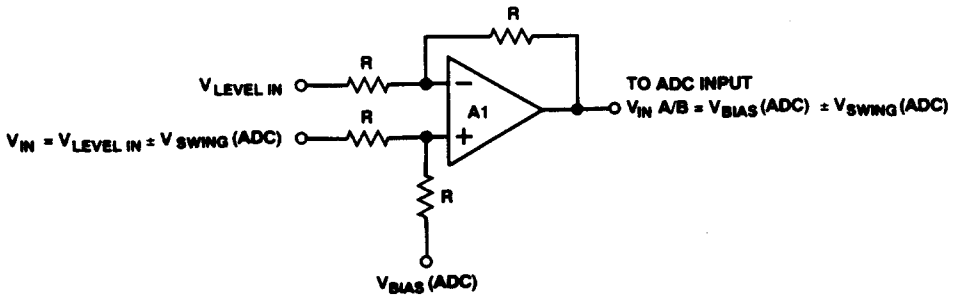

Figure 2. Changing from $V_{LEVEL\ IN} \pm V_{SWING}(ADC)$ to $V_{BIAS}(ADC) \pm V_{SWING}(ADC)$

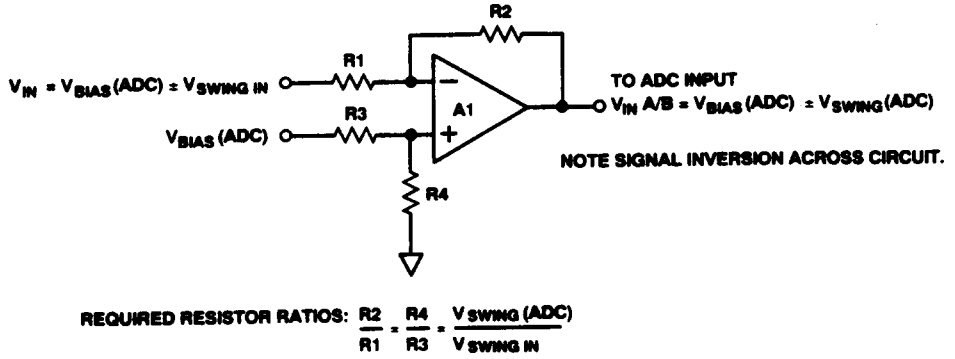

Figure 3. Changing from $V_{BIAS}(ADC) \pm V_{SWING\ IN}$ to $V_{BIAS}(ADC) \pm V_{SWING}(ADC)$ When $V_{SWING\ IN}$ Is Less than $V_{SWING}(ADC)$

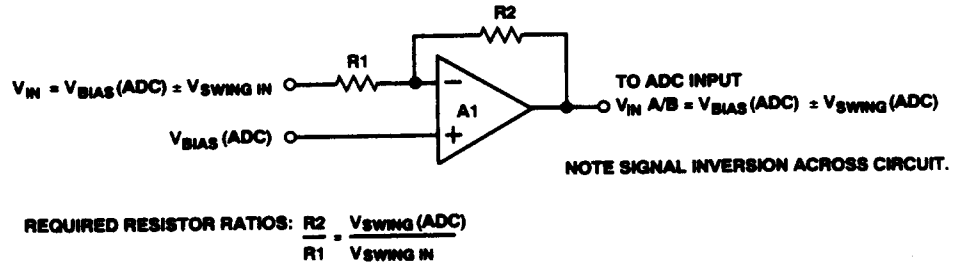

Figure 4. Changing from $V_{BIAS}(ADC) \pm V_{SWING\ IN}$ to $V_{BIAS}(ADC) \pm V_{SWING}(ADC)$ When $V_{SWING\ IN}$ Is Greater than $V_{SWING}(ADC)$

Output Level Shifting Circuits

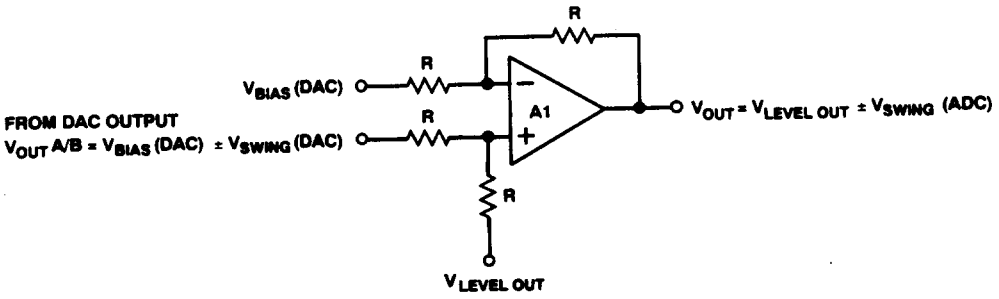

Figure 5. Changing from V_{BIAS}(DAC) ± V_{SWING}(DAC) to $V_{LEVEL\ OUT}$ ± V_{SWING}(DAC)

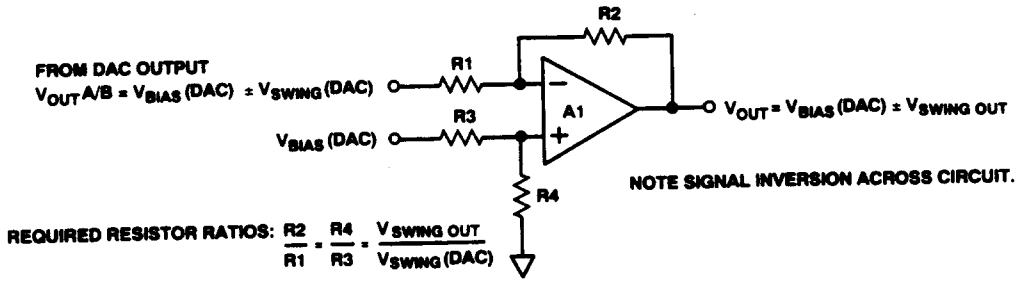

Figure 6. Changing from V_{BIAS}(DAC) ± V_{SWING}(DAC) to V_{BIAS}(DAC) ± $V_{SWING\ OUT}$ When $V_{SWING\ OUT}$ Is Greater than V_{SWING}(DAC)

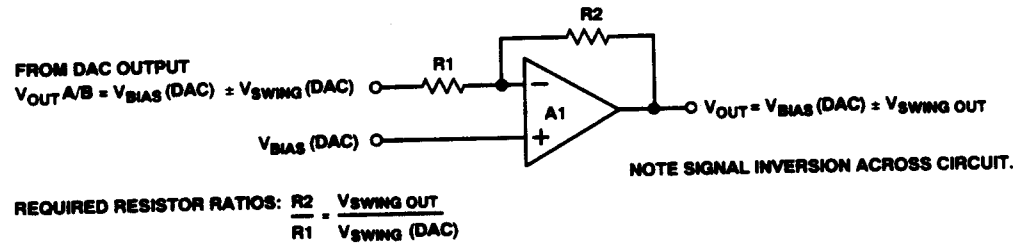

Figure 7. Changing from V_{BIAS}(DAC) ± V_{SWING}(DAC) to V_{BIAS}(DAC) ± $V_{SWING\ OUT}$ When $V_{SWING\ OUT}$ Is Less than V_{SWING}(DAC)