Analog Panning Circuit Provides Almost Constant Output Power

by John Wynne

In audio recording and playback it is often required to split or "pan" a single signal source into a two-channel signal for stereo effects. To locate the signal source as desired in the sound stage, the overall signal power is maintained constant while the relative levels in the derived channels are adjusted. This application note describes a circuit which limits variations in the total output power to ± 0.1dB. It uses two CMOS Multiplying D/A Converters to control the signal levels in the derived channels. CMOS DACs are ideal in this application because of their low distortion. The DACs function as resistive attenuators using thin-film resistors which have low noise and very low voltage coefficient. Converters which are especially suitable for this application are Dual-DACs which contain two CMOS DACs on a monolithic substrate. These are available from Analog Devices with 8-bit resolution (AD7528) or 12-bit resolution (AD7537/47/49).

The simplest and most obvious circuit for panning is shown in Figure 1. The digital data N_B fed to DAC B is the 2's complement of the data N_A fed to DAC A. For n-bit converters the digital input codes, N_A & N_B, can be represented by fractional values, D_A & D_B respectively, where $D_A = N_A/2^n$ and $D_B = N_B/2^n$, with N_A and N_B in decimal format. Because of the 2's complement arrangement between the DACs, the all 0's code or full mute condition is not allowed – in theory at least. The relationship between the two fractional representations, D_A & D_B, is given as:

$$D_A + D_B = 1 \qquad (1)$$

The output voltage expressions for the two channels in Figure 1 are as follows:
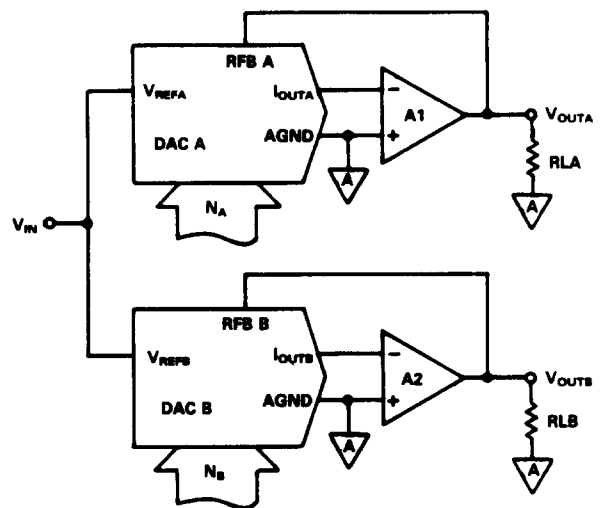
$$V_{OUTA} = -D_A \cdot V_{IN} \qquad (2)$$

Figure 1. Simple Power Splitter Circuit

$$V_{OUTB} = -D_B \cdot V_{IN} \qquad (3)$$

The performance of a 12-bit system is shown in Figure 2 where the total output power level is plotted versus N_A. The 0dB output power level used as the reference level in Figure 2 is the total output power available when $D_A = D_B = 0.5$, the balanced condition. With this simple panning circuit, the total output power level at either extreme of the allowable input code range has increased by 3dB (a doubling of the power) over the power output level at the balanced condition. Load impedances, RLA & RLB, are assumed equal for both channels.
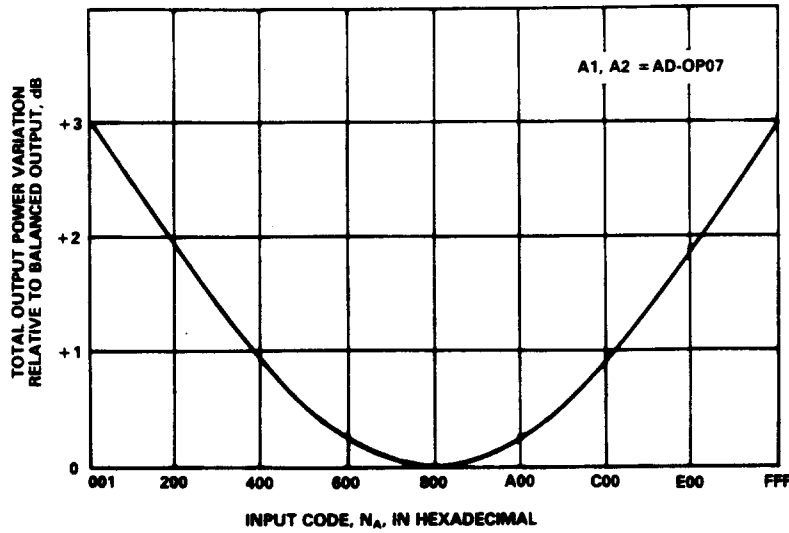
Figure 2. Response of Figure 1 Using 12-Bit DACs

A circuit which avoids this doubling in output power level is shown in Figure 3. The DACs are again driven with 2's complementary data. The output voltage expressions for the two channels are as follows:

$$V_{OUTA} = \frac{-D_A \cdot V_{IN}}{1 + D_A} \qquad (4)$$

$$V_{OUTB} = \frac{-D_B \cdot V_{IN}}{1 + D_B} \qquad (5)$$

Power splitter performance for this circuit when implemented with 12-bit DACs is shown in Figure 4. At the extremes of the input code range the total output power is now only 0.5dB greater with respect to its level at the balanced condition. This amount of output variation would be acceptable in many applications. Certain applications, however, may demand better performance than this.
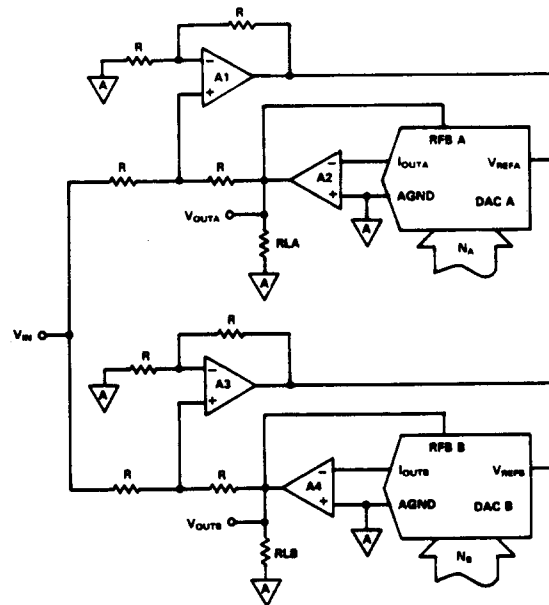

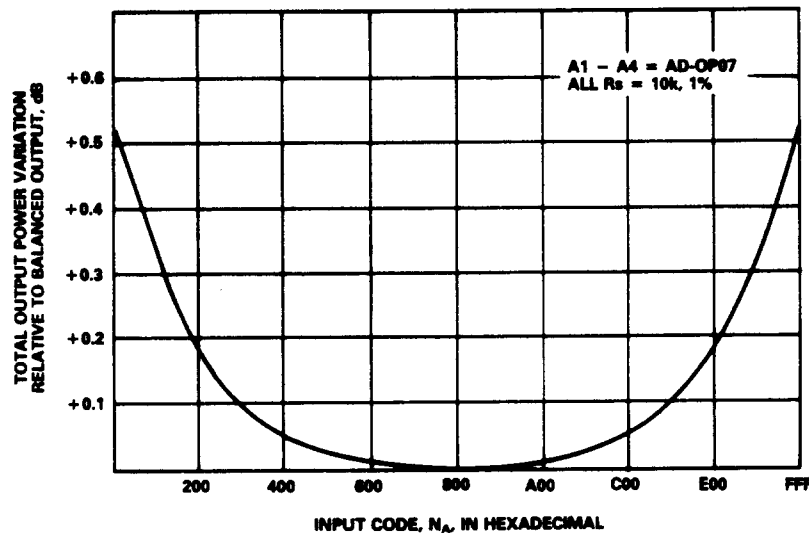*Figure 3. Improved Power Splitter Circuit*

Figure 4. Response of Figure 3 Using 12-Bit DACs

HIGHER PERFORMANCE POWER SPLITTER

A higher performance power splitter circuit can be built by adding some gain around the CMOS DACs of Figure 3. The gain factor required is equal to $\sqrt{2}$.

In order to provide a DAC output voltage which is $\sqrt{2}$ times greater than normal, the effective value of the feedback resistor must be made equal to $\sqrt{2}$ times the DAC ladder impedance R_{DAC}. Reference 1 outlines how additional gain can be added to the standard configuration without requiring a large gain adjustment range or compromising the circuit's temperature coefficient. The circuit configuration of Figure 5 provides the additional $\sqrt{2}$ gain factor. Resistors R1, R2 and R3 should have similar temperature coefficients, but they need not match the temperature coefficient of the DAC. The three resistors are precision (0.1%) metal film resistors with standard EIA/MIL values. When both DAC circuits of Figure 3 are changed to include the gain resistors of Figure 5, the output voltage expressions for the two channels become:

$$V_{OUTA} = \frac{-\sqrt{2} \cdot D_A \cdot V_{IN}}{1 + \sqrt{2} \cdot D_A} \tag{6}$$

$$V_{OUTB} = \frac{-\sqrt{2} \cdot D_B \cdot V_{IN}}{1 + \sqrt{2} \cdot D_B} \tag{7}$$

$$V_{OUT} = V_{IN} \cdot \left(\frac{N}{2^n}\right) \cdot \left(1 + \frac{R1}{R2}\right)$$

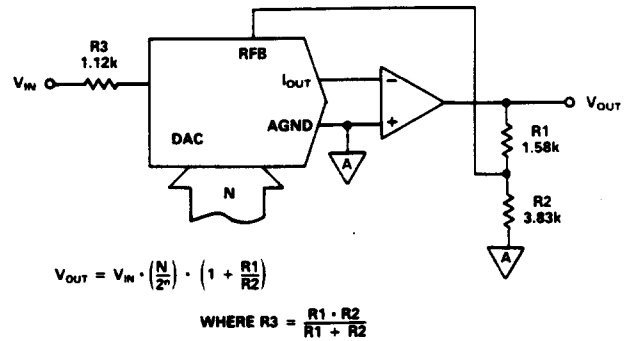$$\text{WHERE R3} = \frac{R1 \cdot R2}{R1 + R2}$$

Figure 5. Additional Resistors to Provide $\sqrt{2}$ Gain Factor

The performance of the revised circuit is shown in Figure 6. The total power output at either extreme of the input code range is equal to the total power output at the balanced condition. The output power level remains constant within a ±0.1dB error band. With the exception of R1, R2 and R3, all resistors are metal film, 10kΩ, 1% tolerance.
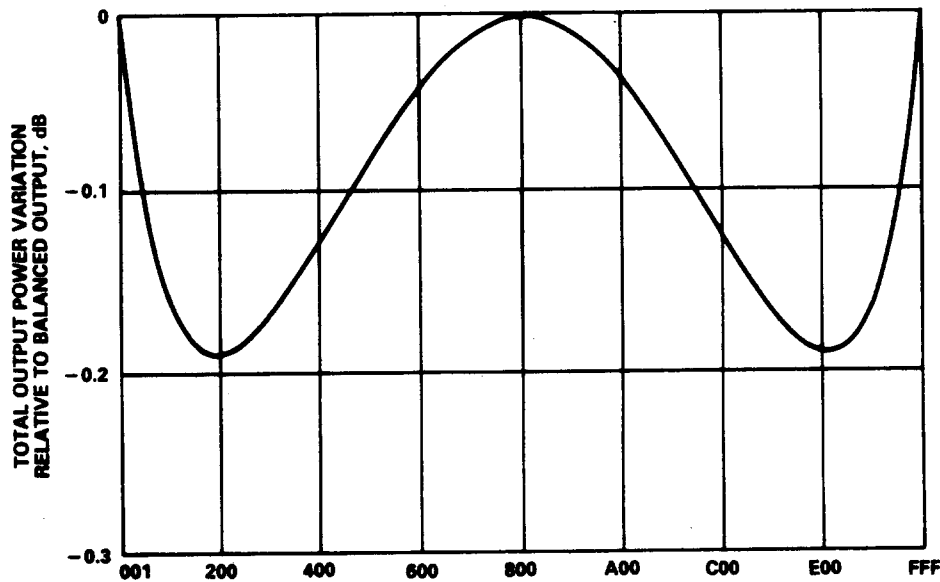

Figure 6. Response of Figure 3 Using $\sqrt{2}$ Gain Factor

STAND-ALONE APPLICATIONS

Many applications which are microprocessors-based will have no difficulty in generating the 2's complement data required for the previous power splitter circuits. It is also possible in non-microprocessor-based systems to perform the 2's complement operation with dedicated hardware. If either of these approaches are unsuitable, for whatever reason, it is still possible to build a power splitter circuit by rewiring one of the DAC channels and driving both DACs with identical data. Figure 7 shows the rewiring and the additional circuitry required to achieve this.

The output expressions for the two channels are now:

$$V_{OUTA} = \frac{-D \cdot V_{IN}}{1 + D} \tag{8}$$

$$V_{OUTB} = \frac{-(1-D) \cdot V_{IN}}{2 - D} \tag{9}$$

The performance of Figure 7 is identical to that of Figure 3. Additionally, the circuit performance can be upgraded in a similar fashion as previously described for Figure 5.
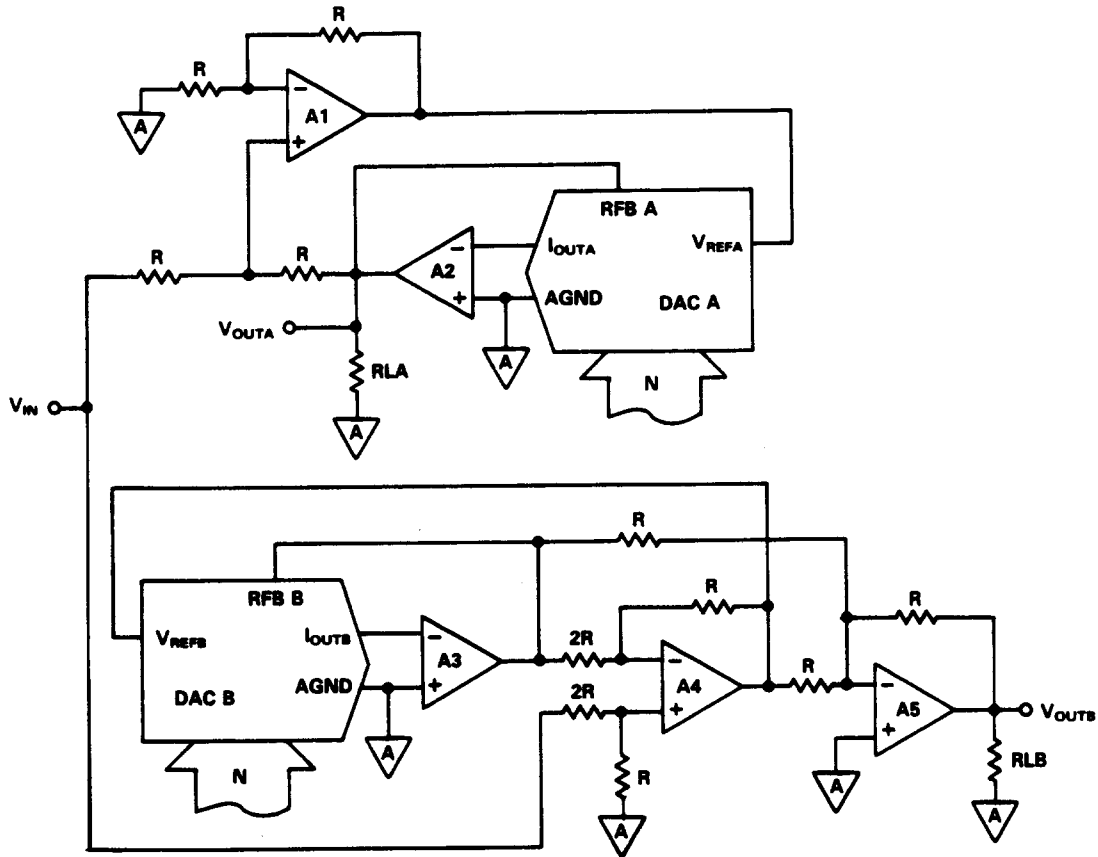

Figure 7. Power Splitter Circuit with Identical DAC Data, N

REFERENCES
1. Brokaw P., "Input Resistor Stabilizes MDACs Gain".
   EDN, January 7, 1981, pp.210-211.