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APPLICATION NOTE

ONE TECHNOLOGY WAY • P.O. BOX 9106 • NORWOOD, MASSACHUSETTS 02062-9106 • 617/329-4700

JFET-Input Amps Are Unrivaled for Speed and Accuracy

by Peter Henry

JFET-input amplifiers provide an economical means of achieving high accuracy in applications that need wide bandwidths for large signals. They are ideal for pulse amplifiers, fast D/A converters, peak detectors, and logarithmic amplifiers.

JFET-input operational amplifiers are an option for designers who require speeds greater than those provided by standard bipolar op amps such as the OP-07. The high slew rates of JFET-input amplifiers make these devices attractive for pulse amplification and other applications that require wide bandwidths and handle large signals. Their low bias currents make them equally suitable for peak detectors and logarithmic amplifiers. Furthermore, their fast settling rates make them ideal for fast, high-precision DACs.

To obtain the full performance of which JFET-input amplifiers are capable, you'll need to take all the standard precautions in designing and laying out your pc boards, along with a few extra precautions that are specific to JFET-input devices (see "Caveats, warnings, and design reminders").

A JFET-input amplifier can help a CMOS D/A converter achieve a fast settling time while converting the DAC's current output into voltage levels and reducing output impedances. You'll obtain the fastest settling times from bipolar DACs, because they have lower output capacitance than their CMOS counterparts, but CMOS devices have the advantages of low price and the availability of a wide variety of interface options. The primary disadvantage of CMOS DACs is their large output capacitance, which can be 50 to 120 pF for an 8-bit DAC, and as much as 70 to 150 pF for a 12-bit DAC. This large capacitance increases the settling time. However, if you add a JFET-input amplifier (such as PMI's OP-42) to create a voltage output, you can compensate for the DAC's output capacitance. A CMOS DAC will then settle in approximately 3μs to within 0.01% of a 10V full-scale output step.

The offset voltage of many older JFET amplifiers suffered from large thermal drifts. However, newer state-of-the-art precision JFET-input amplifiers exhibit relatively little drift with temperature, and the resulting output error is generally insignificant unless you operate the amplifier at a high gain level. If your application requires the minimum possible offset error, however, you can use a servo loop that automatically corrects offset-voltage and drift errors. In Figure 1's circuit, for example, IC_1 multiplexes eight analog channels to the input of an OP-42 or OP-44 amplifier, which has a gain of 100. One of the analog channels grounds the amplifier input in order to correct for V_{OS} (offset) errors; the other channels are available for signals.

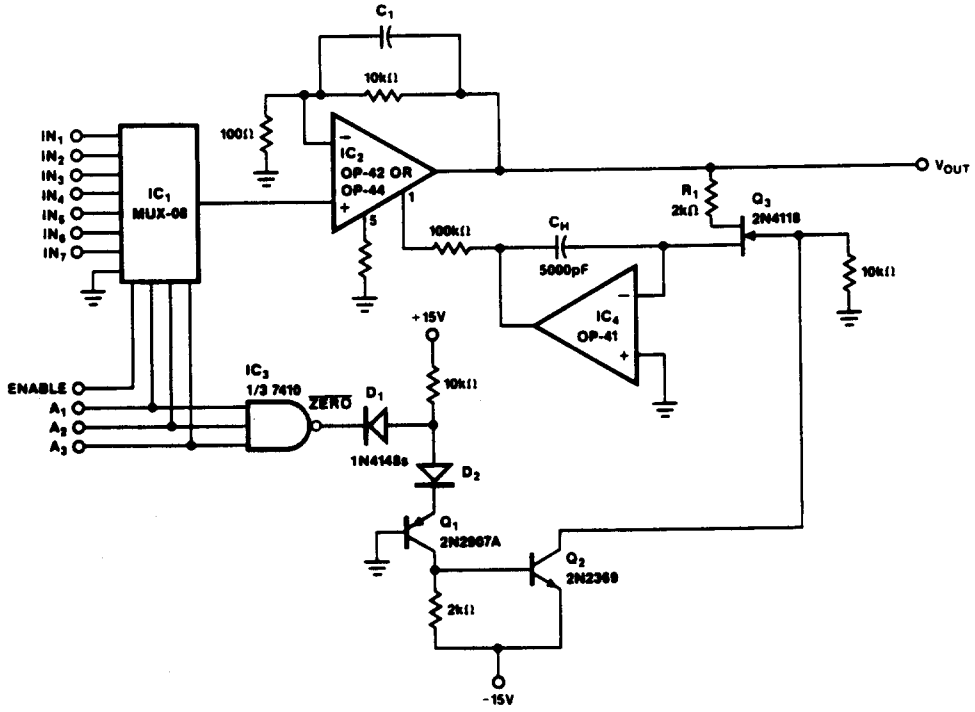

FIGURE 1: *This autozeroing amplifier multiplexes seven inputs to a common output. The eighth input grounds the input of IC_2 to zero the amplifier's offset voltage. Before you select a signal, hold the three address lines high for 200μs to ensure proper zeroing.*

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To correct V_{OS} errors during a conversion, you first drive the three multiplexer-address lines (A_1 — A_3) high, so that multiplexer IC_1 grounds the input of JFET-input amplifier IC_2. At the same time, AND gate IC_3 drives the $\overline{Zero}$ line low and thereby causes the switching circuitry consisting of transistors Q_1 and Q_2 to turn on JFET switch Q_3. This action connects JFET-input amplifier IC_4 into the feedback path of IC_2 via that IC's null pins (1 and 5) and thereby forces the output of IC_2 to assume the value of the offset voltage at the input of IC_4. The current in the feedback loop then develops a voltage across hold capacitor C_H.

KEEP LEAKS AWAY FROM CORRECTION CIRCUITRY

After a time period that's determined by the RC time constant of R_1C_H and the current through Q_3, you can change the multiplexer address so that the $\overline{Zero}$ line goes high and turns off Q_3. The voltage across C_H holds the output of IC_4 (which is also the offset-voltage compensation for IC_2). IC_1 has a relatively long switching time, so Q_3 turns off before IC_1 connects a new input to IC_2; consequently, the signal cannot leak into offset-correction circuits.

If you use the component values shown in Figure 1, you should make sure that the $\overline{Zero}$ line remains low for at least 200μs to ensure proper nulling. You can achieve a faster nulling time by using a JFET switch that has a higher I_{DSS}, such as a 2N4393, but you'll do so at the expense of increased leakage and faster droop. Some error is induced by charge injection through Q_3 into C_H, but you can minimize this error by using a large value of C_H.

To minimize droop at the output of IC_4, make sure that hold capacitor C_H is a low-leakage type (such as a polystyrene device). For higher precision, add a potentiometer to null the offset voltage of IC_4. When you use the component values shown, the droop of the offset voltage at 25°C is only 1.3μV/s. Near the center of the adjustment range, each 100mV of swing at the output of IC_4 will cause a shift of 150μV in the V_{OS} of IC_2. The circuit is capable of correcting as much as 10mV of offset, so that it can handle some system offsets in addition to IC_2's offset.

YOU CAN SUBSTITUTE DIGITAL CORRECTION

If your application requires digital correction of the offset voltage, you can substitute an ADC/DAC combination for IC_4. With this scheme, when you ground IC_2's input, the ADC digitizes the IC's output (offset) voltage and passes a correction factor to the DAC, which in turn applies an analog nulling voltage to pin 1 of IC_2. This modification is of value in applications that digitize the output of IC_2, and it has the advantage that digital correction circuits do not droop with time. However, the scheme is a needless complication in systems that do not include a μP for other purposes.

The level-shifting circuitry (D_1 and D_2, Q_1 and Q_2) converts a TTL signal to the levels necessary to drive JFET switches, and you can use the same circuit in a wide variety of applications. When the TTL input signal ($\overline{Zero}$) goes low, it turns off transistor Q_1. This action forces the base of transistor Q_2 to −15V, turning off Q_2 and holding the gate of Q_3 at ground level. While these conditions continue, Q_3 presents a low impedance to the signal applied to it through R_1. Consequently, the inverting input of IC_4 follows the output signal of IC_2, and IC_2 charges C_H.

When the TTL $\overline{Zero}$ signal goes high again, it turns on Q_1 and Q_2, which in turn pull the gate of Q_3 to −15V. This action puts Q_3 into a high-impedance state, so that the switch disconnects the input of IC_4 from the output of IC_2, and IC_2 maintains the charge across C_H.

FAST S/H AMPLIFIER EXHIBITS 0.01% ACCURACY

The characteristics of JFET-input amplifiers make them natural choices for fast sample-and-hold (S/H) amplifiers. Figure 2a's circuit has an aperture time of 80ns and can acquire a 10V step in less than 1μs with an accuracy of 0.1%, and in 2μs with an accuracy of 0.01%. The corresponding settling times are 100ns and 300ns, respectively.

The $\overline{Sample}$/Hold control-input circuit uses the same level-shifting circuit used by the autozero circuit described above, with the addition of a Schottky clamping diode (D_3) and a pullup resistor R_1 to accelerate transitions. Diodes D_4 and D_5 prevent the forward-biasing of JFET switches Q_3 and Q_4. During the sampling time, the JFET switches conduct, so that amplifiers IC_1 and IC_2 both operate at unity gain and IC_1 charges hold capacitor C_{H1}. The V_{OUT} signal precisely tracks the V_{IN} signal.

When you switch the control line to the hold mode, the JFET switches present a high impedance, so that Q_3 disconnects the output of IC_1 from the input of IC_2, and Q_4 allows IC_2 to charge hold capacitor C_{H2}. The charges on the two hold capacitors then cause IC_2 to maintain the V_{OUT} signal at the sampled value.

MATCHED COMPONENTS REDUCE ERRORS

The low bias current of the JFET-input amplifiers and the low leakage of the JFET switches combine to minimize leakage of the charges on C_{H1} and C_{H2}. Furthermore, you can closely match the remaining leakage by matching the capacitor values and by using a matched pair of JFET switches contained in the same housing. This configuration has two advantages. First, it matches the amounts of charge injection through the switches into capacitors C_{H1} and C_{H2} and thereby considerably reduces the hold step. In fact, adjusting a trimmer capacitor connected in parallel with one of the hold capacitors will let you reduce the hold step below 1mV.

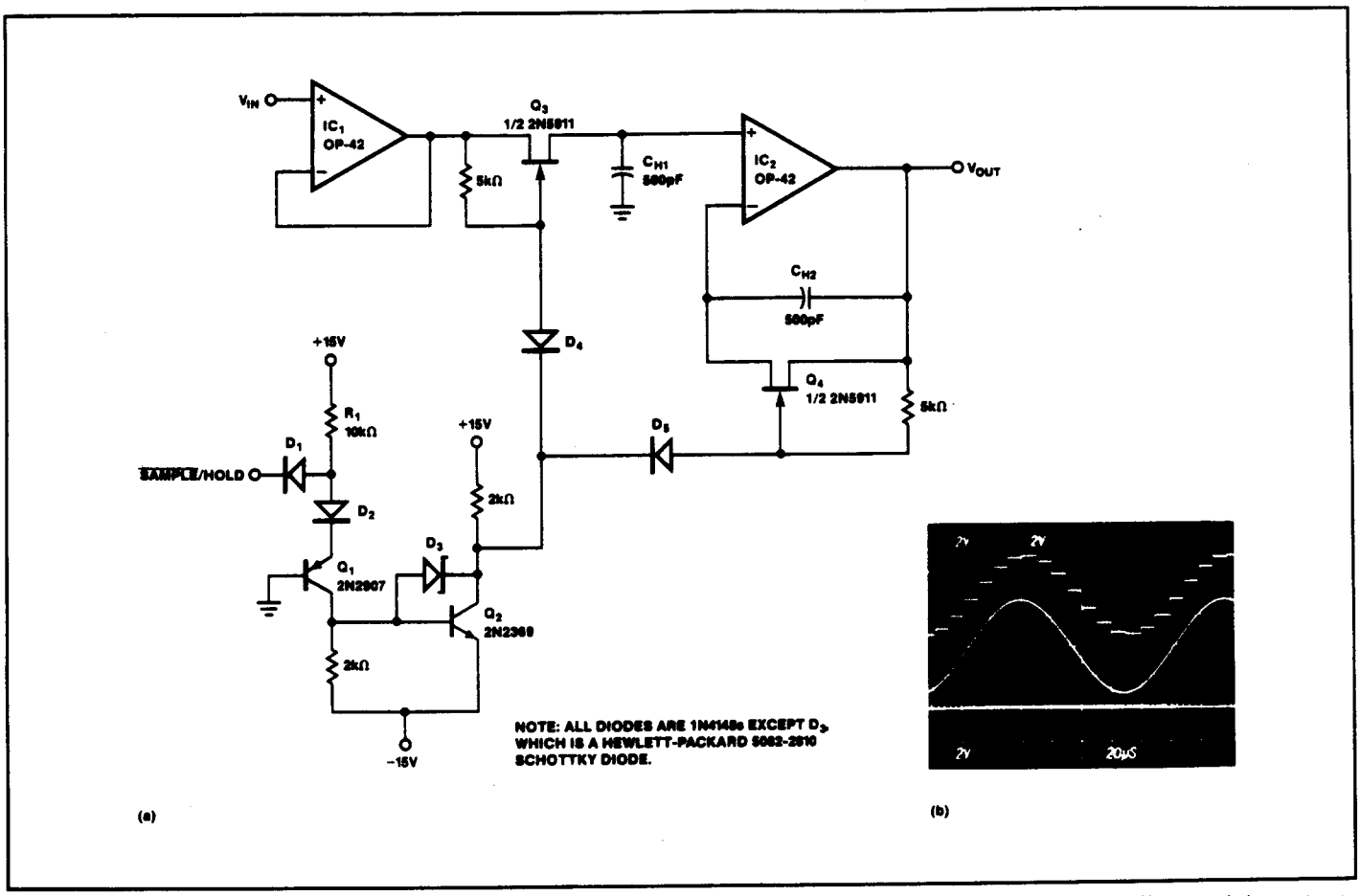

FIGURE 2: *This fast sample/hold amplifier (a) uses two hold capacitors to minimize both the hold-step effect and the output droop. You can see the very small hold step and the absence of droop in the scope photo (b).*

Second, the scheme causes the I_{OS} of IC_2 and the leakage through the matched JFET switches (rather than absolute leakage levels) to control the voltage droop at the output terminal. Furthermore, the output voltage is controlled by the differential voltage between the two capacitors. The absolute voltages across the capacitors droop because of IC_2's bias current, but both droop at the same rate, making this voltage change appear as a common-mode effect. The differential voltage is controlled by I_{OS}, which is usually much smaller than I_B. IC_2 can maintain a constant output voltage, even though the actual voltage levels on the two capacitors may change considerably during the hold period. In Figure 2a's circuit, this scheme reduces the droop rate to 7μV/ms. Figure 2b shows a sine wave applied to the S/H circuit, and the resulting samples at the output.

The control provided by these differential voltages breaks down when their absolute values fall below the minimum input voltage of IC_2. However, that condition will typically not occur until several seconds have elapsed. You can reduce both the hold step and the droop rate even more by using larger values for the capacitors, but you'll then sacrifice some speed. (For more on the examination of errors, see "Calculating error magnitudes.")

You can exploit the low bias currents inherent in a JFET-input amplifier to create a fast peak detector (Figure 3a) that an capture a 10V peak only 2.5μs wide. This circuit uses the level shifter employed by the two previous circuits, but it does not drive any FET switches. Instead, a Reset command causes Q_2 to discharge hold capacitor C_H directly.

After a reset operation, the voltage across C_H is negative, so the circuit will detect very small peaks even if the ac signal has a negative dc offset. Be aware, however, that the reset method prevents this circuit from detecting negative peaks. The droop rate is 3mV/ms and is mainly due to leakage of the charge on C_H through Q_2; diode D_5 contributes very little charge leakage, because it operates with only a small voltage across it. The action of the circuit is illustrated in Figure 3b.

You'll find that JFET-input amplifiers yield excellent performance in logarithmic amplifiers. Figure 4's circuit follows the usual log-amp configuration, in which the logarithm (to base 10) of the input voltage is derived from the differential between the threshold voltages of two transistors (Q_1 and Q_3). A precision reference source (IC_2) sets the collector current of Q_3, and the input voltage controls the collector current of Q_1. You can derive the threshold voltages (V_T) of the transistors using the following equation:

$$V_T = (kT/q)\ln(I_C/I_S),$$

where q is the electronic charge, T is the temperature, and k is Boltzmann's constant. The difference in V_T between the two transistors is then

$$\Delta V_T = (kT/q)\left[(\ln I_{C1}) - (\ln I_{C3})\right].$$

The output voltage is ΔV_T multiplied by a factor appropriate to your application. The circuit scales the output for 1V per decade with a zero-crossing at an input voltage of 100mV. For a V_{IN} greater than zero, this configuration yields a transfer function of

$$V_{OUT} = -\left[\log(V_{IN}/R_{IN}) + 4\right]$$

(for V_{OUT} in volts and the quantity V_{IN}/R_{IN} in amps). The circuit operates correctly for inputs from 1mV to more than 10V.

The above equations show that the temperatures of the log-conversion transistors have a direct effect on the output voltage. Conventional circuits provide temperature correction by using a thermistor instead of a resistor in place of R_7. This circuit uses a special method to provide an isothermal environment for the log-conversion transistors.

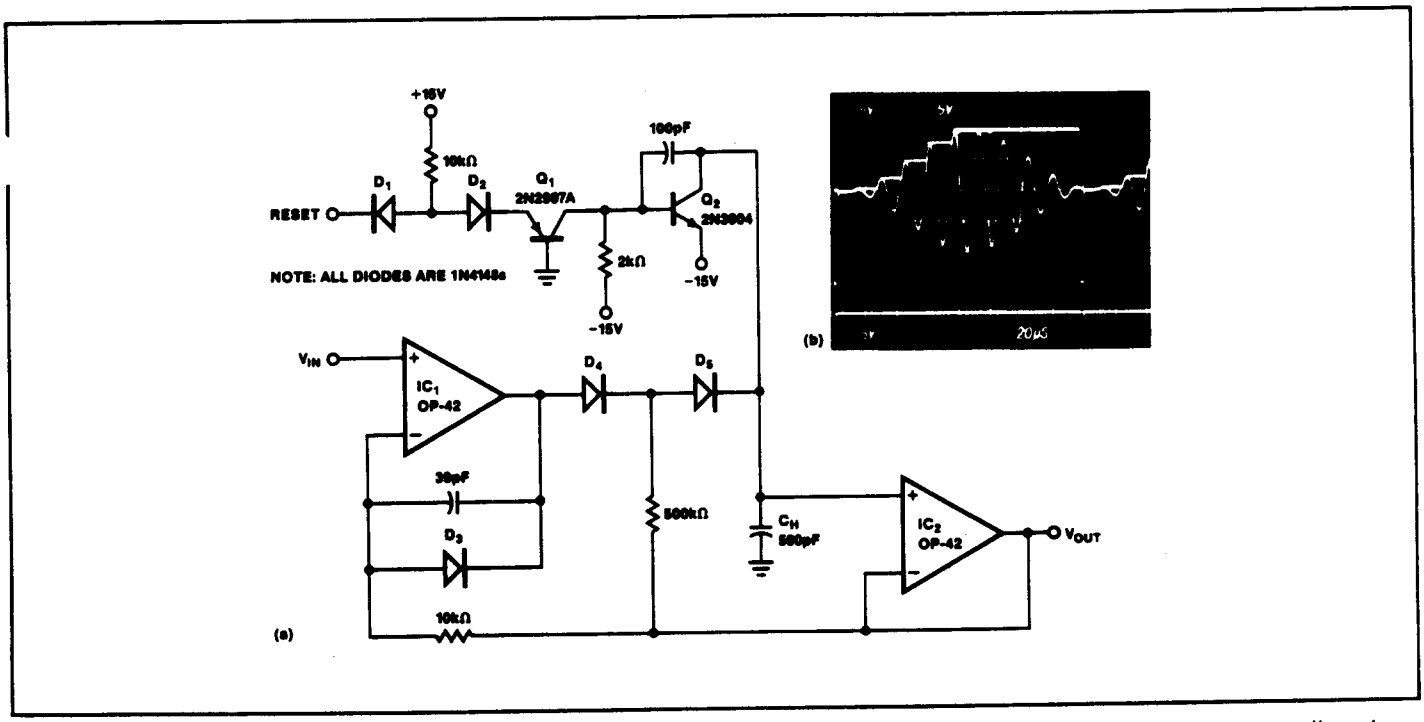

FIGURE 3: *This peak detector (a) can capture a 10V peak that's only 2.5μs wide. After a reset it can detect very small peaks even if the ac signal has a negative dc offset. The detector's JFET-input amplifiers have very low input bias currents and therefore minimize leakage from the hold capacitor. This low leakage is responsible for the absence of droop (b).*

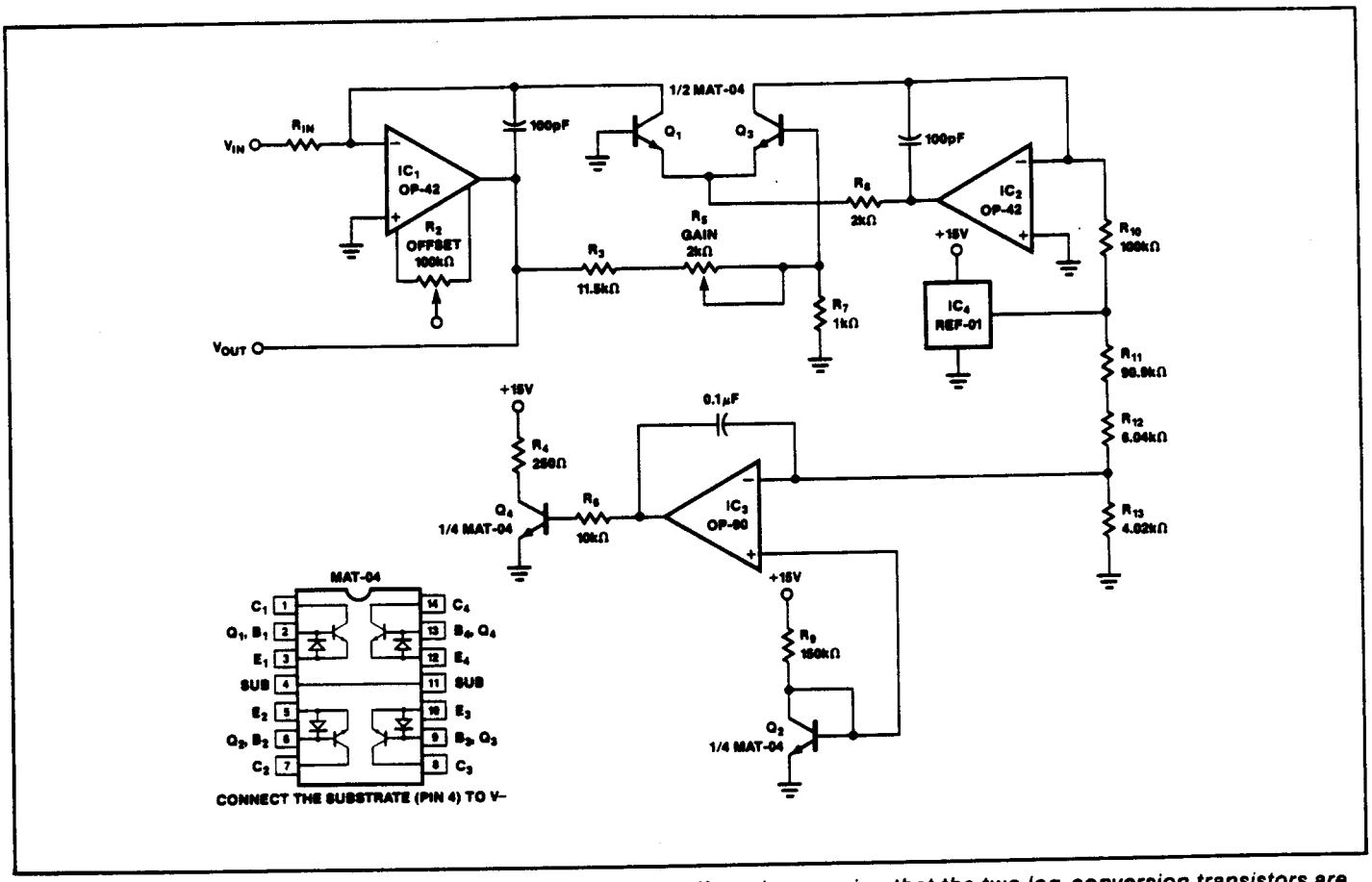

FIGURE 4: *This logarithmic amplifier eliminates temperature effects by ensuring that the two log-conversion transistors are always at the same temperature. The conversion transistors are on the same substrate as a heater transistor and a temperature sensor, which are connected to each other in a feedback loop.*

The MAT-04 IC used in this circuit is a symmetric array of four transistors placed at the corners of a square die. Two of these transistors, located at diagonally opposite corners, act as the log-conversion elements. Of the remaining two transistors, one (Q_4) acts as a heater and the other (Q_2) acts as a temperature sensor. IC_3 forces the V_T of Q_2 to a specific value by varying the current through Q_4, and it maintains this value by means of the thermal feedback between Q_2 and Q_4. The symmetrical layout of the IC ensures that the two log-conversion transistors are always at exactly the same temperature. The component values shown will maintain the MAT-04 die at approximately 60°C.

This operation may violate the rated specifications of the MAT-04 package and cause degradation of Q_4's β, but it does not hurt performance, because the characteristics of the heater are unimportant. You'll get the best results by encasing the MAT-04 package in thermally insulating foam, such as the urethane foam used for housing insulation.

To null the amplifier, you begin by setting the input voltage to 1mV. Adjust the offset voltage of IC_1 for an output of 3V. Next, raise the input to 10V and adjust the gain for an output of –1V. These two adjustments are interactive, so you may have to repeat them several times. You can modify the zero-crossing point by changing the value of resistor R_3.

CAVEATS, WARNINGS, AND DESIGN REMINDERS

The following design principles are critical for the performance of any high-speed amplifier. They are included here as a check list.

- — Use separate supply traces and grounds for each amplifier.
- — Bypass each supply, right at each amplifier, with a 1 to 10μF tantalum or electrolytic capacitor connected in parallel with a glass or ceramic capacitor that has a value of 0.01 to 1μF.
- — Provide separate supply lines and ground lines for the digital and analog sections of your system.
- — Switching power supplies can inject spikes of several hundred millivolts into the supply lines, and they can radiate EMI. Shield the analog sections and bypass all supply lines at the point where they enter the shielded enclosure.
- — Be careful not to exceed an amplifier's maximum input-voltage specification. If a signal could be applied before the amplifier's supplies reach their full values, provide clamping diodes — but remember that these devices add leakage and capacitance to the circuit.
- — Be careful not to exceed the maximum junction temperature or the maximum power-dissipation ratings of an amplifier. If you connect a capacitive load to the output of an op amp, be sure to include in your calculations the power dissipation caused by the rms ac currents delivered to the load.
- — Internal power dissipation raises an IC's junction temperature. You can find the amount of the increase from the formula $\Delta T = P_D \theta_{JA}$, where P_D is the power dissipation and θ_{JA} is the thermal resistance of the package. For 8-pin packages lacking a heat sink, this parameter varies from 90°C/W (plastic DIP) to 200°C/W (TO-99 can). The junction temperature is the ambient temperature plus ΔT.

PRECAUTIONS FOR JFET AMPS

The following design principles also have general application, but the focus here is on their implications for designing with JFET-input op amps.

First, remember that a rise in junction temperature increases the bias current of a JFET-input op amp; a rise of 10°C may double the bias current. JFET-input op amps have a naturally low bias current, however; for PMI's OP-42, for example, the current is only 200pA at room temperature and less than 20nA over the full military temperature range. The errors produced by such small currents are usually insignificant; at a slew rate of 100V/μs, you would need a current of 1mA to drive stray capacitances amounting to only 10pF. Although some JFET-input op amps use cancellation methods to derease bias current, these techniques can create excessive phase shifts in high-speed amplifiers.

Remember also that the slew rate of an op amp varies according to the voltage difference between its two inputs. If you want to achieve the maximum slew rate specified in the data sheet, you must ensure a difference of about 2V between the inputs of a JFET-input op amp so that one side of the op amp's differential-input circuit turns completely off. At unity gain, such voltages are normal, but in circuits that have a higher gain, the input-voltage levels —and hence the slew rate — decrease. A JFET-input op amp that yields a slew rate of 60V/μs at unity gain might yield only 20V/μs if you operate it at a gain of 100 with a ±100mV input signal.

You should also keep in mind that an amplifier that has a high slew rate or a wide bandwidth doesn't necessarily settle fast. Many amplifiers with high slew rates obtain their speed at the cost of inducing excessive ringing in the output waveform; this ringing increases the settling time. Remember, too, that the ac characteristics of some amplifier types vary widely from part to part. Data sheets usually specify a typical settling time. Very few vendors guarantee a maximum value.

VARYING COMPENSATION

Most JFET-input op amps have input capacitances from 4 to 8pF. A small capacitor placed across the feedback resistor compensates for the pole created by the input capacitance. The amount of compensation needed depends on the performance you expect from the amplifier. Critical damping may give the fastest settling times to within very narrow error bands. In general, however, you'll improve the settling time, even to error bands as small as 0.01%, by providing compensation that yields slight underdamping. The optimum compensation is a function of the circuit and its layout, and you'll have to determine its value by experiment.

Proper compensation becomes critical when you use an op amp to convert the current output of a DAC to a voltage output. The output capacitance of the DAC, in parallel with stray capacitance and the input capacitance of the op amp, exacerbates any ringing and instability problems and you'll have to optimize the compensation for the combination of settling speed and accuracy that you want.

The gain-bandwidth product (GBW) is adequate to describe the ac response, at any frequency, of single-pole amplifiers such as the 741. The more complex design of a JFET-input op amp such as PMI's OP-42 yields higher slew rates with greater stability, but it distorts the meaning of the GBW. Nevertheless, you can derive an approximation of the cutoff frequency for any closed-loop gain (A_{VCL}) from the following formula:

$$f_C = (GBW/A_{VCL}).$$

This approximation is adequate for most purposes and is valid for most amplifiers, including PMI's OP-42 and OP-44.

The slew rate (SR) of an amplifier largely determines the maximum frequency at which it can operate with large

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CAVEATS, WARNINGS, AND DESIGN REMINDER *Continued*

signals. You can calculate this frequency (known as the power bandwidth, or BW_P) from the equation $BW_P = SR/(\pi V_{p-p})$. An amplifier such as the OP-42, which has a 50V/μs slew rate, can operate at frequencies above 800kHz with only 1% distortion on a $20V_{p-p}$ signal. The OP-44 has a BW_P that's greater than 1.5MHz; it achieves a slew rate of 100V/μs in applications that have a closed-loop gain greater than three.

PMI's OP-42 guarantees settling times of 1μs or less to an accuracy of 0.01% — that is, to within ±1mV error bands — for a 10V input step. You can approximate settling times for input steps other than 10V by subtracting the slew time from the specification and adding the slew time for the desired output change. For example, to obtain the settling time for a 1V step, subtract the slew time for 10V (167ns at 60V/μs) from the 800ns typical settling time. To this result (800 – 167 = 633ns) add the slew time for 1V (16.7ns) to obtain a calculated settling time of approximately 650ns to 0.01%. The OP-42's measured settling time for a 1V step is somewhat better, being less than 600ns.

CALCULATING ERROR MAGNITUDES

For a concrete example on which to base an examination of errors, assume a circuit consisting of the autozeroing amplifier of Figure 1 as the first stage, and the S/H amplifier of Figure 2 as the second stage. Provide zeroing pulses to the amplifier in the first stage once every milli-second to eliminate thermal drifts and offset problems.

For the purposes of this discussion, assume that IC_2 is a PMI OP-44, with a GBW of 50MHz (think of the entire circuit of Figure 1 as this gain stage). Because IC_2 operates with a gain of 100, the system bandwidth is 500kHz before signals enter the S/H amplifier. The S/H circuit yields 2.5μs acquisition times and holds the output for 18μs; consequently, the sampling bandwidth is 50kHz. Assume that the power supplies are well regulated so that you can ignore power-supply rejection. Also, ignore phase errors.

ASSESSING GAIN-STAGE ERRORS

In the first stage, errors arise primarily from finite gain, common-mode rejection (CMR), and noise. Servo amplifier IC_4 nulls IC_2's offset voltage and drift; these values are no greater than 1mV over the full temperature range, without additional adjustment. The drift is negligible during the periods between nulling. IC_4 also nulls the offset voltage caused by bias current flowing through the multiplexer. If you assume that source impedances are no greater than 1kΩ, then the contribution traceable to bias current is less than $1.5\mu V \times A_{VCL}$, or an additional 1.5mV. (This includes leakage current from the switches in the MUX-08.) At dc, the common-mode error is only 0.004% (essentially nonexistent), but at 50kHz the CMR falls to 70dB and can contribute an error of 0.03%.

You can express open-loop gain errors as a percentage of the signal; at dc, these errors are approximately equal to the percentage calculated from A_{VCL}/A_{VOL}. Both the OP-42 and the OP-44 have an open-loop gain of more than 500,000. At dc, the gain error is less than 0.02%, but at 50kHz, gain errors can contribute amplitude errors as high as 0.5%. The amplitude error decreases rapidly as the operating frequency moves away from the 500kHz cutoff frequency (f_C).

You can obtain an approximate value of the error, for any frequency f, from the formula

$$\epsilon_A \approx 1/2(f/f_C)^2,$$

down to the frequency at which the formula yields a value that's less than the dc value. In Figure 1's circuit, this point occurs at 10kHz. Because the amplitude error is primarily a function of f_C, operating the amplifier at a lower closed-loop gain would result in a significantly smaller error at any given frequency.

You can calculate the noise by multiplying the square root of the bandwidth by the rms noise density. In a wideband amplifier, the noise is dominated by the high-frequency flatband noise, rather than by the higher-density low-frequency noise. For PMI's OP-42 amplifier, the flatband-noise density is typically $12nV/\sqrt{Hz}$. To get an idea of the worst-case performance, use $15nV/\sqrt{Hz}$, which yields a value of 10.6μV rms at the input and 1mV at the output. Always use the full bandwidth of the circuit for noise calculations, because noise frequencies higher than the maximum signal frequency can alias into the lower frequencies and affect the final value.

You'll see that, because error terms sum in an rms fashion, gain error is the dominant source of error. The OP-42 and OP-44 amplifiers minimize, but do not eliminate, these errors. Consequently, you'll find that the output of the autozeroing amplifier is accurate to within 0.5% at 50kHz, and to within 0.02% at frequencies below 10kHz, with the addition of a 7mV noise contribution and 2.5mV of offset error.

These gain-stage errors are passed on to the S/H amplifier, which has its own sources of error, arising from aperture time and aperture jitter, hold steps, droop, and finite CMR (think of the entire circuit of Figure 2 as the S/H stage). However, because the amplifiers of the S/H stage operate at unity gain, they eliminate gain error that's caused by bandwidth limitations or high closed-loop gain,

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CALCULATING ERROR MAGNITUDES *Continued*

and they greatly reduce the other errors associated with the multiplexed stage.

You can simplify matters by eliminating the input amplifier (IC_1) and driving the S/H buffer (IC_2) directly from the output of the multiplexed stage. Then the primary source of error affecting the output will consist of the hold step (1mV) and acquisition error (0.01%). Errors arising from aperture uncertainty and aperture jitter will be minor and will add no more than 0.01%.

The CMR error can be more significant, depending on the frequency. It's difficult to estimate what frequency to use for calculating errors in the S/H stage; some designers use the dc specifications, on the assumption that the amplifier operates in dc mode after the hold settling time. This assumption would be true for long hold times, but in fact the S/H stage not only reproduces the primary waveform but also adds high-frequency components to form steps. For this reason you should always use actual operating frequencies in your error calculations. Consequently, at 50kHz, the 70dB CMR of the OP-42 amplifier can contribute 0.03% error. The error terms again sum in rms fashion to yield a total of slightly less than 0.04% error from the S/H stage. Noise is negligible in comparison with that delivered by the gain stage, and the dc offset is simply that of the OP-42, an additional 0.75mV.

IMPROVING PERFORMANCE

The total system error for both the gain stage and the S/H stage consequently becomes approximately 0.05% at frequencies less than 10kHz and increases to 0.5% at 50kHz. This is in addition to the 7mV noise contribution and 2.25mV dc offset. You could eliminate gain-stage errors by cascading two amplifiers, each with a gain of 10, instead of using a single amplifier with a gain of 100. The error terms contributed by the S/H stage would dominate in such a configuration.

You can calibrate and eliminate many of the error terms discussed above. For example, in a system that uses a fast Fourier transform to examine the spectral content of a waveform, you could apply a correction factor to correct for gain roll-off at high frequencies. You could also correct for CMR errors by applying an additional correction factor based upon the signal level. DC offsets are simply eliminated by subtracting a constant term from the signal. Noise can be eliminated only by averaging many repetitive signals.