CCD Imaging Systems

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CCD Imaging System
Typical Block Diagram

V/H - Driver — Timing Generator

Preamp and Clamp — Correlated Double Sampling (CDS) — Gain and Driver — A/D — DSP

DC-Restore

CCD

Coarse Offset Level Shift

D/A

Fine Offset
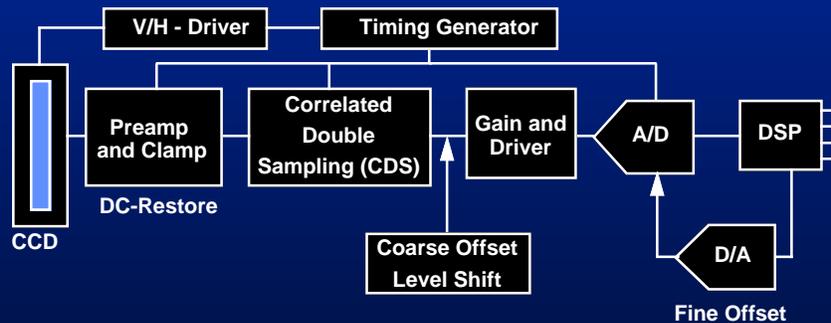
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Technology advances with CCDs (Charge Coupled Device), like increased resolution at lower manufacturing costs, have fueled the growth in the electronic imaging industry. However, some of the typical constraints of CCDs remain unchanged, such as the very low output signal level and the inherent noise sources. Furthermore, increased resolution generally equals higher read-out speed, which in turn dictates the requirements for the subsequent electronics.

The CCD is the central element in an imaging system. Designers need to be aware of the special requirements for the signal conditioning of the CCD in order to achieve the maximum performance. The output signal of the CCD is a constant stream of the individual pixel "charges" and this results in the typical form of stepped DC voltage levels. This output signal also contains a DC-bias voltage, which is in the order of several volts. The signal is then passed through a capacitor to block the DC voltage before going into the preamplifier. To maintain the necessary relationship between the pixel information and the baseline, a clamp or DC-restore circuit is usually situated in the first processing stage. The next stage is used as a noise reduction circuit specific to CCD based systems: the correlated double sampler (CDS). Following is another gain stage, which could be a automatic gain control amplifier (AGC), or a fixed gain stage with offset adjustment. Before going into the A/D converter it usually passes through a dedicated buffer or driver circuit optimized for the selected converter type. Further baseline stabilization can be achieved by having a D/A converter in a digital control loop. In the following discussion the CCD itself is looked at and design techniques are explored.

Basic CCD Theory
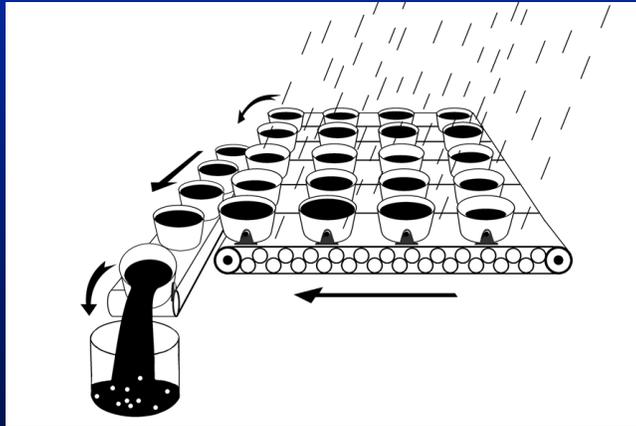
- Raindrops = Photons
- Buckets = Pixel
- Conveyor Belts = CCD Shift Register
- Metering Glass = Sense Capacitor

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In its principle, the operation of a CCD array is quiet simple. A common analogy[1] is shown here, using an array of buckets on conveyor belts. During a rain shower the raindrops will fill the lined up buckets more or less. Then the conveyor belts transport the buckets to the front belt and dump their content into another row of buckets. As they move forward the rainwater is spilled into the metering glass. The scale on the metering glass indicates how much water was collected in the individual bucket. When relating this model to a real CCD element, the "raindrops" are the light (photons) falling onto the CCD surface, the buckets are the many pixels of a CCD array and the "conveyor belts" are the shift registers that transport the pixel charge to the output stage. This output stage is mainly the sense capacitor, here the "metering glass", and an output source follower is used to buffer this sense capacitor.

Basic CCD Theory

The CCD Array Configuration
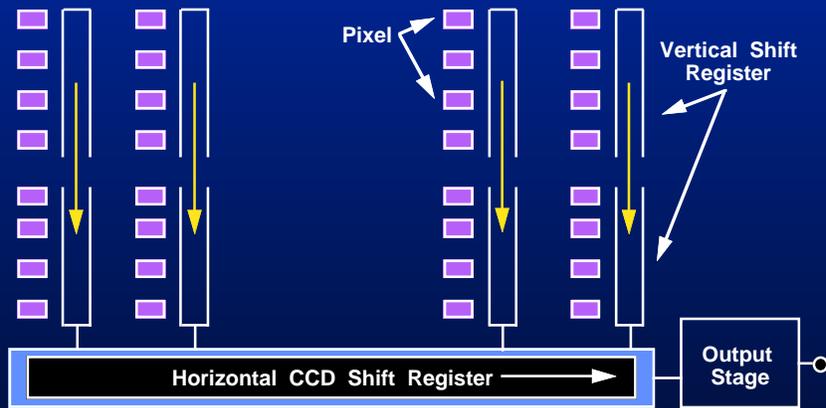
The CCD array is configured into multiple vertical shift registers and usually one horizontal shift register, both requiring different clock patterns. The flow is as follows: the pixel converts the light (incoming photons) into electrons which are stored as electrical charge. Then the charge is transferred down the vertical register in a conveyor-belt fashion to the horizontal shift register. This register collects one line at a time and transports the pixel charges in a serial manner to the on-chip output stage. The on-chip output converts the charge into a voltage. This voltage is then available at the output in the typical CCD pulse form.

With the standard CCD, most of the pixels can detect the light. The CCD also has small sections at the beginning and at the end of each vertical segment that are covered and therefore "optically black". Those pixels will always have the voltage level representing black. Some image circuits use those as reference pixels to adjust the signal offset.
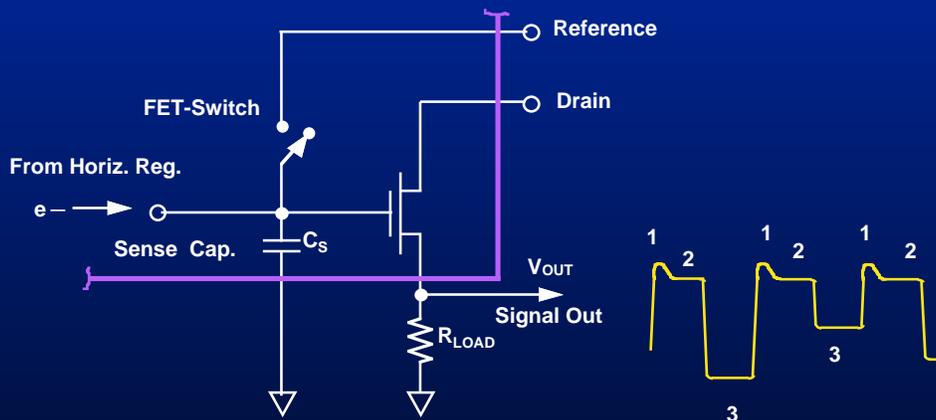
Some numbers:

The horizontal read-out speed for systems with up to 12-bit resolution is up to 10MHz. For higher resolutions ($\leq$16-bit) the clock speed is around 1MHz.

Typical pixel dimensions are: ~27μm^2 for a 512x512 array or ~12μm^2 for a 1024x1024 array.

Basic CCD Theory
Built-In CCD Output Stage — Charge Detection

Shown here is the conceptual schematic of the output stage inside the CCD element. This stage is responsible for the so called 'charge detection'. As discussed earlier, the charge e^- generated is moved into the horizontal shift register. The charge of each individual pixel is controlled by the horizontal clock and stored onto the Sense Capacitor (C_S). A typical value for such a capacitor is 0.1pF to 0.5pF. According to $V = Q/C$, the charge will develop a voltage across capacitor C_S, representing the light intensity for the particular pixel. A MOSFET transistor configured as a source follower buffers the capacitor from the output node, which connects to the load resistor, R_{LOAD}. At this point, the image (video) signal becomes available at V_{OUT} for further signal processing.

As indicated in the figure above, the output voltage is a series of stepped DC voltages. One pixel period is composed of three different levels: (1) the "reset feedthrough", (2) the "reference level", (3) and the "pixel level".

A readout sequence begins with the reset. Where the FET-switch is closed, set the sense capacitor to the initial reference voltage. The reference voltage can be relatively high, up to +12V. The closing of the switch causes the reset feedthrough, a result of capacitive coupling through the MOSFET. After the decay of this feedthrough the capacitor will reflect the reference voltage level (2). Once the capacitor has been reset, the switch opens and pixel charge is transferred to the capacitor, altering its voltage.

An important specification for CCD elements is the sensitivity. This is a measure of the achievable output voltage per electron, $S_V = V_{OUT}/e^-$. With a 0.1pF capacitor, the output voltage would be -1.6µV per electron. Unfortunately, the source follower has a gain of less than 1 (~0.8).

System Performance Limitations

➡ **The Main Limiting Factor:** *NOISE*

Noise Sources:
- CCD — output stage kT/C-noise
- Semiconductor Noise — Shot, Flicker, White Noise
- Resistor / Thermal Noise
- ADC Quantization Noise
- Line Frequency, 50/60Hz

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The lower limit of the dynamic range in an image system is set by the noise floor. Different techniques are available to maximize the dynamic range and optimize for the input range of the A/D converter, but a thorough understanding about the noise sources is crucial. The main noise source, besides digital feedthrough, is the so called kT/C-noise of the FET reset switch caused by its channel resistance.

The MOSFET also contributes noise — the flicker (1/f) noise and some white (thermal) noise. Additionally, each resistor is a source of thermal/white noise.

Another limit is set by the quantization noise of the A/D converter. The rms quantization noise is expressed by the equation $q/\sqrt{12}$, with q being the bit size or LSB weight of the converter. For example, a 10-bit converter with a full-scale input range of 2V has a bit size of 2.0V/1024 = 1.953mV. Hence, the quantization noise is 564µVrms. Assuming a 0.1pF sense capacitor the detection limit would be at about 350 electrons due to the quantization noise.

One obvious way to reduce this limitation is to use an A/D converter with a higher resolution, e.g., 12 bits.

Another example for a noise source would be the line frequency with 50Hz or 60Hz.

On-chip Output Stage Noise
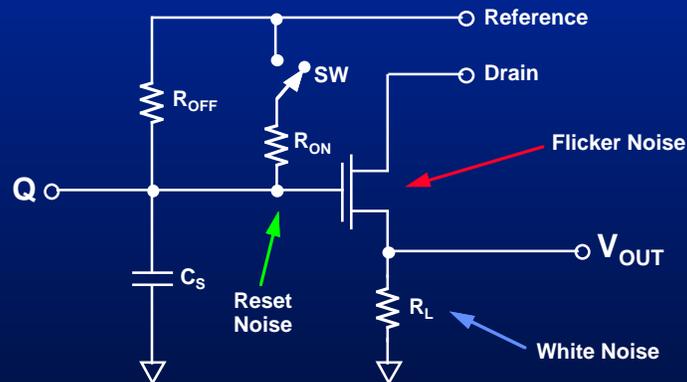
Looking again at the built-in output stage of the CCD, we can identify the different noise sources previously discussed.

- RESET NOISE: The thermal noise of the channel resistance (R_{ON}) of the FET switch (SW). This noise is often termed as kT/C-noise. With a typical value of 100 to 300 electrons (rms), this is the dominant limitation for the detection of small signals.

- FLICKER NOISE: Also 1/f-noise. Originates in the MOSFET, and relates to the presence of traps associated with contamination and crystal defects in the semiconductor. Its magnitude is therefore process dependent.

- WHITE NOISE also known as resistor noise: It is temperature dependent and equal to $\sqrt{(4kTRB)}$. White Noise has several origins. For example, the noise of the load resistor (R_L).

A closer look at the RESET NOISE

Reset Noise (kT/C) + White Noise

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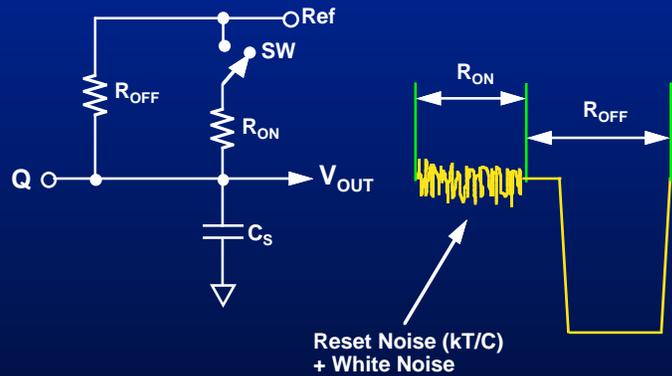
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The main components of reset-noise come from the sense capacitor C_S and the switch (SW), represented by its On-resistance, R_{ON}. Capacitors are usually thought of as noise-free devices. In the case of sampling systems, however, they exhibit a theoretical noise because the capacitor is periodically reset. The finite resistance of the reset switch has an associated thermal noise. This noise is transferred to the capacitor when the reset switch opens. As the resistor, R_{ON}, is made smaller, its noise will decrease, but the RC bandwidth will increase at the same time. The noise can be calculated as follows:

The thermal noise of a resistor is given by: $e_n = \sqrt{4kTRB}$ (Vrms).
Where:

k = Boltzmann's constant = 1.38054 E -23
T = absolute temperature in Kelvin, (298°K = +25°C)
R = on resistance of switch in Ω
B = Noise Bandwidth in Hz

Since the CCD model has a single-pole response, B is the -3dB bandwidth times $\pi/2$, which will be called NBW indicating the noise bandwidth for a single pole response. Therefore:

$NBW = 1/(2\pi R C) \cdot \pi/2 = 1/(4RC)$

$\Longrightarrow e_n = \sqrt{(4kTR)/(4RC)} = \sqrt{(kT/C)}$

Using an example relevant to CCDs: $C_S = 0.1pF$, $R_{ON} = 2k\Omega$

The Noise Bandwidth would be: NBW = 1.25GHz

The Reset Noise would be: $e_{nr} = 0.203mVrms$

Taking the lowest detectable charge, one electron (e— = 1.6 E-19A-sec), the reset noise relates to 126e— of charge. With a maximum video signal amplitude of about 0.3V (187500e—), the signal-to-noise ratio would be 1500 or 63dB. The dynamic range is about 11.5 bits.
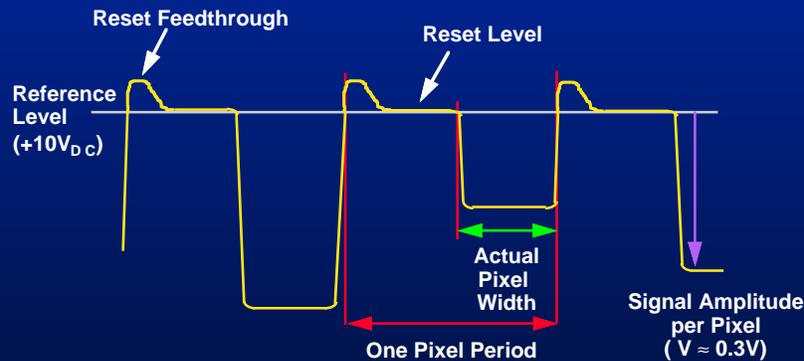
White noise or thermal noise is present in any resistor or conductor. The rms-voltage noise is proportional to the square root of the temperature, T, the bandwidth, B, and the resistance, R, as given by the equation $e_{nw} = \sqrt{4kTRB}$.

The typical output resistance of a CCD, which includes the external load resistor, is in the range of 200Ω to $20k\Omega$. The output impedance of the CCD output stage (R_O) is formed by the load resistor (R_L) and the channel resistance of the output MOSFET.

The CCD Output Signal

Reset Feedthrough

Reset Level

Reference
Level
(+10V$_{DC}$)

Actual
Pixel
Width

Signal Amplitude
per Pixel
(V ≈ 0.3V)

One Pixel Period

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This is a typical output voltage waveform from a CCD element. The signal can be described by five characteristics: the Reset Feedthrough, the Reset Level, the Signal Amplitude, the Pixel Period and the actual Pixel Width.

As mentioned before, this CCD signal is not a continuous sinusoidal waveform, but rather is a sequence of stepped DC levels.

The sequence for one pixel is as follows:

• Reset Feedthrough: This can be a relatively large pulse, as a result of capacitive coupling through the FET.

• Reset Level: The "Sense Capacitor" will be charged to this final reset voltage. This level can be in the order of +10V or more, creating the requirement for a DC-decoupling capacitor at the output of the CCD element.

• Pixel Level: After the reset period, the pixel is transferred. The amplitude corresponds to the charge representing the incident light level of the addressed pixel. Because of the electron charge (e−) the CCD output signal is inherently unipolar (negative).

Typical CCD pixel rates can vary between 1Mpixel/sec up to 20Mpixel/sec, depending on the application.

First Stage - The Preamplifier

CCD

Drain

DC - Block

C_B
$0.1\mu F$

OPA655

V_{OUT}

A_1

R_L

SW

R_2
50Ω

R_1
200Ω

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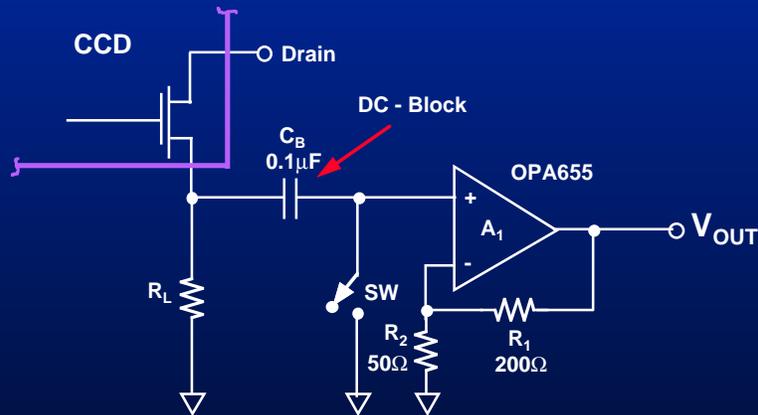
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The CCD output signal is immediately gained up by the preamplifier, as shown in this circuit schematic. The amplifier itself uses the wideband FET input op amp OPA655, set in a gain of +5V/V. With a -3dB bandwidth of 400MHz for a gain of +1, the bandwidth of the OPA655, in a gain of +5V/V, is 75MHz. The specified 12-bit settling time for this part is about 16ns. To estimate the total response time, the slewing time for the 1Vp-p output needs to be added to the 16ns settling time. With a slewing time of 3.3ns, this adds up to a total of about 20ns. Considering a system with a 5MHz readout frequency, one pixel period takes 200ns. The actual pixel width will be approximately half of that time, or 100ns. The OPA655 will take only 1/5 of the pixel time and still be accurate to 12 bits. The fast response of the OPA655 leaves sufficient time for the subsequent stages and for the acquisition time of the A/D converter.

As discussed previously, the pixel information rides on the reference voltage, which can be +10V or more. This could cause unwanted common-mode effects or even saturation. The series capacitor, C_B, blocks this DC component from the video signal and the reference of the baseline is lost. A new baseline can be established with the switch, SW, to ground. For each reset period the switch closes and grounds one side of the capacitor, setting its charge to a defined potential, ground or 0V, in this case.

The Preamplifier

Op Amp Selection Criteria

- Gain Bandwidth Product
- Slew Rate
- Settling Time
- Low Noise
- Overload Recovery

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Because of the nature of the CCD output voltage, the performance requirements for the processing components, like the preamplifier, focus on the time domain specifications of the ICs.

For the operational amplifier specifications like slew-rate, settling time and overload, recovery time is important. Of course, the components should have low noise specifications and not add too much noise to the CCD signal, reducing the dynamic range.

When designing a CCD imaging system, time domain parameters of the ICs are the specifications that the designer will look at. A designer may not always be able to find all of them in the product data sheets and a good first-order approximation of the missing specification can be obtained using the relationships between the frequency and time domain shown above. For example, the rise time may be calculated by using the simple relationship between the -3dB bandwidth and the rise time of a first-order system: Risetime = 0.35/Bandwidth.

This rise time may then be used to obtain the system's time constant, which will lead to the settling time: Time Constant = Risetime/2.2.

Another familiar relationship for a single pole system is its pulse response: $V_{OUT}(t) = V_{IN}(1 - e^{-t/\tau})$. Here, τ is the time constant formed by RC. Solving this equation for t results in $t = -\tau \times \ln(\%/100)$. This provides the settling time for any desired settling accuracy, usually used as a % term.

Again, keep in mind that all these design equations are based on a single-pole response. The actual values may differ due to second-order effects of the ICs.

High Speed FET Op Amps

	BANDWIDTH	SLEW RATE	SETTLING TIME	NOISE
OPA655	400MHz	290V/μs	17ns	6nV/$\sqrt{Hz}$
OPA637	80MHZ	135V/μs	450ns	4nV/$\sqrt{Hz}$
OPA671	35MHz	107V/μs	240ns	9nV/$\sqrt{Hz}$
OPA627	16MHz	55V/μs	550ns	4nV/$\sqrt{Hz}$

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This table provides a selection of high speed op amps that feature a FET input. The advantage over bipolar input stages is the very low bias current. The bias current becomes important in applications where a capacitor is connected to the input, or where the source impedance is high. The typical input bias current of all three listed op amps is 5pA or better. Input bias currents on high speed bipolar op amps are in the range of 1 to 30μA. All of the listed op amps operate on ±5V supplies, except for the OPA671, which requires ±15V supplies. The OPA637 is a decompensated version of the OPA627 and therefore only stable in gains of 5 or higher. The decision whether to use a FET input or bipolar input device will always depend on the requirements of the individual application.

Preamplifier with DC - Restore
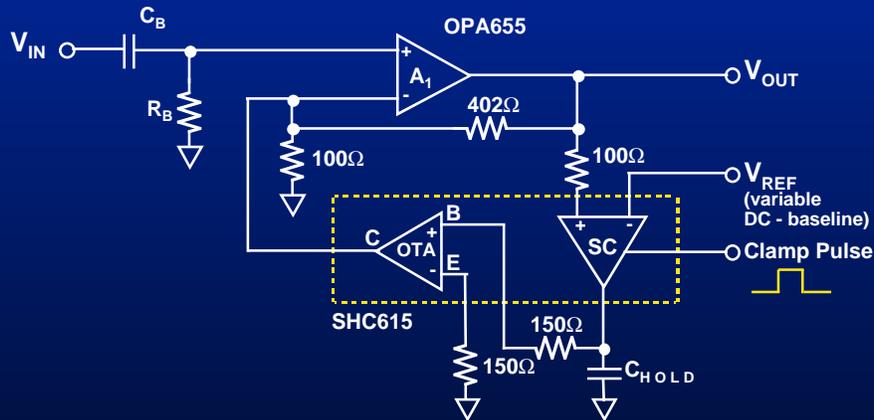
Another circuit example for the preamplifier and the clamp circuit is shown here. The preamplifier uses the wideband, low noise OPA655, again configured in a gain of +5V/V. Here, the OPA655 has a typical bandwidth of 57MHz with a 12-bit settling time of about 30ns (0.01%).

The video signal passes through the capacitor C_B, blocking the DC component. To restore the DC level to the desired baseline, the DC-restoration IC SHC615 is used. The SHC615 basically incorporates two OTAs, or voltage controlled current sources. One of the OTAs can be digitally controlled and resembles a switched difference amplifier. The inverting input is connected to a reference voltage. During the high time of the clamp pulse the switching comparator (SC) will compare the output of the op amp to the reference level. Any voltage difference between those pins will result in an output current that either charges or discharges the hold capacitor, C_{HOLD}. This charge creates a voltage across the capacitor, which is buffered by the OTA. Multiplied by the transconductance the voltage will cause a current flow in the collector, C, terminal of the OTA. This current will level shift the OPA655 up to the point where its output voltage is equal to the reference voltage. This also closes the control loop. Because of the buffer, the voltage across C_{HOLD} stays constant and maintains the baseline correction during the off - time of the clamp pulse.

The external capacitor (C_{HOLD}) allows for a wide range of flexibility. By choosing small values, the circuit can be optimized for a short clamping period or with higher values for a low droop rate. Another advantage of this circuit is that small clamp peaks at the output of the switching comparator are integrated and do not cause problems in the signal path.

DC-Restore Circuit with SHC615
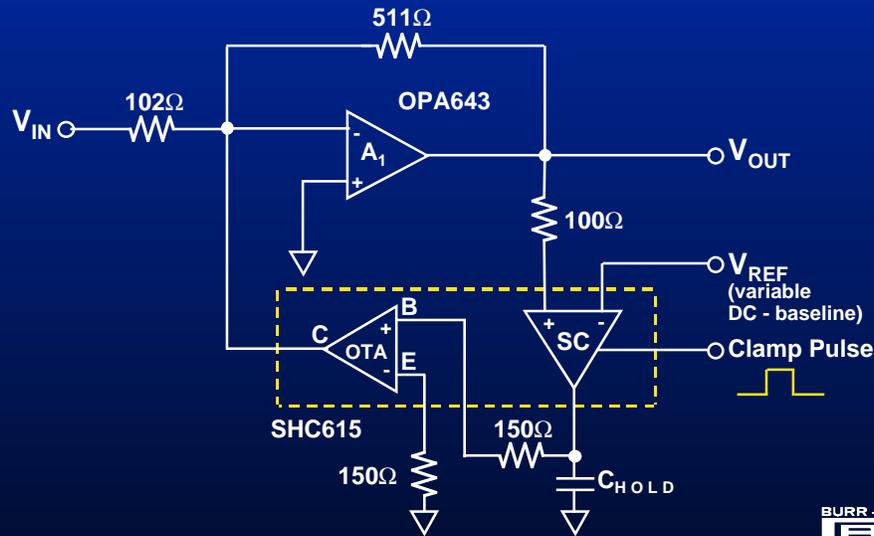
This circuit shows a slight alteration of the previous restoration circuit. Here, the FET op amp, OPA655, is replaced with the wideband, low noise amplifier, OPA643. The OPA643 is configured in an inverting gain of 5V/V. The typical bandwidth of the OPA643 is 250MHz, making the op amp ideal for CCD systems with high pixel rates. The common mode voltage problem encountered in the previous circuit is avoided with this configuration by selecting the inverting topology for the signal processing op amp. Depending on the individual application, the resistor values may need to be changed in order not to load the previous stage.

## The DC - Restoration Circuit SHC615

Features:

Bandwidth	**280MHz**
Hold Command Delay	**3.8ns**
Propagation Delay	**2.2ns**
OTA, Input I$_{BIAS}$	**0.3μA**
SC, Hold Output I$_{BIAS}$	**10pA**
Feedthrough Rejection	**-100dB**

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The SHC615 is a complete monolithic IC for very fast and precise DC-restoration, offset clamping, and low frequency hum suppression. This function can be realized with just the SHC615 alone or having the SHC615 alongside a video op amp for out-of-path restoration. The application list for the SHC615 also includes high speed sample and holds, high speed integrators, or peak detectors for fast pulses. The functions inside the SHC615 are a sampling comparator (SC) and an operational transconductance amplifier (OTA) for buffering the external hold capacitor. The transconductance of the OTA and the sampling comparator can be adjusted by an external resistor, allowing bandwidth, quiescent current, and gain tradeoffs to be optimized.

Simplified CCD Output Signal

S_1

ΔV

kT/C - Noise p-p

Reset Level

**Video Level**

S_2
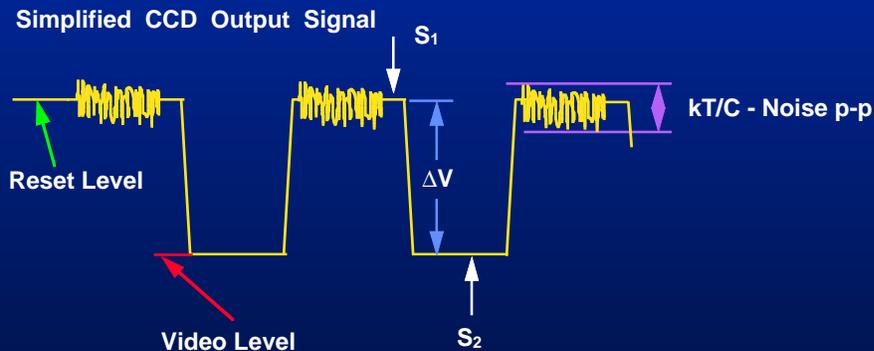
Note: Signals are out of scale

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As shown before, the noise is the limiting factor for the resolution in a CCD system, where the kT/C noise is dominant. To reduce this noise, imaging systems use a circuit called a "Correlated Double Sampler" (CDS). The name comes from the double sampling technique of the CCD charge signal. The first sample (S_1) is taken at the end of the reset period. When the reset switch opens again, the effective noise bandwidth changes because of the large difference in the switch's R_{ON} and R_{OFF} resistance. This causes the dominating kT/C noise essentially to "freeze" in its last point.

The other sample (S_2) is taken during the video portion of the signal. Ideally, the two samples differ only by a voltage corresponding to the transferred charge signal. This is the video level minus the noise (ΔV).

The CDS function will eliminate the kT/C noise as well as much of the 1/f and white noise.
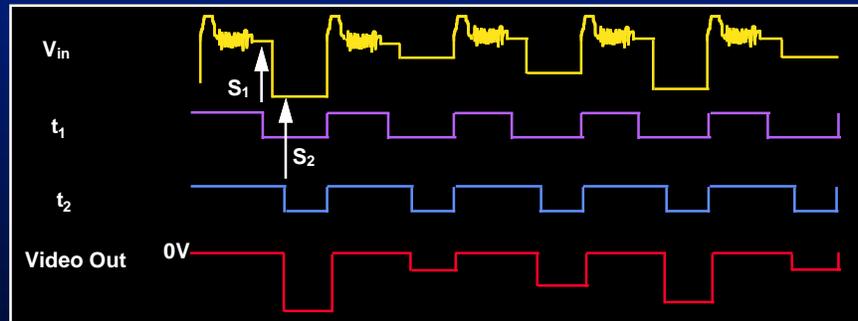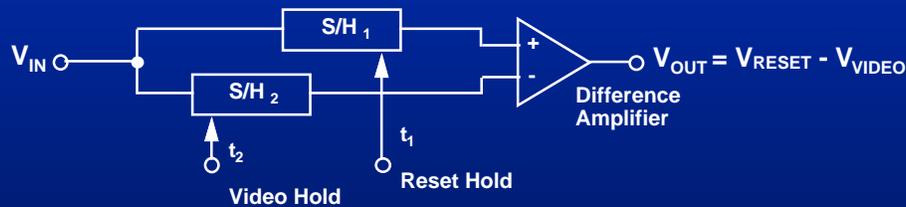
Here is a block diagram of a CDS circuit. Two sample and hold amplifiers and one difference amplifier constitute the correlated double sampler.

The signal coming from the CCD is applied to the two sample and hold, with their outputs connected to the difference amplifier. The timing diagram will clarify the operation. At time t_1, the sample & hold (S/H$_1$) goes into the hold mode, taking a sample of the reset level including the noise. This voltage (V_{RESET}) is applied to the non-inverting input of the difference amplifier. At time t_2, the sample and hold (S/H$_2$) will take a sample of the video level, which is V_{RESET} -V_{VIDEO} . The output voltage of the difference amplifier is defined by the equation $V_{OUT} = V_{IN+} - V_{IN-}$. The sample of the reset voltage contains the kT/C noise, which is eliminated by the subtraction of the difference amplifier.

The double sampling technique also reduces the white noise. The white noise is part of the reset voltage (V_{RESET}) as well as of the video amplitude (V_{RESET} - V_{VIDEO}). With the assumption that the noise of the second sample was unchanged from the instant of the first sample, the noise amplitudes are the same and are correlated in time. Therefore, the noise can be reduced by the CDS function.

CDS Circuit with S/H, Example #1
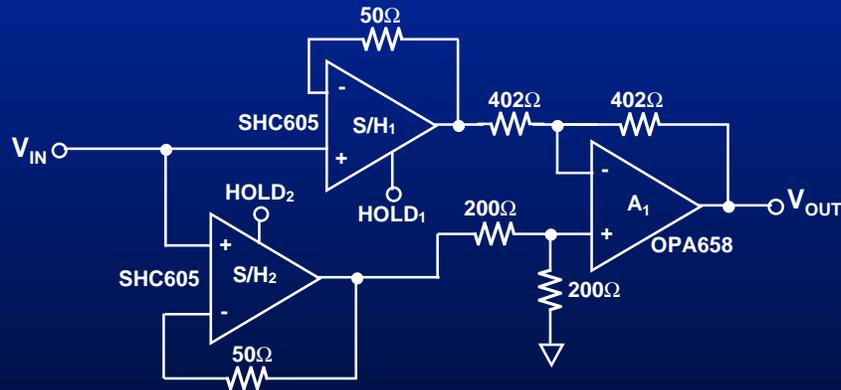
This is a circuit implementation of a correlated double sampler, CDS. It uses two SHC605 sample and hold ICs and the current-feedback op amp OPA658. The SHC605 has a differential input and can be connected in inverting or non-inverting configurations. In this design both sample and holds are connected as unity gain buffers, with a 50Ω resistor in the feedback. S/H$_1$ will capture a sample from the reset level. The other sample and hold, S/H$_2$, takes the sample of the video signal. The held output signals drive the positive and negative inputs of the difference amplifier, A$_1$. Its function is described by the equation $V_{OUT} = V_{IN+} - V_{IN-}$. As previously shown, the result will be the charge signal reduced by the noise component.

To match the output load of the two sample and holds, S/H$_2$ drives into two 200Ω resistors. This matches the load S/H$_1$ sees driving the one 402Ω resistor to the inverting input of the amplifier A$_1$.

For more details on the difference amplifier employing a current feedback amplifier and optimizing it, see section 6 (High Speed Amplifiers).

CDS Circuit with S/H, Example #2
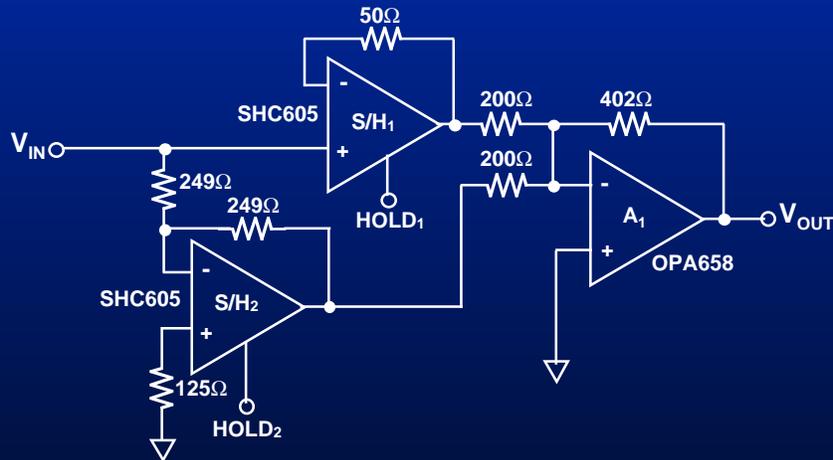
This circuit shows a slight modification from the previous one. It also uses two sample and hold circuits (SHC605) to take the two samples needed for the correlated double sampling function. Again, sample and hold amplifier S/H_1 is set in a unity gain configuration. To implement the subtract function now, sample and hold amplifier S/H_2 is used for the signal inversion. This is done by configuring it in a gain of -1V/V. The difference amplifier can now be replaced by a simple summing amplifier, A_1. A current feedback amplifier, like the OPA658, is the preferred choice for this function because of its wide bandwidth and the independence of the bandwidth to the input resistors.
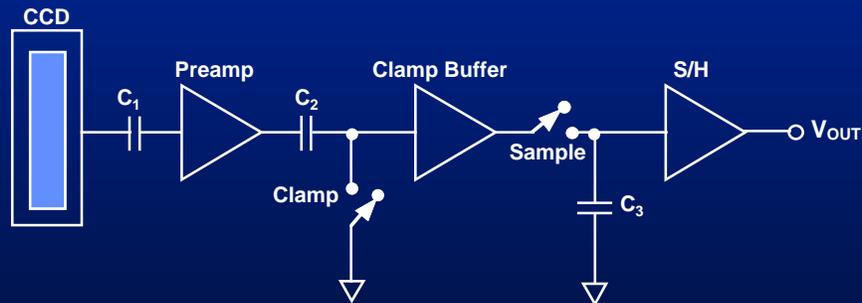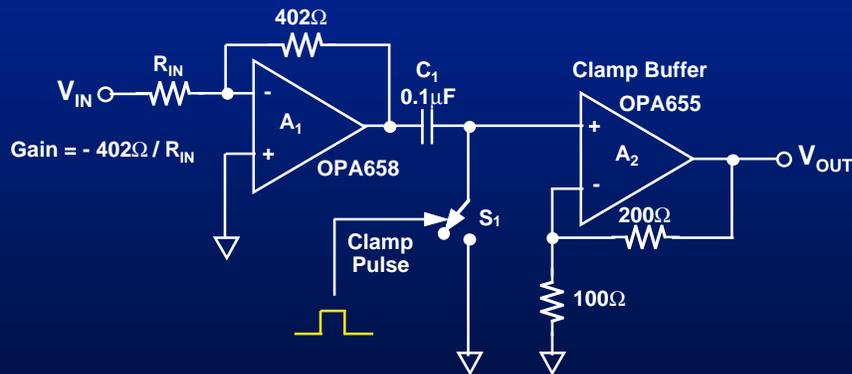
Another implementation of correlated double sampling is the "clamp and sample" technique as shown in this circuit. Capacitor C_1 blocks the high DC level from the first amplifier stage leaving only the signal amplitude. As already discussed, the preamplifier will gain up this signal. The capacitor C_2 and the clamp switch are the main elements within the CDS function. During the reset period of the CCD, the clamp switch is closed, grounding one side of the capacitor. At that time, the noise will charge the capacitor. In the next phase the clamp switch opens and the signal charge is processed through the amplifiers. By passing through C_2 the signal level gets subtracted by the amount of charge previously stored, thus eliminating the noise. The "noise free" signal level gets sampled in the subsequent sample and hold stage. This stage could be implemented by a monolithic S/H IC, like the SHC605.

CDS Clamp Circuit

402Ω

R_{IN}

V_{IN}

-

+

A_1

Gain = - 402Ω / R_{IN}

OPA658

C_1
$0.1\mu F$

Clamp
Pulse

S_1

Clamp Buffer

OPA655

+

A_2

-

200Ω

100Ω

V_{OUT}

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To further improve the signal-to-noise ratio, the first amplifier, A_1, gains the input signal by G = -$402\Omega/R_{IN}$. This also gains the noise, but it will be removed from the signal with the CDS function. During the CCD reset period the clamp pulse is applied to switch S_1, grounding the capacitor C_1. The voltage on the ungrounded side of this clamp capacitor remains stationary, leaving the noise sample stored on the capacitor. The CCD reset period ends and switch S_1 opens. Now the pixel information, which is also contaminated with the noise, is transferred. Gained up by amplifier A_1 the signal passes through the clamp capacitor. Here a subtraction takes place, eliminating the noise component from the signal. Again, this is because the capacitor carries a charge (voltage) representing a sample of the rms-noise. As the signal passes the capacitor C_1, it is reduced by the noise sample stored on the capacitor. This effectively eliminates the noise. The "on" and "off" state of the switch implements the correlated double sampling.

The clamp buffer insures a decoupling of the sensitive node. The wideband FET op amp OPA655 is used here, since the FET input assures a very low bias current (10pA, typ). Bias current causes droop on the clamp capacitor, which could create a significant error depending on the timing.

The output of amplifier A_2 would be sampled by a sample and hold IC.

The drawback of this circuit is that the used electronic switches can introduce kT/C-noise again. A standard CD4066 switch could be used for slow speed systems, whereas switches like the DG611 from Siliconix could be employed for high speed systems.
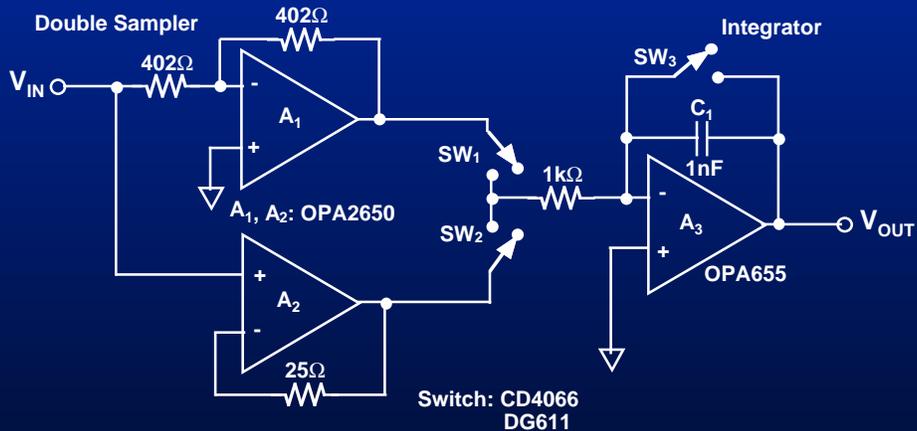
CDS with "Dual Slope Integrator"

1 - Integrate (-)
2 - Integrate (+)
3 - Hold
4 - Reset

7 .24
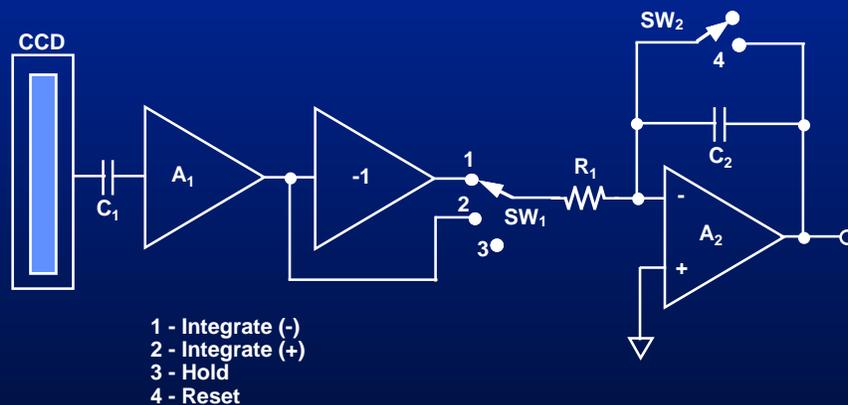
Another example of a CDS circuit is known as the dual slope integrator, named after the method used for its implementation. A basic design schematic is shown here. The principle function is as follows:

• During the reset time the first sample is taken with the switch (SW_1) in position 1. The sample is inverted before stored on the capacitor of the integrator.

• The second sample is taken shortly after the signal charge is transferred from the CCD output. Now the inverting stage is bypassed and the integrator sees the signal without the sign inversion.

• The switch goes into position 3, which is the HOLD position. Because of the sign inversion of the first sample, this charge will be subtracted from the signal charge of the second sample. Because of its correlation, the portion of the signal that gets eliminated is the noise. The signal sample is now available for further processing.

• Before the above procedure is repeated, the charge on the integration capacitor is zeroed by closing the reset switch (SW_2) across it.

• This CDS method is often used in low-light detecting systems. The integration time can range from ms up to several hours. The integrator CDS is found in applications for Astronomy, Spectroscopy, Microscopy, and Photometry. Those applications demand a wide range and high resolution.

CDS with Dual Slope Integrator Circuit Example

Another way of implementing the CDS function is by using a dual slope integrator. The simplified circuit shown here realizes this function. The requirement for an integrating CDS is that the video signal needs to be preconditioned in a way that it is available as a straight signal ($0°$ phase) and as an inverted signal ($180°$ phase). Here, amplifier A_1 and A_2 respectively, perform this function. A dual op amp, like the OPA2650, is well suited for this, since both amplifiers are closely matched in bandwidth and phase characteristics. During the CCD reset phase switch SW_1 closes, allowing the integrator A_3 to store the noise sample (kT/C-noise) for a finite time period.

In the next phase switch SW_1 opens and switch SW_2 closes, transferring the pixel information, which also includes the noise, to the integrator. Because this signal is now inverted, the common signal contents, which is the noise, will cancel out leaving only the video signal.

Note that a 25Ω feedback resistor, rather than a direct short, is used for the unity gain follower, A_2. This effectively reduces the Q of what would otherwise be a parasitic inductance (the feedback wire) into the parasitic capacitance at the inverting input.

Depending on the application and the desired speed, the current feedback equivalent to the OPA2650 can be used, which is the OPA2658.

The integrator circuit uses the FET input wideband amplifier OPA655.

The last two analog processing stages within this CCD image system are the A/D converter and its driving circuit. This circuit could also be used to make the last span or offset adjustments to the signal to accommodate for the maximum input range of the converter. Compared to their industrial counterparts, converters in the imaging arena usually have a much smaller input range, for example ± 1V. One reason for this is that a ± 10V input range would require the driving amplifier to slew ten times faster for a fixed time interval. On the other hand, the limited ± 1V input range sets tighter limits on the signal-to-noise ratio, and designers always strive to optimize the signal to the full scale range.

On the next few pages some general design ideas will be discussed.

Fast Switching Gain Amplifier
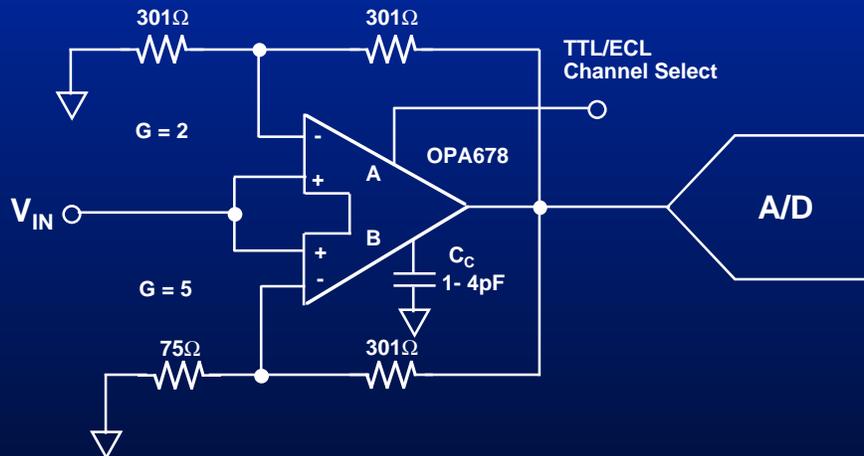
As the signal magnitude becomes smaller, the signal-to-noise ratio decreases. Small signals might need to be gained in order to keep SNR at the required level. Of course, many techniques of implementing gain are available. Besides the continuous level adjust performed by AGCs the signal can also be adjusted in discrete gain steps.

One circuit example that switches between two different fixed gains is given here. The main component in this circuit is the switched op amp, or SWOP AMP, OPA678. The OPA678 is a wideband (200MHz) op amp with two independent differential inputs. Either one of the inputs can be selected by the TTL or ECL logic channel select pin, which takes only 4ns. The settling time to 0.01% for a 1V step takes about 30ns. Therefore, the gain could be switched between channel A and channel B immediately after a weak signal has been detected. To optimize the frequency response, an external compensation capacitor, C_C, in the range of 1 to 4pF is used.

High Speed Op Amps

Implementing Level Shifting - Inverting Configuration

Left circuit equations:
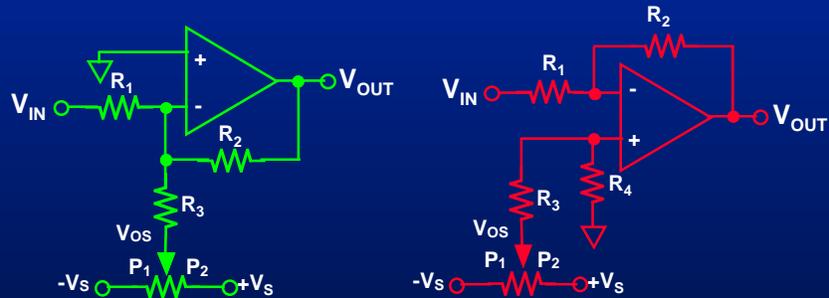
$$\text{Gain} = -\frac{R_2}{R_1} \pm \frac{R_2}{R_3} \bullet V_{OS}$$

$$\text{Noise Gain} = 1 + \frac{R_2}{R_1 \parallel (R_3 + P_1 \parallel P_2)}$$

Right circuit equations:

$$\text{Gain} = -\frac{R_2}{R_1} \pm \left(1 + \frac{R_2}{R_1}\right)\left(\frac{R_P}{R_P + R_3}\right) \bullet V_{OS}$$

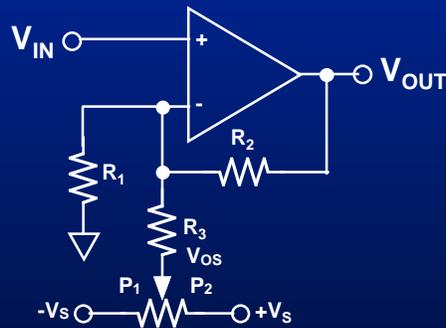$$\text{Noise Gain} = 1 + \frac{R_2}{R_1}$$

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The driver circuit for the A/D converter can be configured for the final gain offset adjustment. Because high speed op amps usually do not have offset adjust capabilities directly on the IC, designers are required to implement the appropriate level shifting externally.

Two inverting level shifting circuits are shown here. In the left figure, a current is injected into the summing junction through R_1. Even though it's a simple method it has the disadvantage of an increased noise gain due to R_3 and the potentiometer resistance. If R_3 can be made much greater than R_1 and R_2, the increase in noise gain can be limited.

The circuit on the right avoids this noise gain problem. Here, the offset voltage is added to the signal through the non-inverting input. However, another resistor, R_4, is needed. The current noise of the non-inverting input creates, together with R_4, another noise source besides R_4 itself. To reduce this noise R_4 could be bypassed with a small capacitor in parallel.

This circuit shows the level shifting scheme for the non-inverting op amp configuration. Similar to the first circuit, it adds a current to the summing junction. This works well for a small adjustment range, when R_3 could have a much higher value than R_1. Because the offset adjustment is in parallel to R_1 it affects the signal gain. For example, if R_3 plus the potentiometer resistance is 100 times higher than R_1, the gain will be altered by about 1%.

A common practice is to place the potentiometer between the two supply rails. The disadvantage of this can be easily seen; any variations in the power supplies will have an immediate effect to the signal.

The A/D Converter

	$f_{SAMPLING}$	DNL	Power
10-Bit			
- ADS820	**20MHz**	$\pm$ 0.2LSB	**195mW**
- ADS821	**40MHz**	$\pm$ 0.5LSB	**380mW**
12-Bit			
- ADS800	**40MHz**	$\pm$ 0.4LSB	**390mW**
- ADS801	**25MHz**	$\pm$ 0.3LSB	**270mW**
- ADS802	**10MHz**	$\pm$ 0.4LSB	**250mW**
14-Bit			
- ADC614	**5.12MHz**	$\pm$ 0.8LSB	**6.0W, Hybrid**
16-Bit			
- ADC701	**0.5MHz**	$\pm$ 0.4LSB	**2.8W, Hybrid**

7.30

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CCDs sensors come in a wide range of capabilities which make them well-suited for a variety of industrial and commercial applications. For example, CCDs are largely used in commercial products like video cameras, fax machines or document scanners. Here, the requirements are mainly focused on the price of using an A/D converter with 8- to 12-bit resolution. Suitable A/D converters for this market segment are the ADS8xx family, offering different speeds and resolutions. The ADS8xxs are monolithic ICs using the pipeline topology, allowing fast clock speeds. Built on a 0.6µm CMOS process they come in a small 28-pin SOIC package.

In the following "High Speed A/D Converter" section we will take a closer look into the pipeline technology and its driving circuitry.

Scientific or medical applications often need higher resolution. Using larger CCD arrays to gather more light they usually operate with longer integration times. This means that the throughput rate of the A/D converter does not need to be that high. In this segment, converters with more than 12 bits of resolution have their place. Converters like the ADC614 (14-bit) or the ADC701(16-bit) could be used here.