Digital Audio

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Digital audio means the digital information that represents the desired analog signals must be encoded as digital data. Although there are a number of ways to encode this analog information as digital data, Pulse Code Modulation has gained acceptance almost universally in the digital audio arena.

PCM is the modulation type most often employed because PCM is a purely digital modulation technique. The Delta Sigma ($\Delta\Sigma$) converter family owes much of its success in the industry because it is a "mostly" digital product. Hence, the PCM mode of encoding and the architecture used in this DAC family share many of the same benefits. Both allow analog information to be decoded or reproduced using digital techniques exclusively.

Why Digital?

1) The sound quality of the reproduction process depends only on the quality of the conversion process and is completely independent of the medium used to record the information. Anyone who has listened to an old LP that has been scratched and "dirtied" knows this not true of analog reproduction methods.

2) Digital reproduction represents a tremendous cost/price benefit for the consumer and manufacturer.

Digital circuitry is cheaper and can be fabricated in a much denser method.

Digital recordings take up much less physical space on a medium than analog recordings. Features such as muting and de-emphasis are much easier, i.e. less expensive using digital techniques.

Format and Description of CD Data

- **Two types of information encoded onto a CD-DA media**
  - **Main code area, the actual sound data**
  - **Sub-code area, optional information such as track number**

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The majority of products that are made and sold for the digital audio market are Digital to Audio Converters or audio DACs. The most common digital source of digital audio data that is presented to these DACs for analog reproduction is CD-DA or compact disc audio data.

While PCM encoded information is used to store this data on the compact disc the data, it is not necessary to be concerned about how to de-crypt digital information.

Once the PCM data has been decoded it is reproduced or changed into another form. The basic information that needs to be interfaced is the digital data, the clock data, and the separation of the data into the appropriate channels (Left and Right).

If the Delta Sigma topology was not used, these three sources of digital data would be all that was needed to reproduce the correct analog data. Delta Sigma DACs and digital filters require a signal in addition to the three just mentioned, namely an oversampling or system clock. This clock is **always** a multiple of the L/R or sampling signal. For purposes of this discussion the multiplier is either 256 or 384.

These four signals are always necessary for the $\Delta\Sigma$ DAC (PCM171X).

Basic Theory of Data Conversion

- **Four Basic Parameters Define a Data Converters Performance**
  - **Quantization Error $\geq$ Number of Bits**
  - **Dynamic Range $\geq$ Number of Bits and Type of Converter**
  - **Sampling Rate $\geq$ Type of Converter**
  - **Noise Floor $\geq$ Type of Converter and Application**

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While system performance may ultimately depend on a great number of device and system parameters, the performance of the data converter ultimately comes down to two criteria; the type of converter or topology and the number of bits used in the conversion process.

The number of bits determine the overall system accuracy and the level of quantization noise. This noise level will ultimately determine, how well the converter can ever perform.

The current segment topology is the basis for most of the theoretical work for data converters.

Delta Sigma devices can, in fact, exceed theoretical performance using techniques such as noise shaping and zero code detection.

- **R-2R—The oldest and still the "cleanest" conversion method**
- **Colinear—A monolithic of two R-2R devices**
- **Delta Sigma—(One bit) Trades resolution in amplitude for resolution in time. Requires a system clock that is faster than the bit data**

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Delta Sigma modulation is one of the newest and most talked about DAC topologies. The main reason is this topology's ability to be oversampled at a high rate, which reduces or eliminates the need for anti-aliasing filters. Some of the disadvantages to this conversion method are limited bandwidth and the inability to digitize discontinuous wave forms.

An R-2R converter, ladder topology, or current segment architecture is the foundation for both low- and high-end products. The topology requires both analog and digital sections. Also laser trimmed resistors are required.

A sign magnitude DAC is the topology used for what the audio profession considers to be the best DACs. This topology is, in essence, two R-2R DACs that are trimmed back-to-back. The advantage of this topology is in its low level performance. In a R-2R device, all of the bits go from 1 to 0. As the device is commanded to go through zero, only a few switches change per channel is a sign-magnitude device. When equal bit devices are compared, the Sign Magnitude DAC always has the best response in terms of THD+N.

R-2R or Current Segment Topology
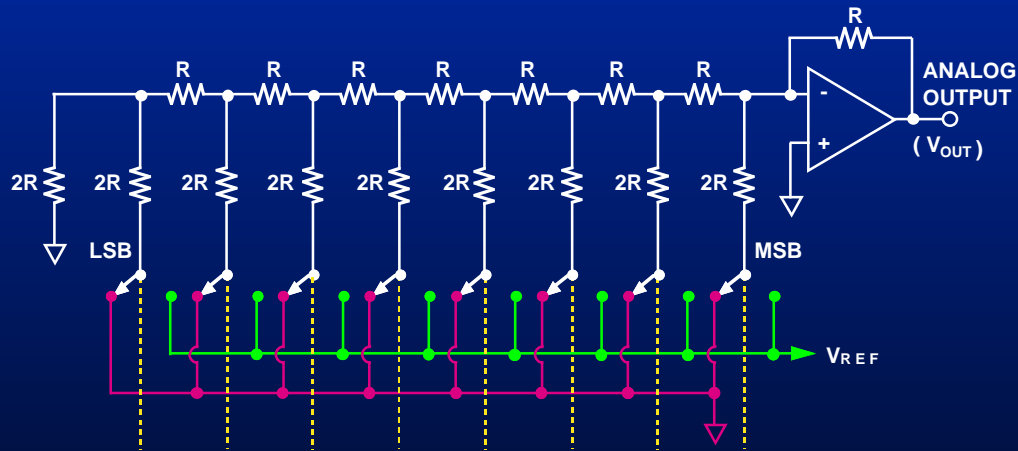
The multi-bit DAC is also referred to as R-2R ladder and current steering. For each new update, internal current sources are turned on or off, based on the digital input word. The above figure illustrates a basic R-2R architecture. Starting at the least significant current source, each has a value twice that of the previous source, with the exact value being set by a ratio of two resistors. The outputs of all the current sources which are "on" are summed to produce the correct analog output. This is a relatively simple architecture to manufacture, assuming the resistors for each current source can be properly adjusted to the necessary precision. These resistors are usually thin-film and laser-trimmed to the final value.

The classical R-2R topology has certain drawbacks, even when the resistors can be trimmed to a near-ideal value. Virtually all digital audio applications use a serial interface format. Internally, the multi-bit DAC uses a serial-to-parallel register before latching the data to the DAC. This format conversion, combined with process differences, results in data timing skews. These skews manifest themselves at the output as glitches. The glitch is most prevalent during the MSB transition, when bits are switching from 0111... to 1000... There is a brief moment in time when all bits are on or off. For example, the DAC switches might be briefly set to all ones (because the MSB switch is faster than the others). To some finite amount, this will occur for any given transition due to uncontrollable sizing errors in the devices and metal lines. If the time period is too long, then the output will begin to slew towards positive or minus full scale. If the time period is short enough, the output will not have time to change and the effect of the glitch will be inconsequential.

R-2R Family

|		PCM61	PCM63	PCM67/69	PCM1702	UNITS
Resolution		18	20	18	20	Bits
Dynamic Performance						
THD+N @ FS	typ	- 88	- 100	- 95	- 100	dB
Idle Channel SNR	typ	112	120	110	120	dB
D-Range	typ	108	108	106	110	dB
Ch Sepr	typ	N/A	N/A	106	N/A	dB
Output Amp		yes	no	no	no	
Output Range		± 3.0	± 2.0mA	± 1.2mA	± 1.2mA	Vpp
Number of Channels		1	1	2	1	1
Data Rate Specification						
Over Sampling Rate		8 x FS	16 x FS	16 x FS	16 x FS	
Input clock/data frequency	max	16.9	25	16.9	35	MHz
Settling Time, current step	typ	250	200	300	200	ns
Supply Voltage		± 5 to 15	± 5	+ 5	± 5	Volts
Power Dissipation	typ	175	225	225	150	mW
	max	475	300	300	250	mW
Package Type		16 PDIP	28 PDIP	16 PDIP 20 SOIC	16 PDIP 20 SOIC	

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This slide presents an overview of some of the R-2R products offered by Burr Brown. The R-2R products do offer some performance improvements over the delta sigma devices at the expense of price and features.

The PCM63 and PCM1702 are actually CoLinear devices. CoLinear devices are two DACs trimmed back to back to avoid the zero crossing glitch inherent in the R-2R topology.

The PCM67/69 devices are actually a hybrid topology of the R-2R and one-bit topologies. These devices are unique because they operate off a single 5V supply making them useful for portable designs.

PCM1710 ($\Delta\Sigma$) DAC System
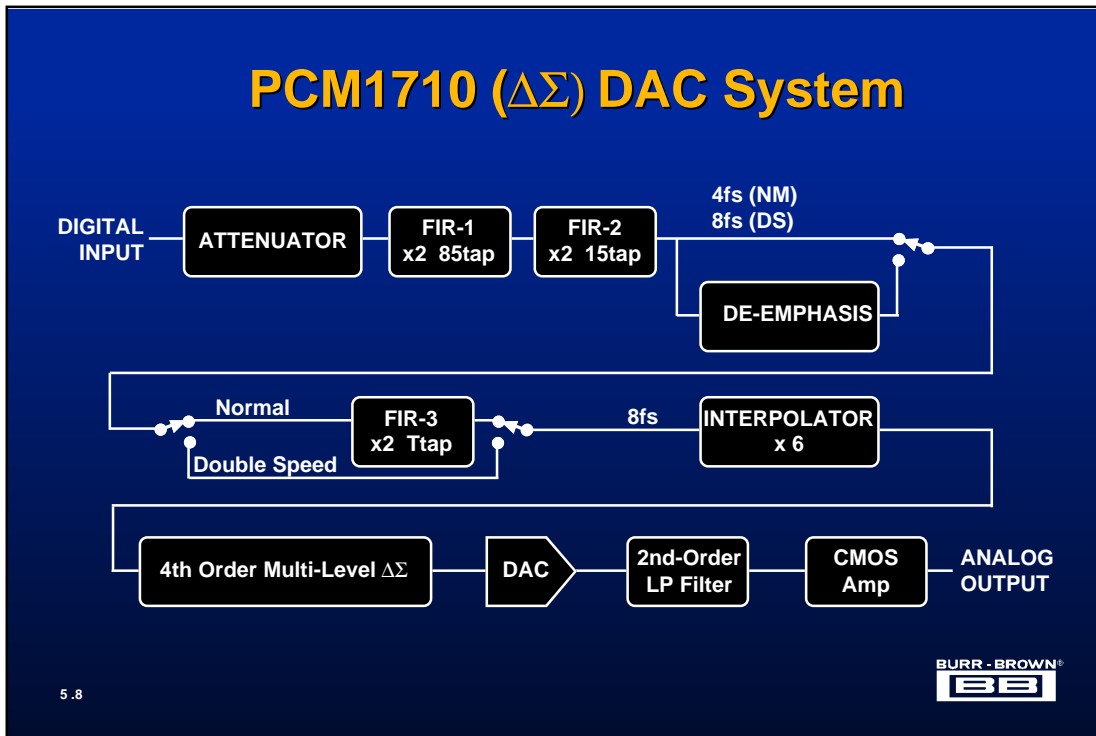
The above diagram shows a block diagram for a modern delta sigma ($\Delta\Sigma$) converter system. The word system is used because the DAC contains most of the necessary blocks that are used in the typical digital audio design.

The first block is a digital attenuator which can provide up to 255 levels of attenuation. The next two blocks are part of the digital filter. De-emphasis is controlled by a look-up table for up to three different sampling frequencies. Finally after another small section of digital filtering, an interpolation circuit, is used to create the "extra" sample points required in an oversampled DAC. This block completes the digital filtering performed in this example. The next two blocks are the core of the $\Delta\Sigma$ conversion process and will be covered in the next slide. Even though this device works with a high rate of oversampling some low pass filtering is still required. The 2nd-order filter is included for this reason. The CMOS amplifier is used to drive very light loads like 600Ω headphones.

PCM1710 DAC Topology
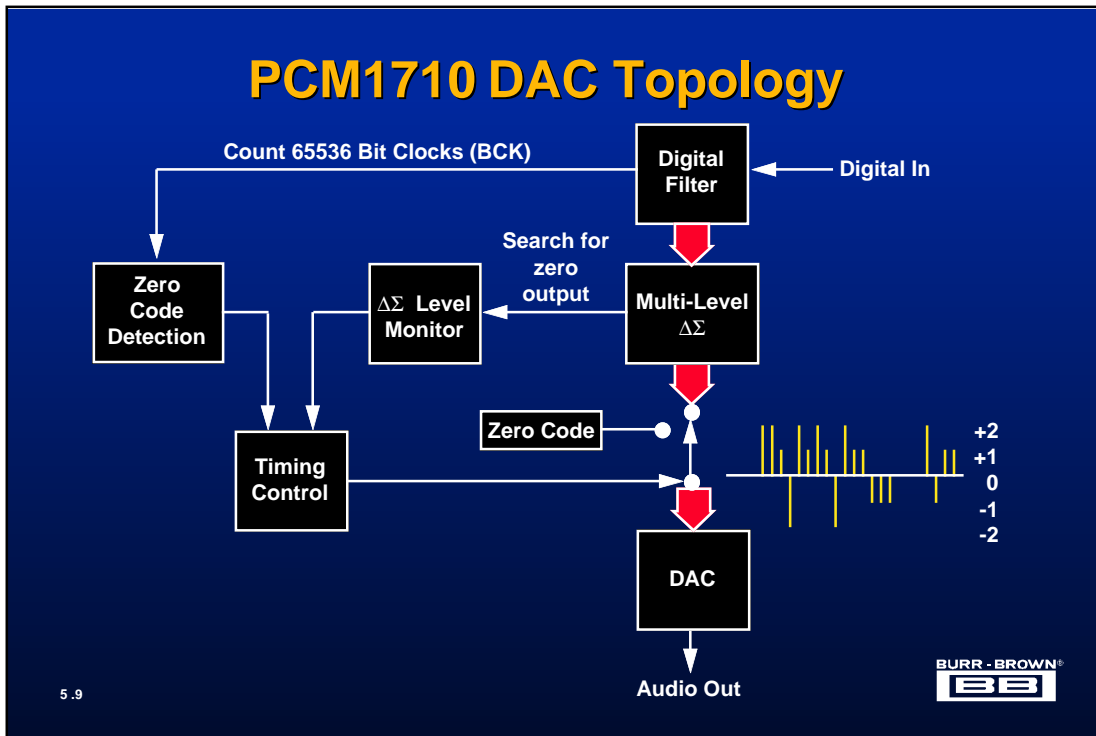
The above diagram details the internal construction of the 4th-order multi-level delta sigma ($\Delta\Sigma$) DAC section from the previous page. The key component of this DAC block is the multi-level delta sigma block which emits 4 different levels of signal at a very fast rate. This quantizer does not emit the instantaneous analog equivalent of the digital word but rather the output is the average of the incoming word. This signal is then low pass filtered so that the final signal is the analog equivalent of the digital word.

The zero-code detection circuitry is used to mute the output of the DAC during the presence of no signal, such as the gaps present between songs on a CD. Dynamic Range is tested, for audio products, by presenting a zero code to the DAC and measuring the level of noise present in the output. For the delta sigma topology that uses zero code detection, this measurement really shows how quiet the output section of the DAC is since it is shorted to ground. Zero code detection gives the delta sigma converter an obvious advantage over the R-2R topology since this detection can only be done in a digital manner.

Quantization Error

- **Analog signals are continuous**
- **Digital signals have discrete values**
- **A digital word that is converted to an analog signal will always contain errors**
- **Quantization Error or Noise is dependent on the number of bits used in the conversion**

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In the process of converting from an analog to a digital signal, the resolution of the conversion is governed by the number of bits used in the converter. As a result, a theoretical error corresponding to the discrepancy between the analog signal and the smallest digital value is generated. This error is defined as a "Quantization or Noise" error.

The level of quantization noise, N_Q, can be calculated using the following equation:

$$N_Q = \frac{1}{12} \bullet V_{LSB}^2$$

The value of the least significant bit or V_{LSB} is given by:

$$V_{LSB} = \frac{V_{FSR}}{N-1}$$

Where V_{FSR} is the full scale output range of the converter and N is the number of bits used in the conversion.

The Dynamic Range (DR) and/or Signal-to-Noise Ratio (SNR) is also an important measure of a converters accuracy. These two performance parameters are calculated from the following equation:

$$SNR = 6.02 \bullet N + 1.76 \{dB\}$$

It is common for audio converter manufacturers to define the DR as the measured THD+N when the output level is set at -60 dB. This is the Electronic Industry Association of Japan (EIAJ) definition.
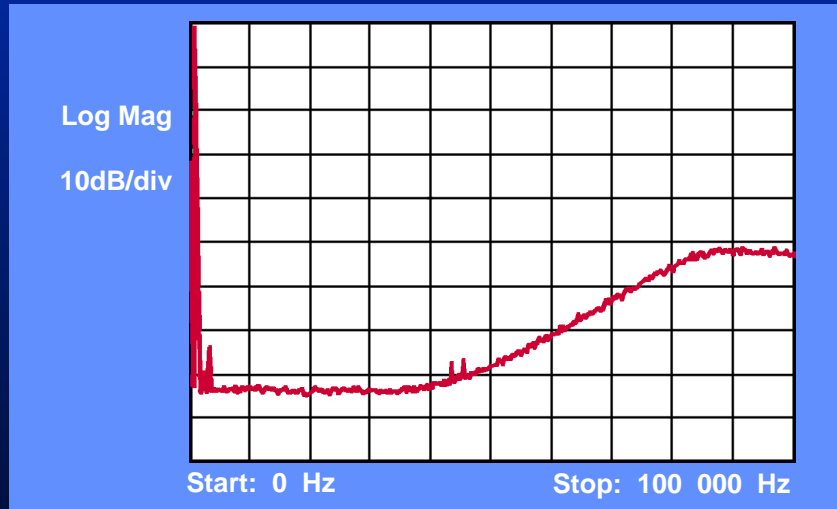
The delta sigma converter uses "noise shaping" to achieve good low level performance and quantization noise is shifted to higher frequencies. If this noise is left it can cause problems for sensitive equipment that may be "downstream" from the DAC.

Usually an application question that involves this issue or problem begins with a statement that the THD+N or SNR of the DAC is not as good as the data sheet states. What is typically happening is that this high frequency or out of band noise is causing the test equipment to saturate or operate in a nonlinear manner. Even the Audio Precision system, used by many in the audio community, is sensitive to this noise.

To solve these problems, a very high order 20kHz low pass filter is used at the output of the DAC when testing the dynamic performance of these Delta Sigma products.

This does not imply that this filter must be used for all delta sigma applications. Only in those applications where the recreated digital audio data might go somewhere other than to a human ear.

Just as a note, the human ear is a very good 20kHz low pass filter, hence this noise does not tend to make the human go nonlinear.

The Sampling Theorem is as follows:

A band limited signal x(t), having no components above f_H hertz, is *completely* specified by samples that are taken at a *uniform* rate greater than 2 times f_H. In other words, the time taken between samples is no greater than $1/(2 \cdot f_H)$ seconds. The frequency $2 \cdot f_H$ is known as the *Nyquist Rate.*
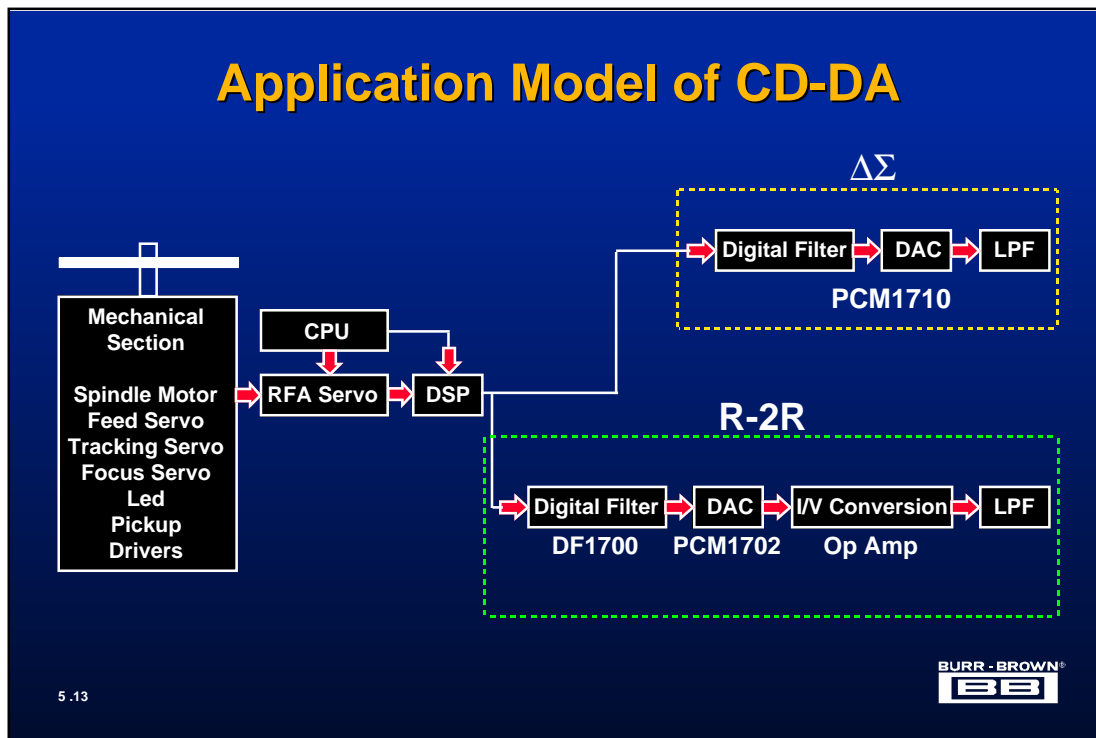
Since human hearing extends to 20kHz sampling frequencies that accommodate this range, the Nyquist Rate must exceed 40kHz. The most common commercial sampling frequency is 44.1kHz. Other sampling frequencies such as 32kHz are used for special purpose applications, in this case to extend medium time.

The mathematical foundation for translating a continuous signal in the time domain to one in the frequency domain, is governed by convolution. Basically this operation allows us to mathematically sample a signal and see the results.

For an input signal f(t) and a sampling pulse u(t) the resulting sample is g(t) and is given as:

$$g(t) = f(t) \cdot g(t) = f(t) \cdot k + 2 \cdot f(t) \cdot k \cdot \sum_{n=1}^{\infty} \cos (n \cdot \omega_S \cdot t)$$
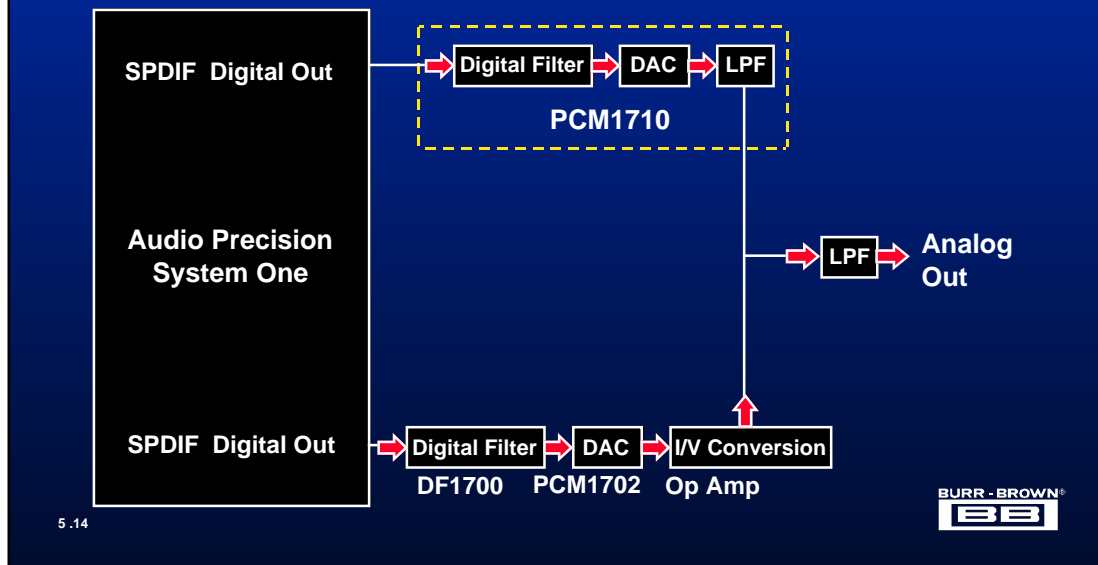
Application Model of CD-DA

$\Delta\Sigma$

Digital Filter → DAC → LPF

PCM1710

Mechanical Section

Spindle Motor
Feed Servo
Tracking Servo
Focus Servo
Led
Pickup
Drivers

CPU

RFA Servo → DSP

R-2R

Digital Filter → DAC → I/V Conversion → LPF

DF1700   PCM1702   Op Amp

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The compact disc or CD-DA is the most common source of digital audio data. The above diagram shows a typical block diagram for a CD player. Depending on which technology path one chooses for the DAC the overall component count changes.

As can be seen the analog or R-2R path necessitates an external digital filter and I/V conversion operational amplifier. Delta sigma converters, being highly integrated, offer a built in digital filter. Also the delta sigma conversion technique does not require I/V conversion since the conversion technique is 100% voltage driven.

Performance Comparison Connection Diagram

SPDIF Digital Out → Digital Filter → DAC → LPF
PCM1710

Audio Precision System One

LPF → Analog Out

SPDIF Digital Out → Digital Filter → DAC → I/V Conversion
DF1700 — PCM1702 — Op Amp

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Now that the two topologies have been compared in a theoretical manner, the actual performance of these two-converter systems will be compared and contrasted.

The THD+N, level linearity or frequency response, and noise performance of each system will be examined.
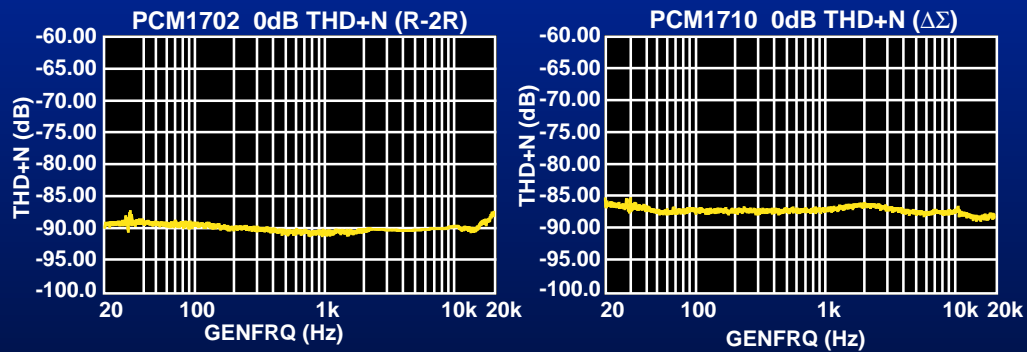
The above slide shows the 0dB or full scale output THD+N results for both DAC architectures. The performance of the R-2R system (PCM1702) is superior to the delta sigma topology (PCM1710) by a small but measurable amount.

The conclusion that can be drawn from this comparison is that for high amplitude outputs the architectures are equivalent.
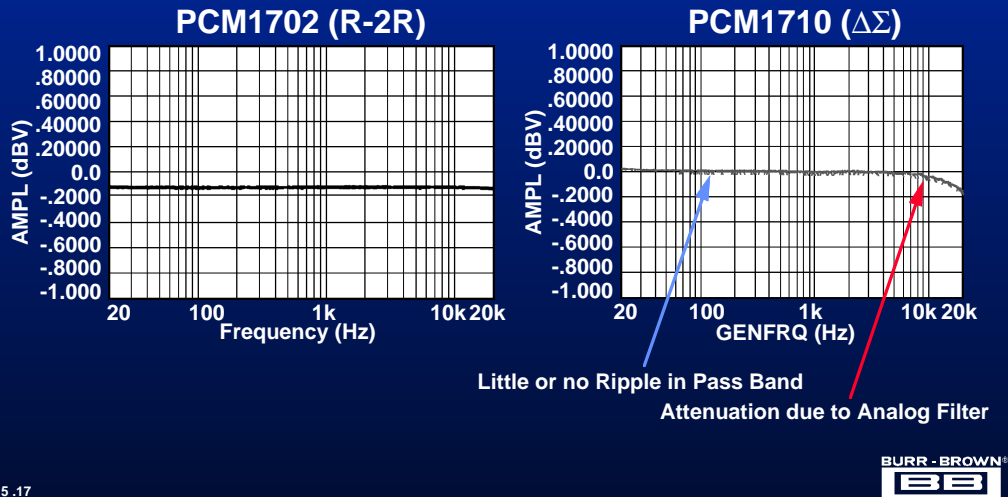
-60dB THD+N Evaluation

PCM1702 -60dB THD+N (R-2R)

PCM1710 -60dB THD+N (ΔΣ)
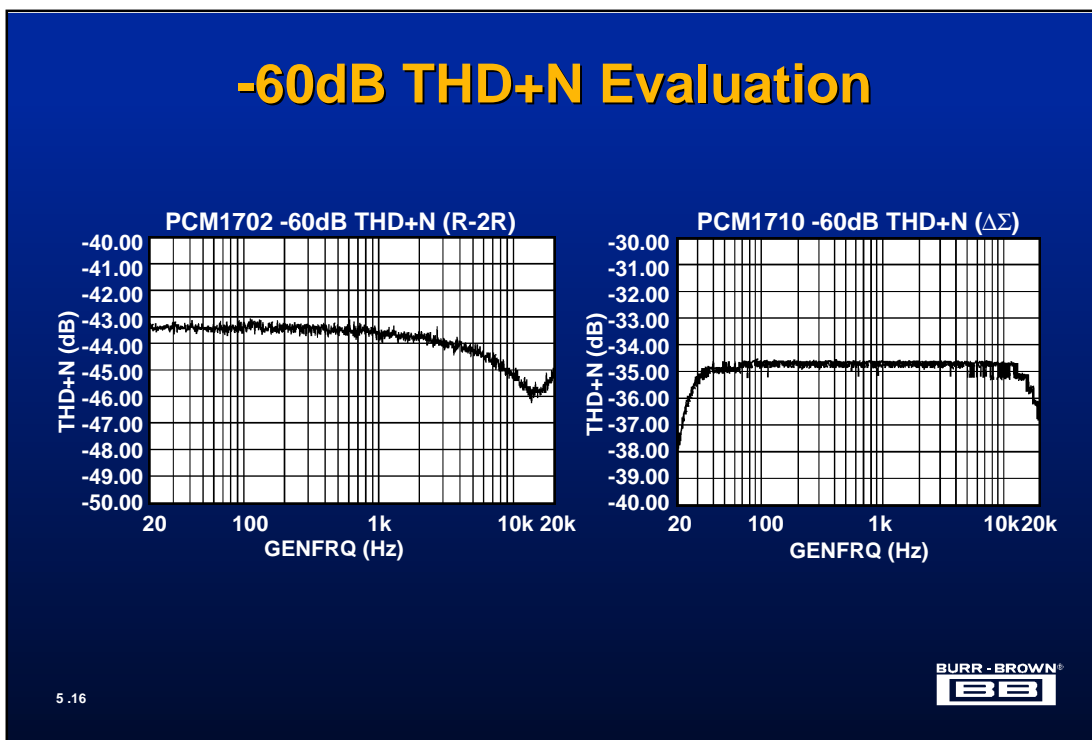
The above graphs show the same evaluation as the previous slide only with the output level set to -60dB. Note the different scales used for the R-2R and delta sigma devices.

In this evaluation, the R-2R (PCM1702) device is clearly superior to the delta sigma device (PCM1710). Again, the fact the R-2R device is a Colinear product and has no zero crossing glitch makes it exceptionally well designed for low level performance.

Frequency Response Comparison

PCM1702 (R-2R)   **PCM1710 (ΔΣ)**

Little or no Ripple in Pass Band

Attenuation due to Analog Filter

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This diagram compares the frequency response for both converter types at maximum output level. Notice how the R-2R device (PCM1702) has no ripple or change in amplitude versus frequency. The reason for the excellent performance of the R-2R system is that both the digital filter and analog portions of the system are of high order and physically large. The reason for the attenuation of the delta sigma system (PCM1710) is that the analog section of this DAC can not be made very large since it is fabricated on a digital process.

Once again performance has been traded for silicon real estate.

PCM1712/17 Frequency Response
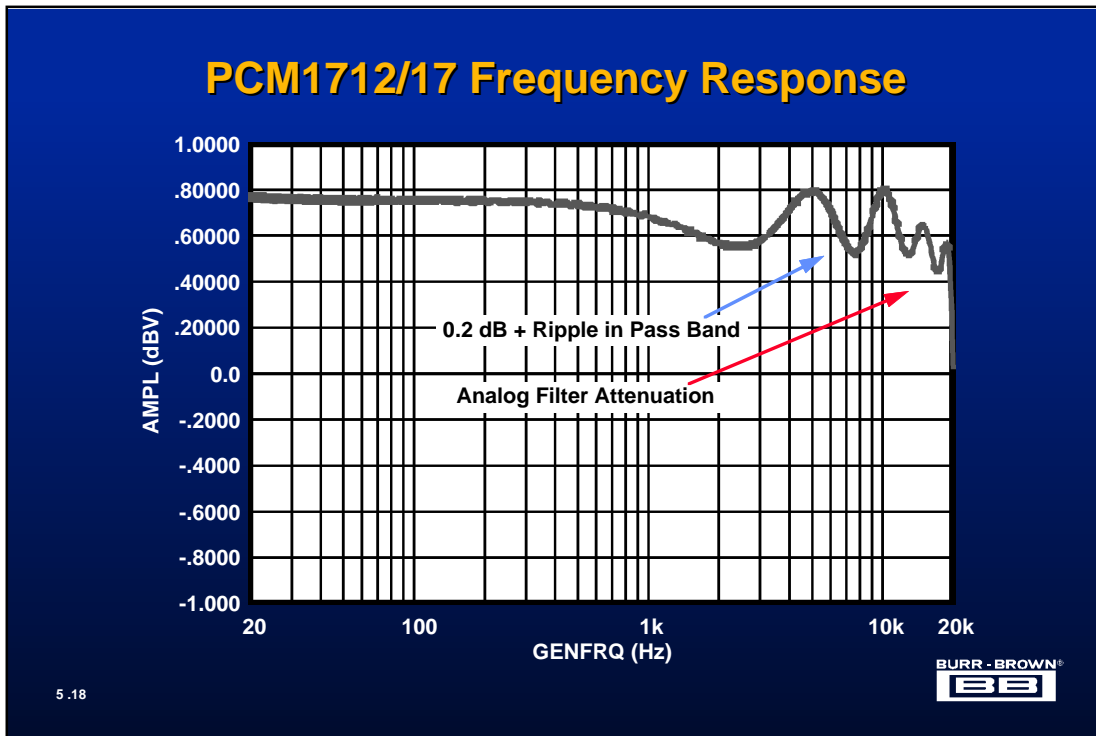
In the case of the PCM1717 or the PCM1712 the digital filter has been reduced in area by approximately 50%. This results in a cost savings of approximately 20% for the entire DAC, since the analog components cannot be downsized.

This reduction in digital filter area shows up as observable pass band ripple. The data sheet quotes a typical value of 0.17dB and this is very close to what has been measured.

Like the PCM1710/15 a high order analog filter is not used and some high frequency attenuation is observed.

Performance Comparison Table

	$\Delta\Sigma$	R-2R
Low Cost	√	
More Features	√	
Higher Integration	√	
Better Level Linearity		√
Lower THD+N (0dB)	√	√
Lower THD+N (-60dB)		√
Lower SNR	√	
Jitter Tolerant		√
For Professional Use		√
For Consumer Use	√	

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The above table summarizes the performance and features obtainable from both systems. While the R-2R system is the clear winner in overall performance, it must be remembered that none of the features – de-emphasis, mute, zero-detection etc. – are available in the systems that have been evaluated. Also all of this performance is obtained by an overall increase of 10x in cost.

The SPDIF format is the most common consumer interface. If you have seen a CD player that can transmit digital audio data, it is transmitting SPDIF data via a BNC or Phono plug connection. This is the interface that the Audio Precision test equipment uses. All Burr-Brown PCM DACs and ADCs are compatible with this format when used with the appropriate receiver or transmitter devices.

The AES/EBU format is a professional format that is typically used in studios. This format is in fact the basis of the SPDIF format.

The basic difference between these two is the type of connector used, termination impedance, and output signal level. The AES/EBU connector and format is a balanced, i.e. transformer coupled version of the consumer format signal. This format will only be encountered in a professional studio environment or application.

The I2S or Inter-IC Sound Standard was developed by Philips to allow audio data exchange between converters, filters and digital input/output interfaces. The serial interface is a three-wire bus that contains a line for two time-multiplexed data channels (Data), a word select line (L/R clock), and a clock line (Bit Clock). The standard also dictates that the actual audio data be delayed by one Bit Clock period from the L/R clock.

The human ear does not have a flat response. Many of the PCM specifications have the typical human ear response factored in. A typical A-weighted curve is used to modify the actual measured response by some amount. A good rule of thumb is that the difference between the actual listened to response is by 1 or 2 dB.

Unfortunately the term "oversampling" has gained acceptance for two entirely different meanings.

In oversampling A/D conversion, a digital filter is operated as a digital low pass filter. This process is referred to as decimation. Frequency components outside of the audio band are removed to prevent aliasing. Essentially the Nyquist frequency is extended or increased. An analog low pass filter is still required but the order is reduced, and cutoff frequency is increased.

An oversampled D/A conversion is called interpolation. Between every valid bit received a zero is inserted. The result is that for a 2x oversampled signal the sampling frequency is increased from 44.1kHz to 88.2kHz. This process has been extended up to 8x.The DAC still requires an analog low pass filter but as before, the resulting filter is still much simpler to design without affecting the reconstructed analog information.

Digital Audio Terminology

- **Emphasis - First Generation technique for high frequency restoration**
- **BTC - Binary Two's Complement**
- **Zero Crossing Glitch is caused by uneven switching of current sources in R-2R DAC**

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Early CDs were recorded with an update or sampling frequency of 44.1kHz. This resulted in a loss of amplitude in the high frequency signals. These signals were thus boosted or emphasized so that when the digital audio was reconstructed the high frequency amplitude was correct. Advances in digital filtering have eliminated this problem and now CDs are recorded without emphasis. However, the digital filter must allow for the older format.

The binary format used in digital audio transmission is called binary two's complement. This format allows for 32768 different signed integers in the 16-bit world.

Unfortunately this format requires that all of the bits must switch from all ones, binary zero minus 1LSB, to all zeroes, binary zero, when the analog signal transitions through zero. The resulting output from a R-2R DAC can contain a glitch due to the fact that all of the current sources are switching at the same time. This problem can be solved in a variety of manners. The cleanest response is achieved by using two back to back DACs. This is the topology that is referred to as "CoLinear".

- **Determined by the rate at which the LRCIN clock changes**
- **Performance is guaranteed for a narrow band of clock frequencies**
- **Minimum is determined by refresh rate of internal memory devices for delta sigma**

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Delta sigma converters are entirely digital devices or state machines. In essence the PCM1710 is like a small computer programmed to perform a specific task. Like other computers the PCM1710 uses memory or DRAMs and this memory must be refreshed from time to time.

The rate at which the refresh process occurs is determined by the system clock. Since this clock is a multiple of the sampling frequency any limits or bounds placed on the system clock will also affect the sampling frequency.

The lowest sampling frequency at which the PCM1710 has been found to work is 10kHz, and this figure is not guaranteed. Usually customers who are interested in the lower sampling frequency are industrial users.

The maximum sampling rate for any DAC type is determined by the settling time for the DAC.

Clock Generation

- **Clock sources should be a crystal-based for best jitter performance**
- **Multiple converter systems should use a buffer to drive clock inputs**
- **XTI/XTO connections are for single use only**

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Every item of a digital audio system will require a stable source of timing i.e. a clock. Jitter, or a difference in time between adjacent clock pulses, will affect system performance.

Given that a digital audio system is being commanded to convert an audio signal of frequency "f" clock jitter will cause the bandwidth of the reconstructed audio signal to spread out.

If we were to observe the resulting signal in a jitter free system on a spectrum analyzer the reconstructed audio signal would have have a width, in frequency equal to the window frequency of the spectrum analyzer. Clock jitter causes the width of the fundamental frequency to spread. Additionally the jitter frequency, whether random or distributed, increases the value of the noise floor. Hence SNR and THD+N are both degraded.

Crystal-based clocks offer the best jitter performance. If used in a multiple converter system this clock should be buffered and sent to all devices requiring a clock.

The clock out pins on audio A/D and D/A converters should only be used to drive one other device. Typically the digital drive capability of these devices are limited and hence should be buffered if additional devices need to be driven.

WORD-CLOCK JITTER

JITTER-FREE CLOCK

JITTERED CLOCK

JITTERED CLOCK

5 .25

Word-clock jitter can deteriorate a systems performance. When trying to achieve high bit accuracy, close attention needs to be paid to what the word-clock looks like. Jitter in a system is a noise that is apparent on the word-clock and is the difference where the falling edge of the clock occurs. Jitter is difficult to measure in most systems and there are few jitter analyzers available today. Pay very close attention to this especially when an optocoupler is in use in a system. Very poor jitter results are obtainable with these kind of parts and this will deteriorate the system performance.

If isolation is required for the digital signals in a digital audio system it is better to use capacitance based isolators like the ISO150.
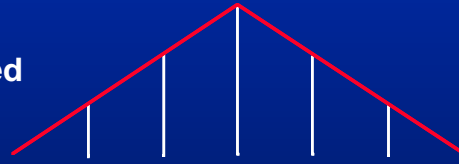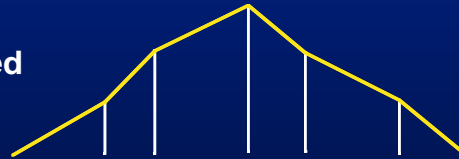
"How sour, sweet music is when time is broke and proportion kept!", Shakespeare, Richard II. Shakespeare never knew how well he would describe a phenomenon in digital audio call "Jitter".

The above diagram shows what can happen to a reconstructed signal if the word-clock or sampling clock changes period length from sample to sample. The amount of cycle-to-cycle change is referred to as jitter and is measured in seconds. There is no good analytical method of describing jitter effects on a converter but there are two effects that are known to occur.

The first would be the introduction of spurious harmonics that could exceed the noise floor of the converter. The above equation describes the SNR achieved when the sample clock is not jitter free where:
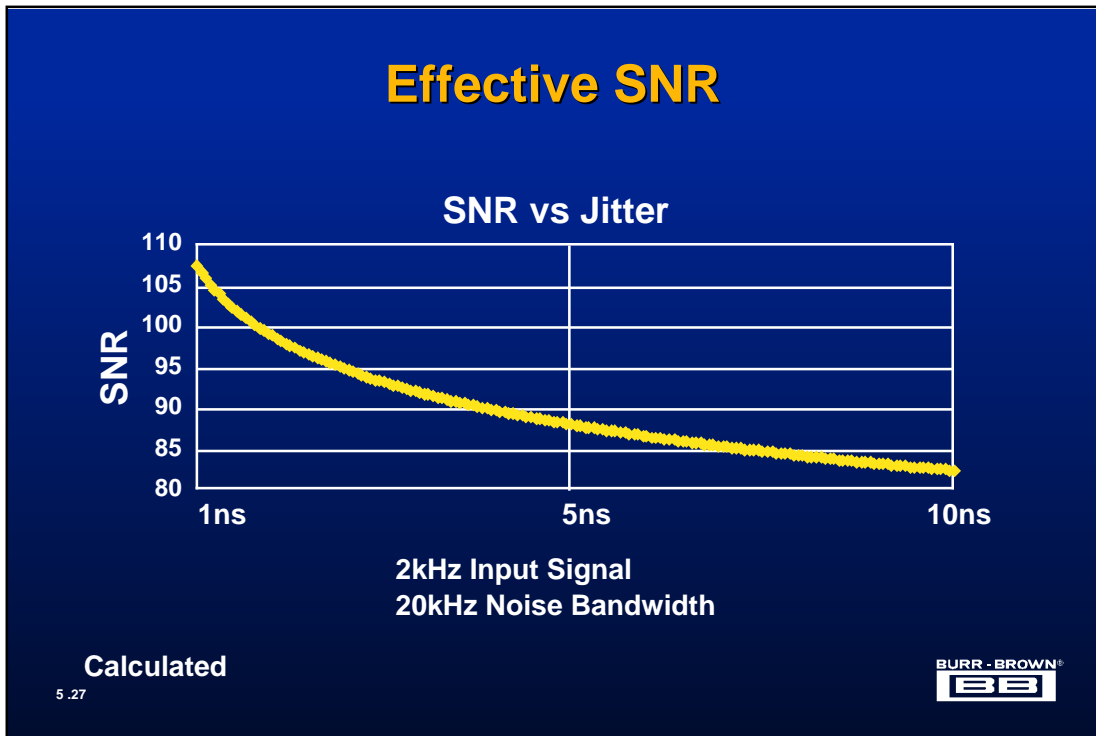
t = rms Jitter (seconds)

f = Signal frequency (hertz)

f_O = Bandwidth of noise measurement (hertz)

f_S = Sampling frequency (352,800 for 8x oversampling) (hertz)

The second effect is described as spreading of the fundamental. What happens is that the width of a given fundamental will increase in the presence of word-clock jitter. In a jitter free environment a fundamental frequency tone would show up on a spectrum analyzer as an impulse. As jitter is introduced this impulse begins to spread.

Effective SNR

SNR vs Jitter

2kHz Input Signal
20kHz Noise Bandwidth

Calculated

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This plot is done with:

F_S = 100kHz (Sampling Frequency)
F_B = 20kHz (Noise Bandwidth)
F_{INPUT} = 2kHz (Signal Input)

The SNR equation from the previous page is shown here solved for the above conditions and plotted for RMS jitter from 1ns to 10ns. If a 16-bit system was to built for the above conditions the theoretical SNR would be 98.08dB. Achieving this theoretical condition in the presence of a jittered system would necessitate an RMS jitter of less than 2ns.

Almost every PCM application circuit will require the use of external active devices. In fact, it is safe to assume that every Delta Sigma device will use an external low pass filter. Even with devices like the PCM1710 which has an internal low pass filter, external filtering is recommended to reduce the high frequency noise inherent in these parts.

For current out DAC devices, like the PCM1702, an op amp operated as a transconductance amplifier will be necessary to produce an output voltage.

The op amp should have a low offset voltage and minimal bias current as these characteristics will affect DC performance. Provided the DAC has the capability for offsetting, the effects of these departures from ideal performance in the op amp can be "trimmed" out.

- **Low Noise**
- **Low THD**
- **Compatibility with Existing Power Sources**
- **Output Drive Capability**
- **Slew Rate**

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As to AC performance, noise and THD are the driving parameters for op amp selection. In the end the audio applications demand a THD+N performance of at least -80dB, and -100 dB is not that uncommon. Thus an op amp should be chosen that has less than $100\mu V$ and $10\mu V$ respectively of noise referred to the output. Note that this specification is not difficult to achieve with low noise devices.

It almost goes without saying that if an audio system has been designed to use $\pm 5V$ supplies, designing in op amp that requires $\pm 15V$ will not represent a good design choice.

If the output of the digital audio system is required to drive a heavy load, a power op amp or buffer will be required. Even if the load is another high impedance device, buffering the output of the system will result in better noise immunity and prevent loading affects on the analog portion of the system.

Even though most audio systems are designed to have a bandwidth of 20kHz the external op amp should have a bandwidth that exceeds this. Specifically, an external op amp should be able to slew fast enough to make up for nonlinearties that will be inherent in musical outputs. In general an external op amp circuit should have a 3dB bandwidth that exceeds 200kHz.

Maintaining Op Amp Gain Accuracy

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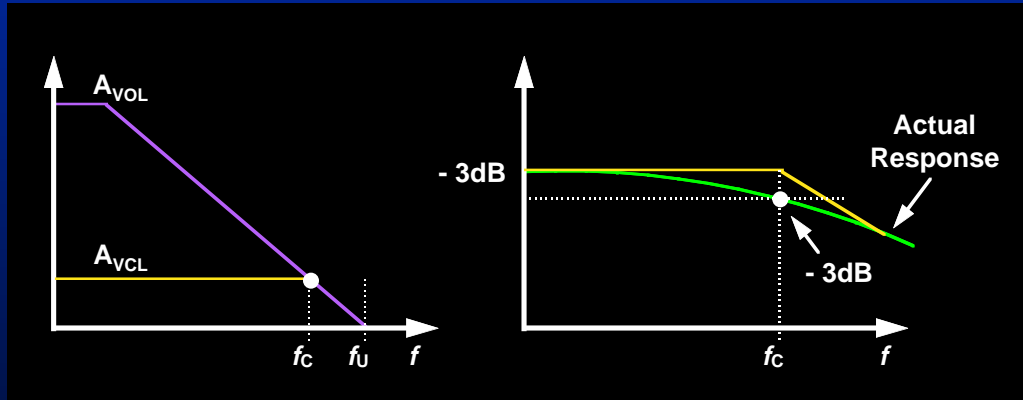
One major consideration is to maintain excellent AC gain accuracy over the specified bandwidth of the system. Most unity-gain stable op amps have a single-pole response, where the AC gain degrades due to the closed-loop pole. Thus, for these single-pole systems, the actual gain of the op amp will be:

$$\text{Actual Gain} = \frac{\text{Ideal Gain}}{\sqrt{1 + (\dfrac{f}{f_C})^2}}$$

The resulting amplitude error, in percent, can be expressed as:

$$\in \% = \frac{1}{2}(\frac{f}{f_C})^2 (100)$$

where f is the frequency of interest.

Op Amp Gain Accuracy

$$f_C = \frac{f}{\sqrt{(\frac{\in\%}{100})} \times 2}$$

- $f_c \geq 363f$ for 0.00038% (16 bits)
- $f_c \geq 91f$ for 0.0061% (12 bits)
- $f_c \geq 46f$ for 0.024% (10 bits)
- $f_c \geq 23f$ for 0.1% (8 bits)

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We can solve the preceding equations for the necessary closed-loop pole frequency, f_C, necessary to achieve a given level of accuracy at a given frequency (f). The ratio shown here is typical for several different accuracies.

As an example, for a 16-bit system that requires 20kHz bandwidth, the closed-loop pole frequency must be at least 7.26MHz.

The conclusion that can be drawn from this example is that accurate high resolution systems require fast op amps.

Op Amp Gain Accuracy

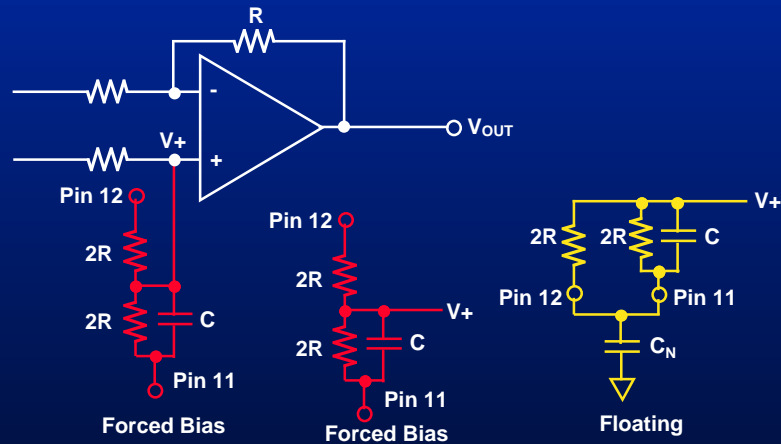For a given frequency, f, closed-loop pole frequency f_C should be:

0.25 LSB Accuracy
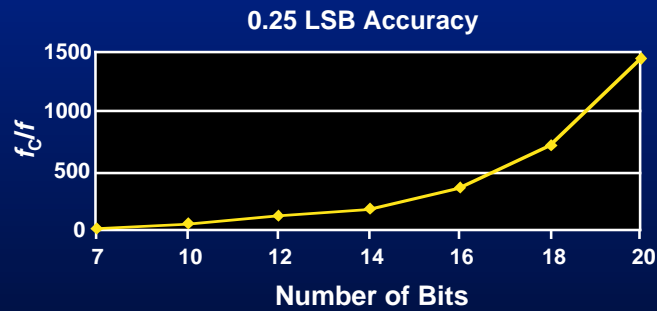
5 .32

This graph can be used to determine the closed-loop pole frequency necessary for a given level of accuracy normalized to a signal frequency of 1Hz.

PCM1710 Output Op Amp

The above diagram is a schematic of the output op amp section of the PCM1710 and PCM1715. The pin numbers refer to the pins of either DAC.

Unless this op amp is configured correctly, the low frequency performance will be impaired.

In general there are ways to configure the output op amp of the PCM1710. These modes are referred to as "Forced Bias" and "Floating".

In the forced bias case, the bias section of the noninverting terminal of the output op amp is referred directly to ground. While this configuration represents the simplest or least component count option, it also causes the output of the op amp to rise with respect to frequency at low frequencies.

The preferred configuration is to use a capacitor to terminate both points to ground with a capacitor. A value of $10\mu F$ will keep frequency response flat below the audible band. This configuration is referred to as floating bias.

- **Should be well regulated and clean**
- **Must have a known power-up condition**
- **Must be bypassed sufficiently to keep power supply constant during peak transients**
- **Should have sufficient head room**
- **Always assume that a reset condition will occur if the power drops below specified minimum**

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Switching supplies are not suitable for audio systems due to the high frequency noise they contain. If the source of power is a switcher that voltage should be regulated down with the use of a linear supply.

The power supply should be checked at power up and at other transient conditions to verify that the power conditions of the PCM device are not exceeded. A transzorb or other transient device might be necessary if all power conditions are not known.

To keep the analog sections in their linear regions sufficient headroom, or a difference between the maximum output and the power supply voltage, must be maintained. While 2V may seem to be on the high side this value does allow for differences in the power supply outputs and due to regulation effects.

Many of the newer PCM products are much like a microprocessor in that they have a power up or boot condition. Dropping below the minimum power supply specification will cause these devices to assume their power up condition. This condition may be different than the desired mode of operation. If the desired condition is hardwired into the circuit via connections to ground and or power supplies, this condition is avoided.

External Components - Capacitors

- As a minimum a low value ceramic should be used for all connections
- Any high current points should also be bypassed with a larger value tantalum
- Experiment with different values on a breadboard

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While the term digital audio might imply a system that is entirely digital anyone who has ever used an audio DAC can tell you that the system is actually a complex analog one with a digital interface. The system requires good analog design practice for acceptable performance.

Nothing in the analog system design is more important than establishing good high frequency bypass or ground points.

All designs will require $1\mu F$ ceramic capacitors as a starting point. These capacitors will establish an AC ground that is good out to the 100MHz region. Unless additional loads are driven by the reference or analog outputs additional capacitance will not be necessary. If additional capacitance is required usually $10\mu F$ tantalum types will suffice.

The final decision as to the amount and type of capacitance will have to be made when the layout is finalized.

As a note many designers have tried, without much success, skipping the prototype and or breadboard step. It is important to remember that layout effects will sometimes either make or break a design. The use a demo board is very much encouraged to verify system performance.

So far we have spent a lot time talking about the PCM1710 in digital terms this is not meant to imply that the converter is entirely digital. However, since the device works from a single 5V supply there is a tendency to simply use noisy digital supplies to power the converter and this is a mistake.

Both the analog and digital supplies of the $\Delta\Sigma$ converter should be operated using the analog power supply. Additionally, these supplies should be well bypassed at the converter.

The capacitors must be a 0.1µF ceramic paralleled with a low ESR, less than 0.5Ω, 100µF electrolytic or tantalum type. There is a tendency to use capacitors rated for high voltage like 25 or 50V and this is not necessary, since most of these converters can not handle more than 5V. Additionally the higher the voltage rating is for a capacitor the higher the ESR is. Analytically what should be achieved is an impedance that is less than 2Ω at 1kHz.

Industrial Applications

- **PCM products are less expensive than their industrial counterparts**
- **They are not specified, tested, or recommended for DC performance**
- **You can not hear DC**
- **There are some industrial applications for which PCM products are appropriate**

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A good example of a very application specific market for data converters is the audio market. Here converters must be "mostly precise". That is, the application is such that the analog signal of the converter will be passing through many digital codes continuously. So, if the majority of the conversions are precise, then the output is acceptable.

If we compare the audio market to the traditional data converter market, we find that the data converter market requires high precision and repeatable results. Another way of saying this is that the data converter market requires devices that are as absolutely precise as possible. The audio market on the other hand requires devices that are specified for AC performance only.

All of these caveats are not meant to imply that audio converters are unsuitable for other applications. They simply do not offer the guaranteed performance of traditional industrial converters.

The bottom line is to check the converter's specifications carefully. Audio converters are tempting, because they are inexpensive.

A major part of a design engineers job is helping the customer decide on a device while making a decision among various tradeoffs. Even if the designer has done extensive characterization of unspecified parameters and designed based on this characterization, unspecified parameters may still change.

Digital Audio Summary

- **Digital Audio DACs fulfill special requirements**
- **Modern DACs are highly integrated**
- **Audio systems are often specified in non-engineering terms**

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DACs used for digital audio applications are the best of both the user's and manufacturer's world. The user gets a lot of features and performance for a relatively small cost. The manufacturer can sell large volumes of these products at this small price because the die size is small and the yields are high. The biggest reason for this is that the DC performance of these products does not need to be tested. Specifications such as differential non-linearity and monotonicity which require a lot of test time for the manufacturer are not necessary. The caveat is that these DC specifications are subject to change at any time. If the application calls for DC performance, build it in via an industrial part. If the application demands a certain level of THD+N then the audio DAC is the choice.

Most DACs being designed today rely on control from a microprocessor or DSP to achieve the full functionality achievable from the DAC. If the application is low cost, or does not demand a lot of features, all of these DACs can be hardwired into simple configurations.

Audio system performance is frequently specified and compared using non-engineering terms. At the risk of alienating the audiophile community, terms like "Sounds Good", "Highly Musical", and "Spatial Detail" do not evoke any engineering design methodologies or techniques known. If possible, these characteristics should be related to an analytical or designable parameter.