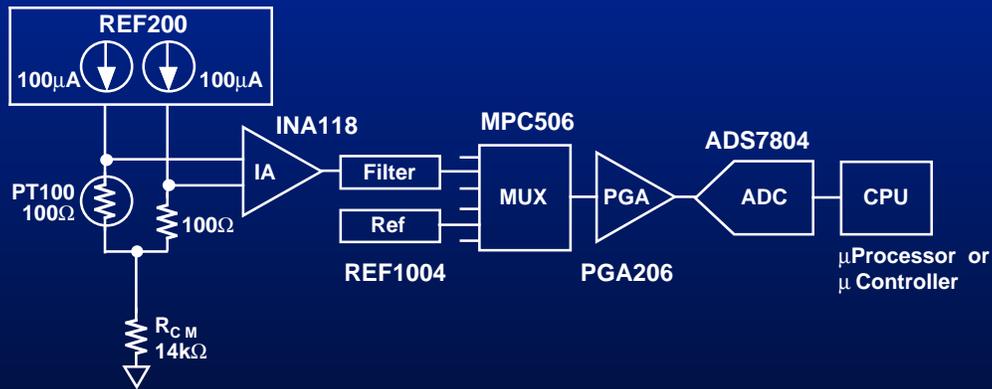


Intelligent Process Controls and Monitoring

- **Discrete versus System1.2**
- **$\Delta\Sigma$ Converter Overview1.4**
- **$\Delta\Sigma$ Design Tradeoffs1.19**
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**Contributing Authors: Bob Lee
Robert Watson**

“Discrete” Temperature Measurement System



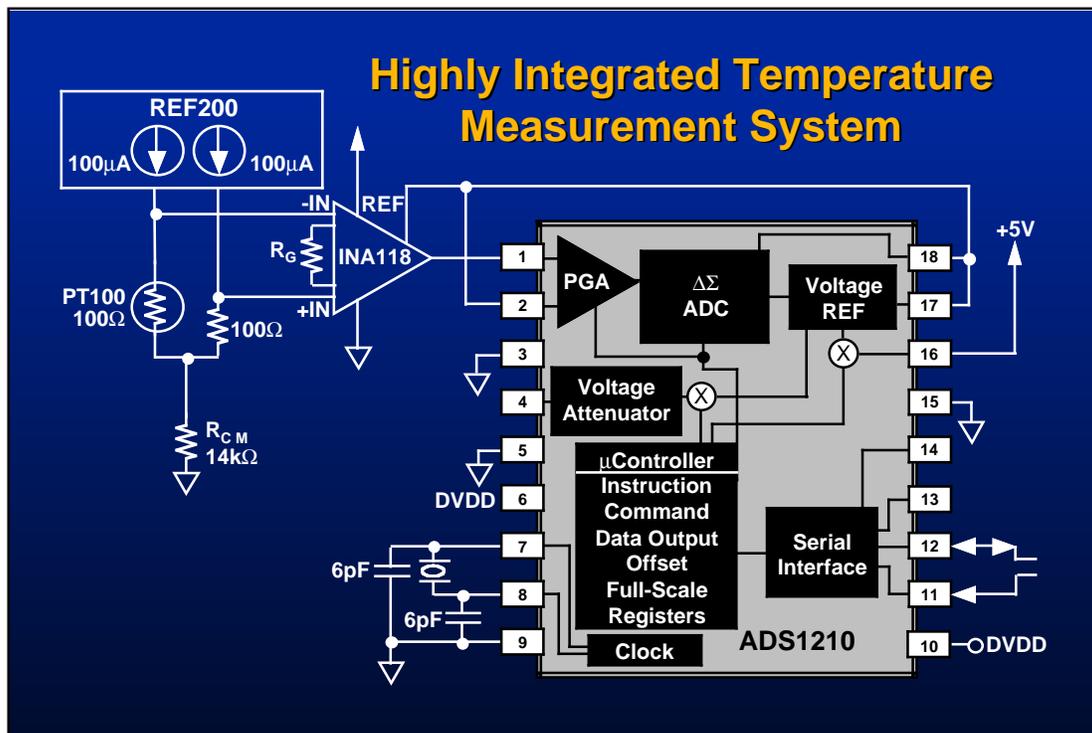
1.2

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Historically, Process Control was implemented in electrical systems using a group of independent chips in the signal path to condition and process the signals from sensors that sensed physical conditions such as temperature, pressure, light, or gas, to name a few. Before the advent of highly integrated data collection and conditioning systems, complex circuits were designed such as the temperature measurement system in this slide. In this temperature measurement example it would have required several stages in the signal path, such as an instrumentation amplifier, reference, multiplexer and A/D converter before the signal could be processed by a CPU.

This type of system had some advantages. Primarily, it was possible to upgrade any one of the different stages in the signal path, usually independent of the other stages. As an example, if the application called for better temperature accuracy, the reference could be changed.

The disadvantages of this system were cost, board space, and reliability. As the component count of this type of system is reduced these disadvantages can be diminished. To further complicate the design, bi-polar supplies were usually required, adding to the circuit complexity.



This slide shows a highly integrated approach to measuring temperature using an RTD as the sensing element. The ADS1210 $\Delta\Sigma$ converter system has an A/D converter, voltage reference, and instrumentation amplifier all in one package. The external instrumentation amplifier, INA118, is only necessary if the overall required gain of the signal is higher than 16V/V. This circuit performs the same function as the discrete version previously discussed, but requires many less components and only a single +5 volt supply.

The tradeoffs that are made when this type of converter is used include accuracy, bandwidth, and gain.

The circuit details are as follows. The REF200 is a dual current source that is used to bias the RTD and the 100Ω reference resistor. The common mode resistor, R_{CM}, raises the common mode input voltage of the INA118 to 2.8 Volts for optimum performance. This input common mode voltage allows the largest output voltage swing from the INA118 when the instrumentation amplifier reference voltage is 2.5V, the gain is large and the device is powered by a single supply.

The internal 2.5V reference is used from the ADS1210 as the reference voltage for the ADS1210 and the INA118. This reference is used not only by the converter, but is also the voltage that the input from the RTD is compared to. To ensure that reference voltage drifts do not affect the accuracy of the measurements, the 2.5V reference is also connected to the reference pin on the INA118.

Delta Sigma Overview

- What is a delta sigma ADC?
 - A 1-bit ADC with massive oversampling
 - resulting in high resolution for low frequency inputs
- What is the advantage of delta sigma
 - Essentially digital parts
 - result is low cost and high stability
- What are the disadvantages of the technique ?
 - Limited frequency response
 - Only good for continuous signals

1.4

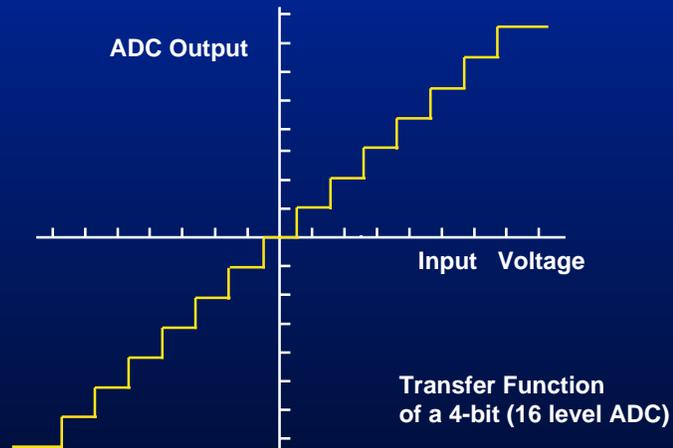


A delta sigma ADC is based on a single bit quantizer rather than multi-bit as used in architectures such as sub-ranging or successive approximation. The single bit quantizer is used with a high oversampling ratio and is followed by a digital filter. This allows the architecture to achieve resolutions of up to 24-bits whereas other architectures tend to be limited to around 16-bits.

Another way of looking at a single bit ADC is to call it a comparator. The input is either more or less than a threshold value, indicated by a '0' or '1' at the output. As will be shown, the analog part of a delta sigma ADC is very simple. With a comparator as the ADC and the bulk of the part being the digital filter, delta sigma ADCs are essentially digital parts. The result is that they can be fabricated cheaply and can still achieve high stability.

Delta sigma ADCs are very good in the right application but they do have some disadvantages. The most obvious of these is a limited frequency response. The frequency response is controlled by the output data rate, a greater data rate leads to a higher frequency response but a lower resolution. The frequency response is limited to hundreds of Hertz or the low kHz. Also they are generally only useful for inputs that change smoothly over time. Step changes to the input takes time to propagate through the digital filter.

Multi-bit ADC Transfer Function

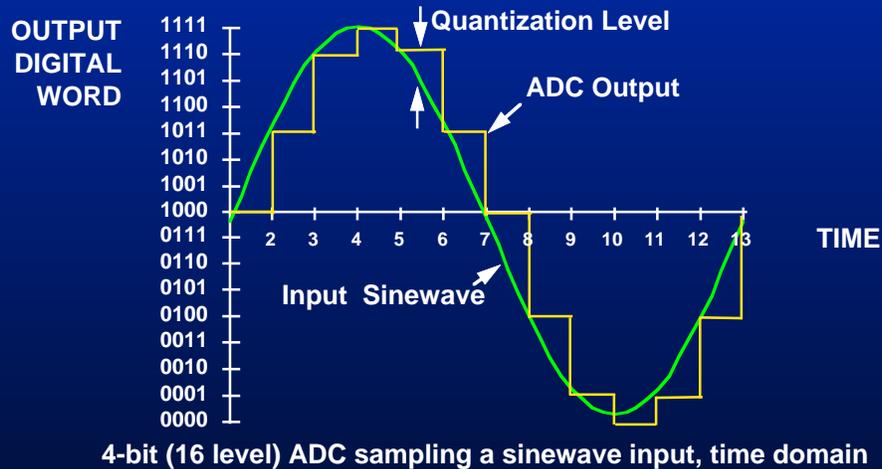


1.5

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The operation of a conventional multi-bit ADC is illustrated with a graphical representation of this multi-bit ADC transfer function. In this case the graph represents a 4-bit ADC transfer function. The input voltage range has been divided into 16 equal steps. The greater the number of ADC bits, the smaller the step size and the greater the .

Sampling and Quantization



1.6

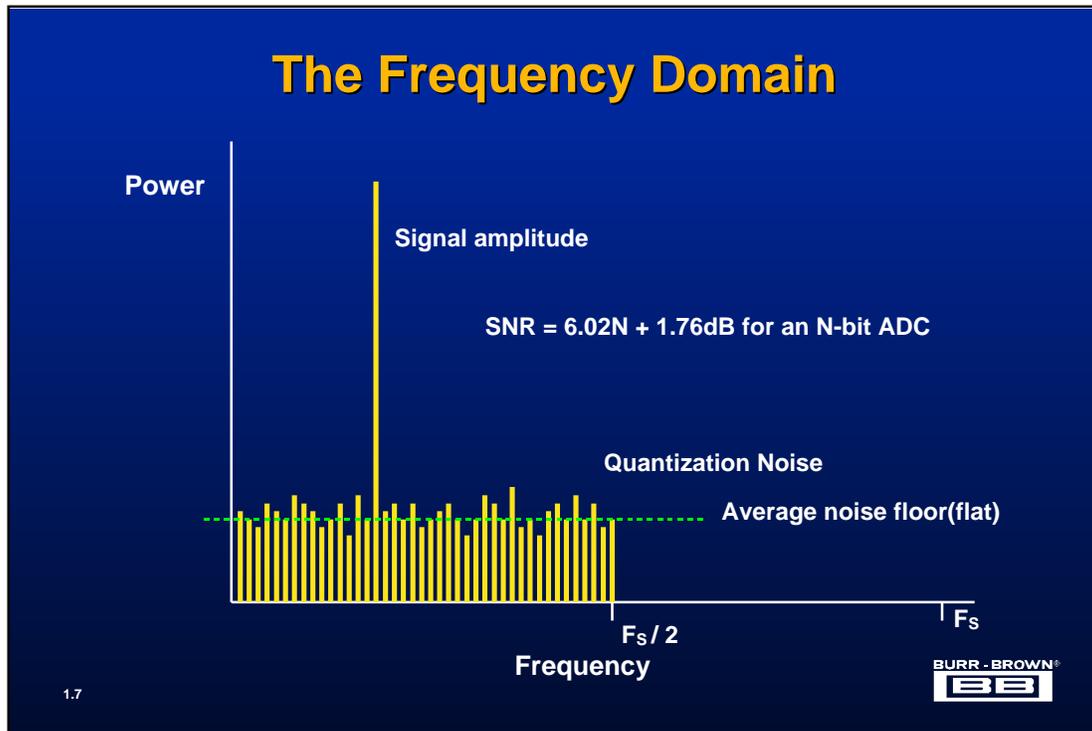


The time domain transfer function of the same 4-bit ADC is shown here, digitizing a full scale sinewave. The ADC output is drawn to correspond to the digital word. If this signal was reproduced with a DAC, the affects of sampling and quantization would be easily noticed.

Sampling means that the input waveform is only captured at certain discrete points in time. Between these points the output value is held constant. The rate at which the input is sampled is known as the sampling frequency. Nyquist theory tells us that this must be at least twice the information bandwidth of the input signal. Sampling faster than this minimum rate is known as oversampling. The delta sigma ADCs exploit the benefits that will be shown later from oversampling.

Quantization is the effect of the continuous analog input amplitude being divided into discrete levels (16 in this case). This means that most sampling points do not capture the exact input value, they capture the nearest equalization bin level. The difference between these two is the quantization error. The value of this Quantization error is up to $\pm 1/2$ LSB for each sample. If the input waveform is not correlated to the sampling frequency the quantization errors are effectively random.

The Frequency Domain

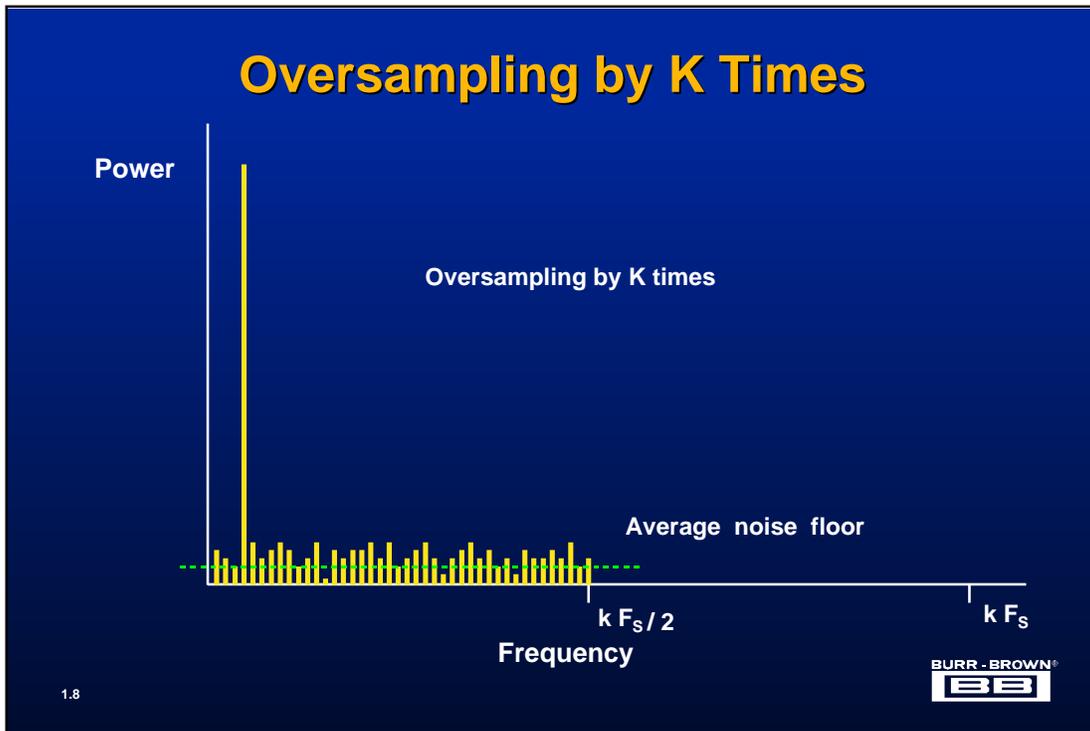


Having looked at the effects of sampling and quantization noise in the time domain, the frequency domain is examined next. This slide shows a diagram of the FFT of the waveform from the previous slide.

The signal being captured is a pure sine wave which clearly shows up as a single tone in one frequency bin of the FFT. The FFT also shows a lot of random noise in all other bins, distributed flat across the frequency range from DC to $F_s/2$. This is the effect of the quantization error and is known as quantization noise. Remember that every sample taken of the input signal has a quantization error and that the magnitude of this error is random and up to $\pm 1/2$ LSB. It is this random error, present on every sample, that generates the noise floor in the FFT. This noise is not due to any inherent shortcomings in the ADC, they have these as well, but in this case we are looking at a perfect device.

Taking the RMS sum of all the frequency bins containing noise (i.e. all except the fundamental) and dividing this into the fundamental amplitude gives the signal to noise ratio (SNR). It can be shown that for an N-bit ADC, the SNR ratio is given by $SNR = 6.02N + 1.76dB$. This formula clearly shows that the obvious way to improve the SNR is to increase the number of bits in the ADC. Conversely, when the number of bits are increased, the reproduced input signal is more accurate.

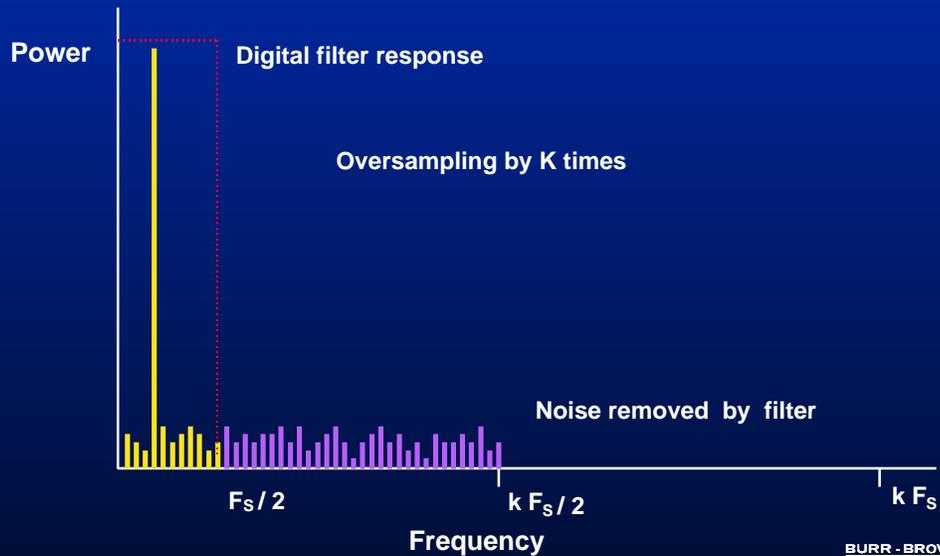
Delta sigma ADCs take another approach. This is to use a one-bit ADC with a 7.78dB SNR and the techniques of oversampling, noise shaping and filtering to improve the accuracy.



In the previous example the signal frequency was fairly close to the Nyquist frequency of $F_s/2$. Here the affects of oversampling can be seen. The signal frequency is the same but the sampling frequency has been increased by an oversampling ratio of k to $k F_s$.

Notice how this FFT shows that the noise floor has dropped. It is important to realize that the SNR is still the same as it was before, after all, the formula on the previous slide made no reference to sampling frequency. The total amount of noise energy is still the same, it has just been spread over a wider frequency range, hence the noise level in each frequency bin has been reduced.

The Digital Filter



1.9

In the previous slide it was shown how oversampling spreads the noise over a wider bandwidth and hence reduces the level of the noise floor. Delta sigma converters make use of this affect by following the 1-bit ADC with a digital filter. The affect of this filter is to restrict the noise bandwidth. Since most of the noise now cannot pass through the digital filter, the RMS noise (i.e. the RMS sum of the noise in those frequency bins that can pass) is reduced.

This technique of spreading the noise over a wide frequency range and then filtering out most of the noise is how a delta sigma converter achieves a wide dynamic range from a low ADC.

Oversampling and Signal to Noise

- **Oversampling improves SNR**
 - Each oversample by a factor of 4 gives a 6 dB i.e. 1-bit improvement in SNR
- **For a 1-bit ADC and oversampling there are:**
 - 2-bits for 4 x oversampling(4^1)
 - 3-bits for 16 x oversampling(4^2)
 - 4-bits for 64 x oversampling(4^3)
 -
 -
 - 24-bits for 4^{23} x oversampling !!!!!
- **Clearly 24-bits from a 1-bit ADC is not realizable just by oversampling**

1.10



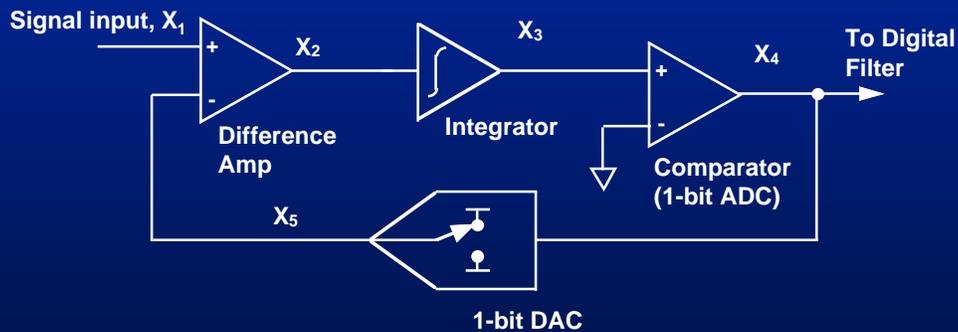
Just how much can be gained by oversampling and then filtering alone? Each oversample by a factor of 4 increases the SNR by 6dB, where $SNR = 6.02N + 1.76dB$. Put another way, each 6dB increase in DR is equivalent to gaining 1-bit in . Hence each time we oversample by 4 times we gain 1-bit of .

Using a 1-bit ADC and oversampling by 4 times, 2-bits of can be achieved. Oversampling by 16 times achieves 3-bits, by 64 times achieves 4-bits, etc.. To achieve 24-bits of from a 1-bit ADC by oversampling alone would require an oversampling ration of 4^{23} times. Clearly not a practical idea.

Delta-sigma ADCs overcome this limitation by using the technique of noise shaping to gain more than 6dB of DR for each factor of 4 times oversampling as will be shown in the next few slides.

Before the subject of oversampling is left, it is appropriate to point out that any ADC can be improved by oversampling and filtering, the simplest filter being averaging. If a little noise is added to the input of a 12-bit ADC and for each reading point an average of 4 readings are taken, 13-bits of will be achieved. Averaging 64 readings will achieve a of 16-bits. Indeed, 16-bit ADCs are limited by internal noise and rarely achieve 16-bits of effective . If 16-bits of is required, then averaging multiple readings can be used to achieve this.

The Delta Sigma Modulator



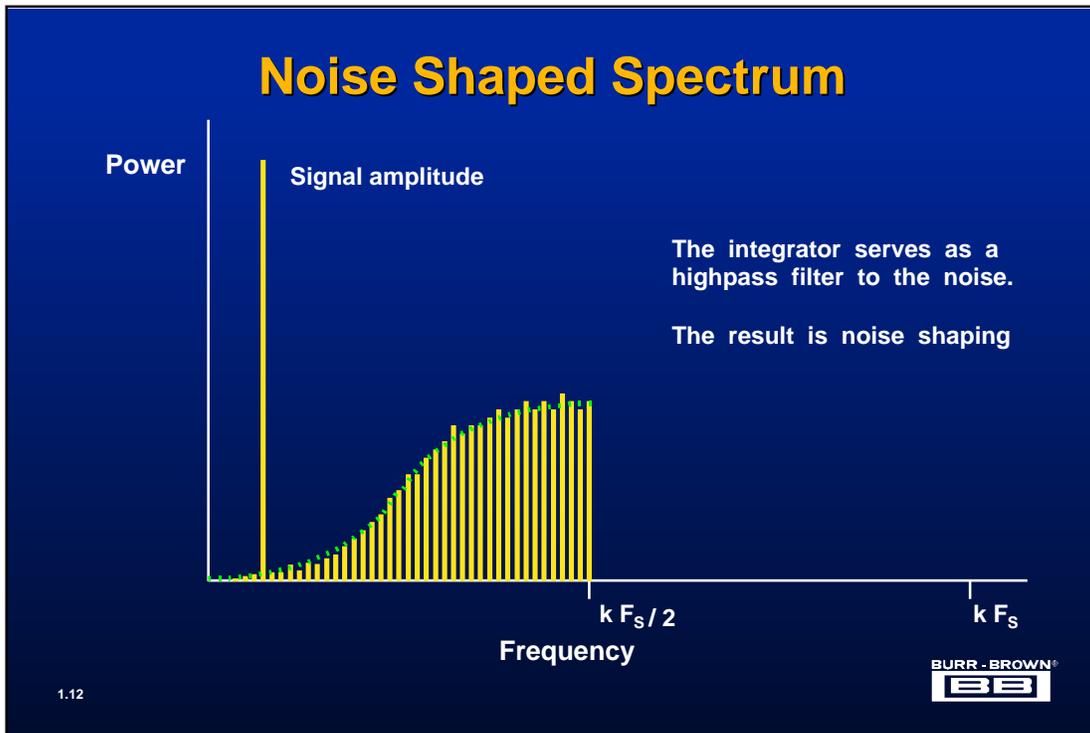
1.11

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The block diagram of the part of the a delta sigma ADC that proceeds the digital filter is shown here. This section is commonly know as the delta sigma modulator.

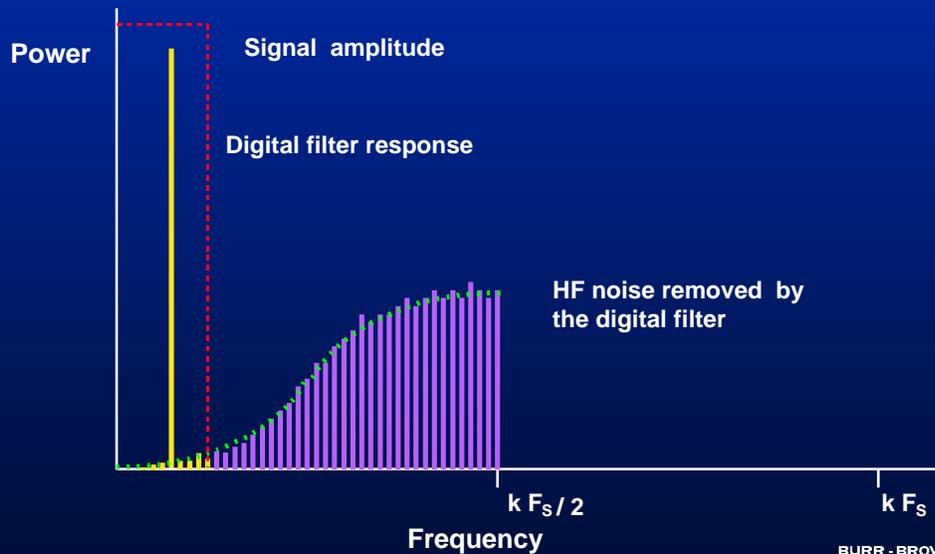
The key to the delta sigma modulator is the integrator. At each conversion, the integrator keeps a running total of its previous output and its current input. The output from the integrator is feed to a 1-bit ADC. This is simply a comparator with its reference input at a level of half the input range. Since in this case the comparator reference is 0V, this ADC will have a bipolar input range. The ADC output feeds a 1-bit DAC which has output levels equal to + or - full scale. A difference amp completes the loop by differencing the current input signal and the previous sample DAC output.

The aim of the feedback loop is to try to maintain the average output of the integrator at the comparator reference level, 0V in this case. It is this effect of the integrator in the feedback loop that allows a delta sigma ADC to improve the SNR by more than simply oversampling. The integrator acts as a low pass filter to the input signal and as a high pass filter to the quantization noise. Consequently, most of the quantization noise is pushed into the higher frequencies.



The affect of the integrator in the delta sigma modulator is shown here. The noise spectrum can be seen to rise as the frequency increases. Note that the total noise power i.e. the RMS sum of all the frequency bins has not changed. There is no less total noise than in the case of simply oversampling but the distribution of the noise has changed.

Filtering the Shaped Noise

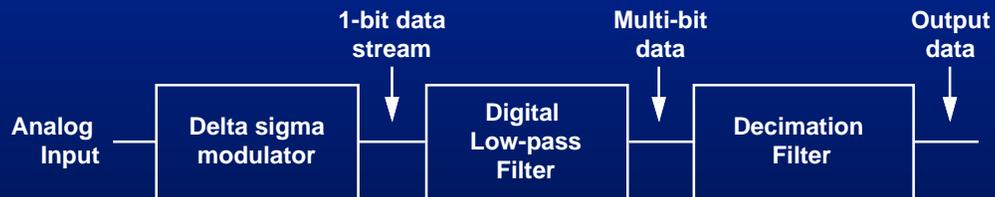


1.13



A digital filter is now applied to the noise shaped delta sigma modulator, more noise is removed than in the simple oversampling case. The delta sigma modulator just described is a first order system and gives a 9dB improvement in SNR for every doubling in sample rate. Compare this with a mere 3dB achieved by oversampling alone. Using this architecture it is now possible to implement a high ADC from a single bit delta sigma modulator with a practical oversampling ratio.

The Digital Filter

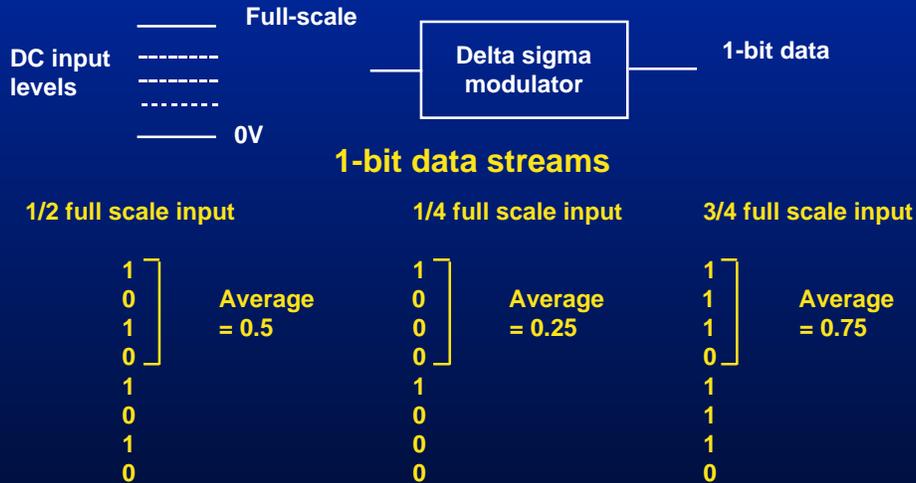


1.14



So far the discussion has concentrated on the role of the delta sigma modulator. The output from this is a rather meaningless one-bit data stream at the sampling rate which may be in the MHz. The object of the digital filter and decimation filter is to extract the meaningful information from this data stream and to reduce the data rate to a more useful value.

Averaging Filters

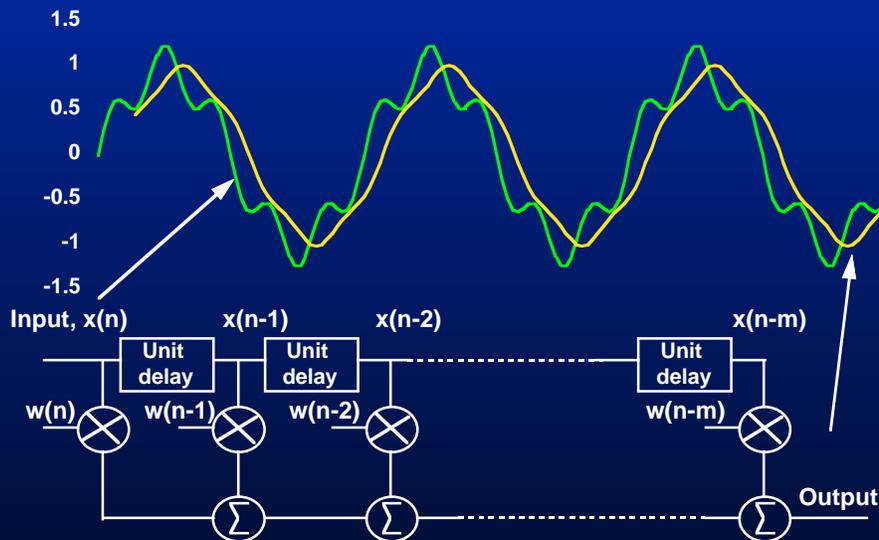


1.15



In order to see the action of the digital filter, first consider the case of a DC input level. The slide shows the values present on the one-bit data stream for three values of the input level. As is clearly shown, the average value of the 1-bit data represents the value of the input signal. In this case 4 samples of the 1-bit data were averaged but in fact any number of samples could equally well have been chosen. The more samples over which the average is taken the greater will be the accuracy of the result. In practice the filter used in a delta sigma ADC is derived from a rolling average filter.

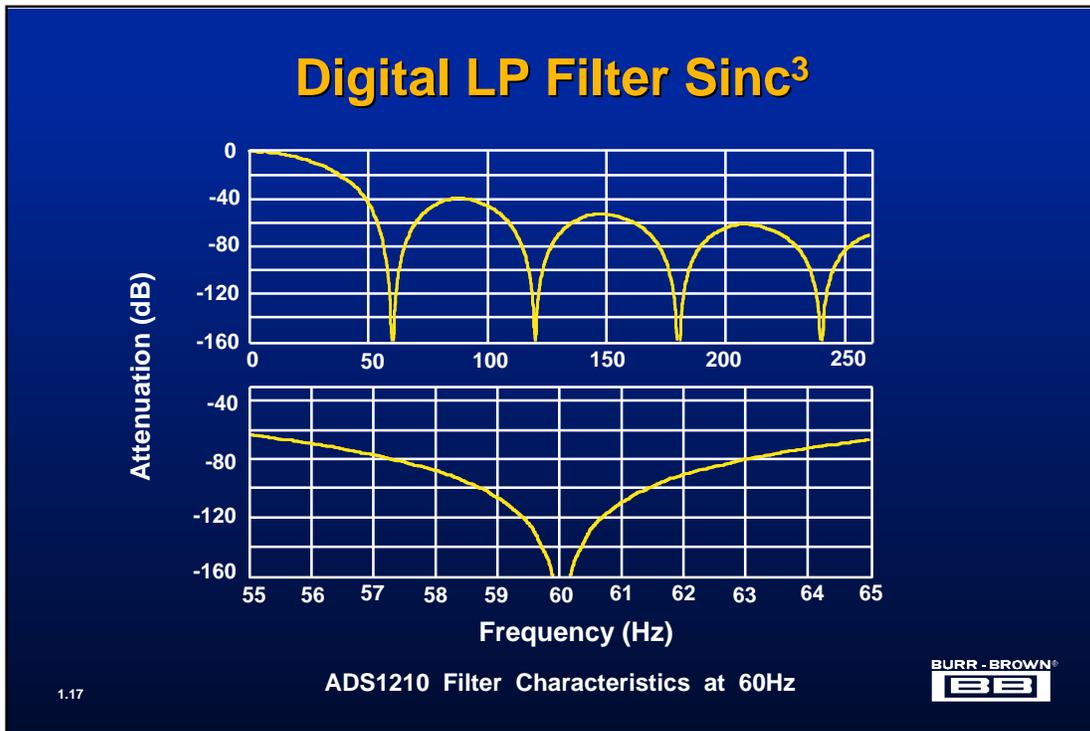
Digital LP (FIR) Filter



A rolling average filter is an example of a Finite Impulse Response (FIR) filter. A method of implementing such a filter is shown in this slide. The filter output is the weighted sum of the current sample and m preceding samples. A weighting factor, $w(n)$ is applied to each individual sample.

In the wave forms shown in this slide, the input waveform is a sine wave with a high order harmonic content. The output waveform was generated from a simple rolling average of 8 samples, each with a weighting factor of one. This example clearly shows the action of a rolling average as a low pass filter. The high order harmonic content has largely been removed while the fundamental is mainly unchanged.

The digital filters used in delta sigma ADCs are considerably more complex than the filter described above but are based on the same principles.

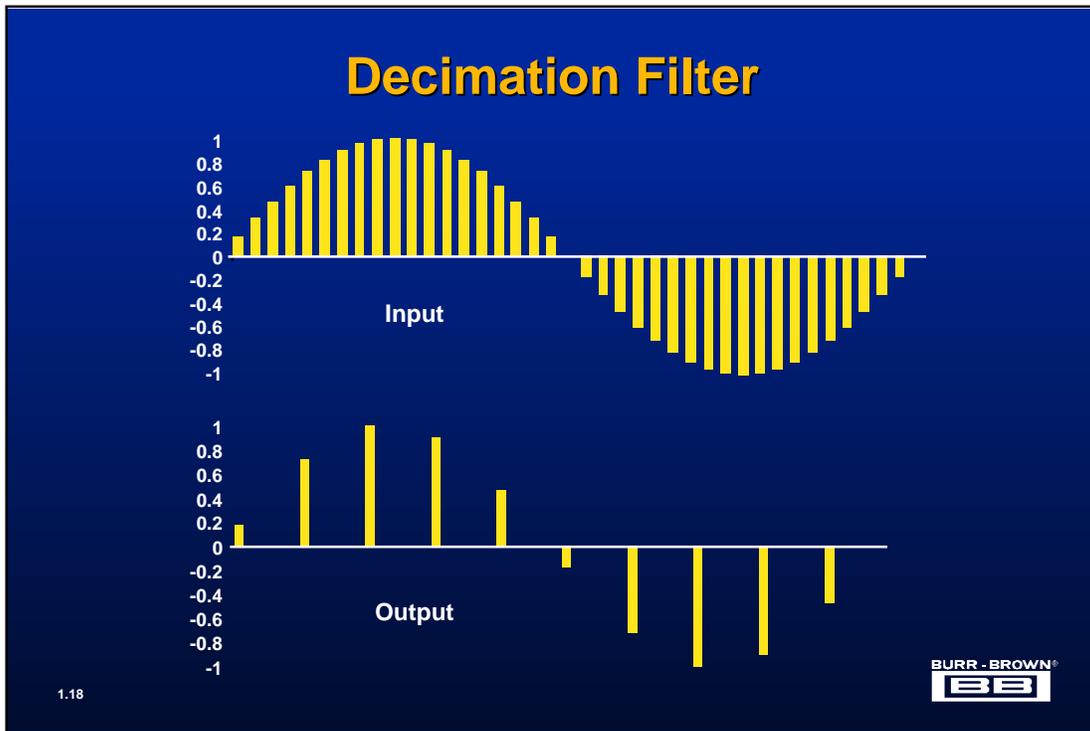


Another filter topology that is widely used in $\Delta\Sigma$ converters in the Sinc³ device. This filter is similar to the FIR topology in that it performs the low-pass function, but its overall frequency response is much different.

The main advantage of this filter over an equivalent FIR is the notch width, shown above centered at 60Hz, is much wider. This allows this filter to reject frequencies that are close to the desired rejection frequency. For instance for the above example the desired rejection frequency is that of line power. If, as is often the case, the line frequency is not exactly 60Hz, this filter would also reject these non-ideal line frequencies.

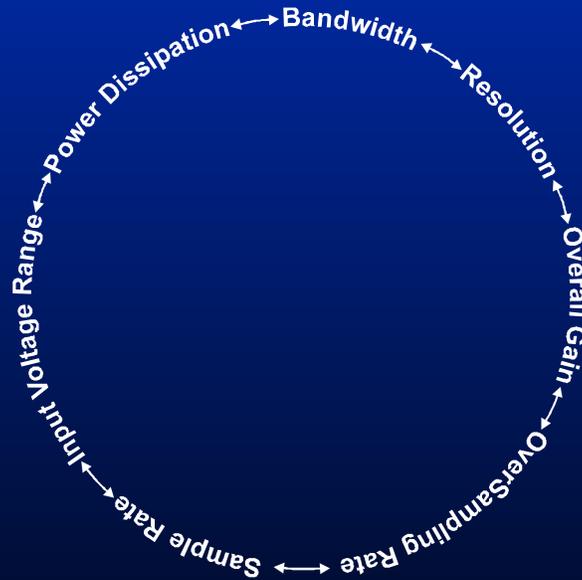
The disadvantage of this topology over the FIR is that its response also has bumps or regions that do not reject or filter signals as well as the FIR.

The FIR has a frequency characteristic that resembles an analog low pass filter. The filter has a passband, a transition region, and finite rejection attenuation.



The role of the decimation filter is to reduce the data rate from the digital filter to a more useful value. It achieves this by only taking certain input samples and discarding the rest. In this case the decimation ratio is 4, so every 4th input sample is retained and the remainder discarded. In practice, the roles of the decimation filter and LF filters are combined

$\Delta\Sigma$ Converter Tradeoffs - Design Cycle

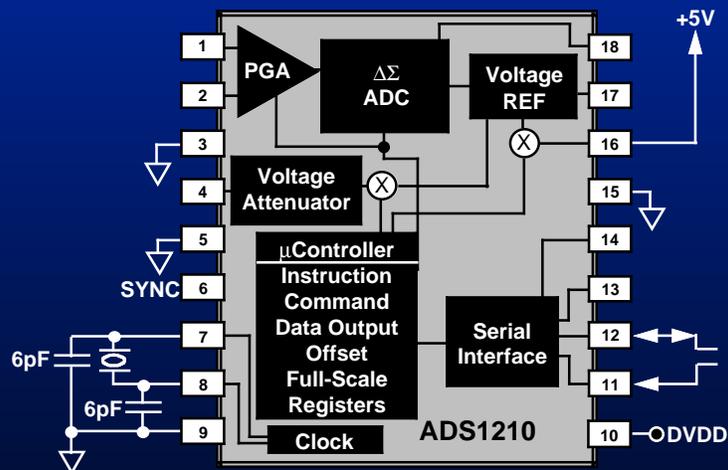


1.19



All of these performance criteria are interrelated. It is impossible to choose one parameter without affecting the possible choices of the others. While it is not possible to predict a design path or flow chart for all applications some general rules are applicable when one parameter is key to a design. For instance, when effective or bandwidth is maximized, power dissipation is increased. When the input voltage range is maximized, the allowable internal gain is decreased. Or when internal gain is increased, the effective is decreased.

$\Delta\Sigma$ Converters ADS1210 and ADS1211

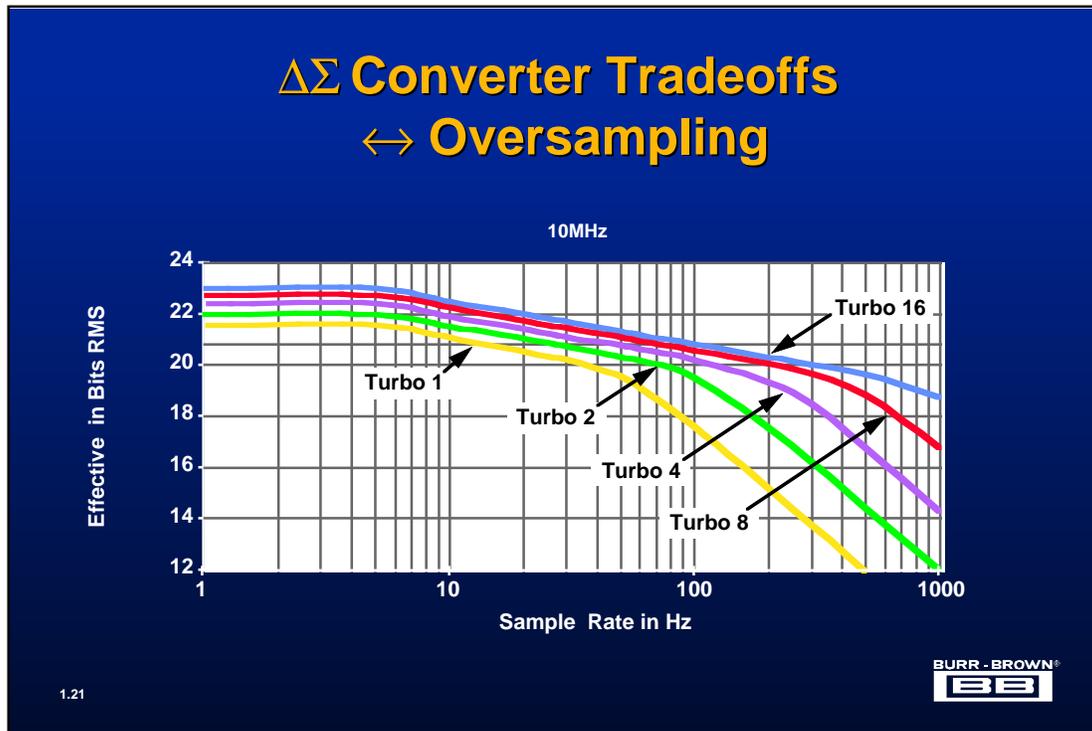


1.20

In the following section the various tradeoffs will be examined in a numerical manner. The data converter used for this examination will be the single channel ADS1210 and the four channel ADS1211. These two data converters differ only by the inclusion of a four channel multiplexer in the ADS1211.

These converters are more correctly defined as a data acquisition system due to the integration of a reference, interface logic, a programmable data converter, programmable gain amplifier (PGA), and other useful sub-circuits. This converter can be calibrated for both offset and gain. The analog functions can also be controlled using the serial interface which controls all functions of the converter.

$\Delta\Sigma$ Converter Tradeoffs ↔ Oversampling



The above diagram illustrates the Effective Number of Bits or ENOB available from either the ADS1210 or the ADS1211 for any given turbo mode. The turbo mode settings are simply another way of saying oversampling rate. The effective of the converter, i.e. the number of bits from the 24-bit stream that can be believed, can be increased if the input voltage is sampled more than once. This technique is commonly referred to as oversampling and will be discussed in greater detail later on.

The price to be paid for oversampling a signal is conversion time and or converter power dissipation. In the case of the ADS1210/11 using the turbo mode to oversample by a factor of two does not by definition double the conversion time. Rather the digital filter used to average the digital equivalent of the data word is run at a higher or faster rate. The effect on the converter is an increase in power dissipation.

$\Delta\Sigma$ Converter Tradeoffs ↔ Oversampling

Sample Rate	Turbo 2	Turbo 4	Turbo 8	Turbo 16
5Hz	23	23	23	23
10Hz	22	23	23	23
20Hz	21	22	22	23
40Hz	21	22	22	23
50Hz	21	21	21	22
60Hz	21	21	21	21
100Hz	20	21	21	21
250Hz	17	19	20	21
500Hz	15	17	19	20
1000Hz	12	15	17	20
2000Hz	10	12	14	16
4000Hz	-	-	14	14
6000Hz	-	-	12	12
10000Hz	-	-	-	10

1.22



Using a higher sampling rate can also increase the ENOB parameter. The above diagram illustrates the ENOB versus sample rate in a tabular form.

Using the previous design parameter of sample rate equaling 10Hz and 22-bits of we can see how this can be increased to 23-bits if a turbo mode of 2 is used.

$\Delta\Sigma$ Data Converter Tradeoffs Gain \leftrightarrow Turbo Mode

<u>Turbo Mode Rate</u>	<u>Allowable PGA Gain Ranges</u>
1 (normal mode)	1, 2, 4, 8, 16
2	1, 2, 4, 8
4	1, 2, 4
8	1, 2
16	1

1.23

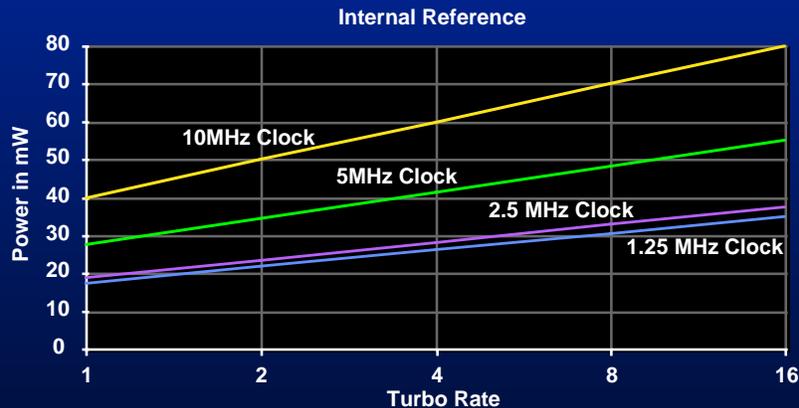


The accuracy of the ADS1210/11 converter family can be improved if the turbo mode is used to oversample the input waveform. When this turbo mode is used the gain setting of the built-in PGA (Programmable Gain Amplifier) must be considered.

The simple rule to remember about this converter family is that the product of the turbo mode times the PGA gain must always be less than 16 or equal to 16.

$$\text{TurboMode} \cdot \text{PGA gain} \leq 16$$

$\Delta\Sigma$ Converter Tradeoffs Power Dissipation \leftrightarrow Turbo Mode



1.24



This diagram illustrates the amount of extra power dissipation that is required if the turbo rate is used. If power consideration is a design concern then the amount of power that can be allowed in the data converter should be selected first. This decision will in turn determine the maximum turbo or oversampling mode. Once the maximum turbo rate is known then the allowable gains for the PGA is determined. Once again the desired accuracy is selected and then PGA gain is selected. This selection will determine whether or not an external amplifier is necessary.

The maximum input voltage range of the converter should always be used. That is the overall analog gain of both the internal PGA and the external INA, if one is necessary, should be selected such that the maximum differential input voltage is gained up to a value that equals the maximum input voltage range of the data converter.

In the case of the ADS1210/11 this range is 5V. As an example, if a maximum differential voltage 100mV is output by the sensor device, an overall gain of 50 should be used. In this case, an external Instrumentation Amplifier should be used in series with the ADS1210 or ADS1211 converter. This overall gain can then be divided between the internal and external gain stages.

$\Delta\Sigma$ Converter Tradeoffs ↔ Sample Rate Turbo Mode = 1

A/D Converter Sample Rate	Output -3dB Frequency	PGA G = 1	PGA G = 2	PGA G = 4	PGA G = 8	PGA G = 16
10	2.62Hz	22	22	22	22	21
25	6.55Hz	21	21	21	21	21
30	7.86Hz	21	21	21	21	21
50	13.1Hz	20	20	20	20	20
60	15.72Hz	20	20	20	20	20
100	26.2Hz	18	18	18	18	18
250	65.5Hz	15	15	15	15	15
500	131Hz	12	12	12	12	12
1000	262Hz	10	10	10	10	10

1.25

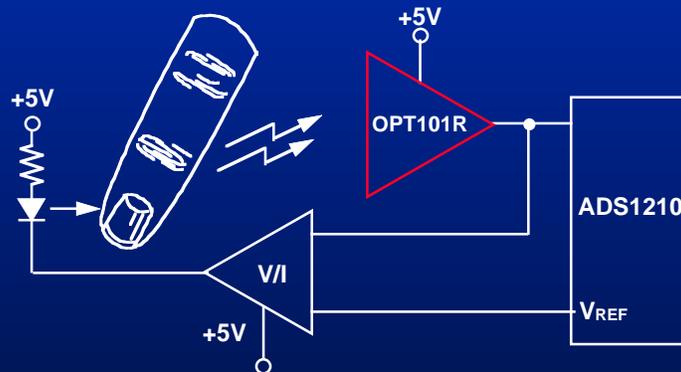


The above chart illustrates the effective or the ENOB of the ADS1210/11 converter for different sample rates and gains. The trade offs that one makes for different sample rates also depends on the gain of the PGA.

Recall that previously the use of an external instrumentation amplifier was discussed for use with a data converter. In that application example it was mentioned that there is a tradeoff made for using higher gains with the internal PGA.

As can be seen from the above diagram the best is obtained when the gain is the lowest or 1V/V. As a general design rule, the of the converter must first be determined. Once this is established, the maximum usable gain of the PGA can be determined. For instance, if a sample frequency of 10Hz is used and a of 22-bits is desired then the maximum gain that can be used is 8.

Heart Rate



- Uses a single color light source
- Uses a photodiode and amplifier
- Heart rate determined by the time between adjacent pulses

1.26



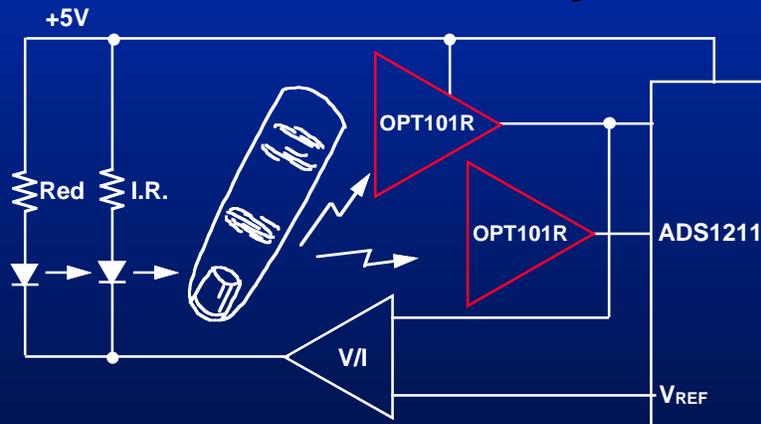
The above diagram shows one way to extract the heart rate of a human based on the changing attenuation of infrared light shown through the subjects finger.

The circuit operates on a single +5V supply, uses an infrared LED as the emitter, an OPT101R as the receiving device, and the ADS1210 as the data converter.

Infrared light is used so that the device can be operated in an ambient lighted room. The OPT101R is an integrated photodiode and transimpedance amplifier housed in a red plastic package. This OPT is used because it can operate from a single supply and the red package filters most of the ambient light. Finally the ADS1210 is used because it is accurate and also operates from a single 5V supply.

The amount of drive current depends on the size of the human finger but generally 20mA of current will produce the desired response. Ideally the steady state voltage from the OPT101R will be 2.5V which is in the middle of the ADS1210's common mode range. The servo loop formed by the amplifier and reference performs this function.

Blood Oximetry



- Uses differential light measurement
- Typically a red and infrared diode as emitter
- Photodiode measures the response

1.27



Blood Oximetry or the measurement of the oxygen content in the blood, is also a photodiode application. Unlike the measurement of heart rate two different light spectrums are of interest. Usually a red LED and an infrared LED are used. The difference between the two responses are used to calculate the amount of oxygen in the blood. Since the heart rate information is also available this rate is usually calculated as well.

Wide-Range DVM



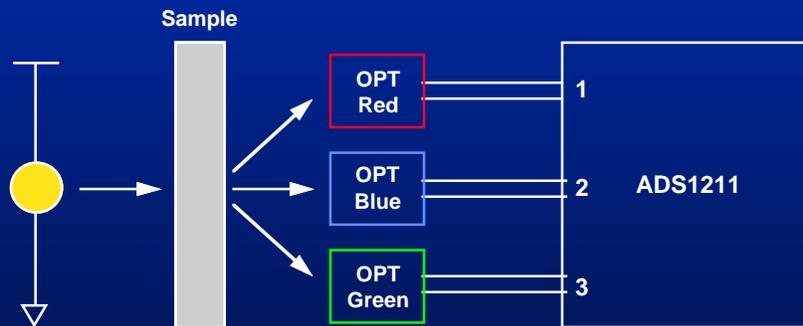
- Relies on the wide > 140 dB dynamic range of a A/D converter
- Requires a oversampling $\Delta\Sigma$ converter
- Bandwidth to 5 kHz
- Accuracy is traded for input frequency range

1.28



The 24-bit ADS1210 is an ideal choice for a wide input range volt meter. Using the internal 2.5V reference allows for an LSB size down to 300nV. This is because the effective of the ADS1210 is 23-bits when operated in the turbo 16 mode for sample rates up to 40Hz. Thus even with a safety factor or design margin of 10 is used, amplitudes as small as 3 μ V can be successfully captured using this converter. Note that no external signal conditioning hardware, beyond the required Nyquist filter, is requires to build a DC volt meter that has 120dB of dynamic range. Beyond measuring DC voltage this circuit is also useful for measuring the low frequency noise, such as from an op-amp.

3-Color Separation



- Uses three light to voltage converters
- Also uses colored filters
- Data is collected in a three channel A/D converter

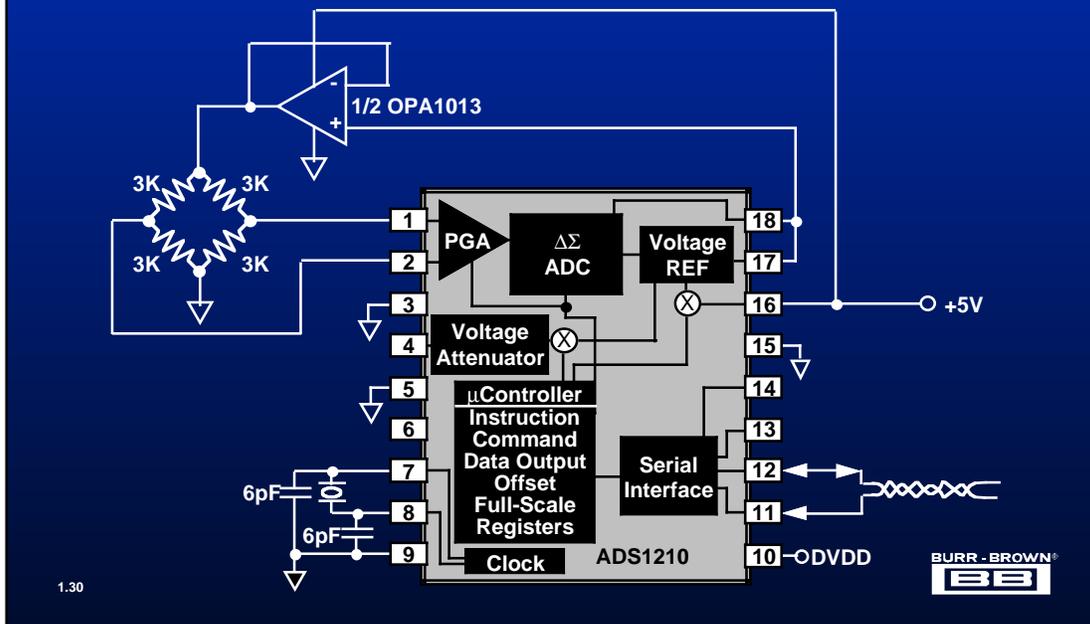
1.29



The above circuit shows a technique for extracting the color components from a sample. The devices used to convert the light samples into voltage are again the OPT products. Each of the three sampling OPTs are fitted with a narrow band optical filter. Each OPT then produces an output which is proportional to the color of the filter.

If for example we were to use a typical computer screen for a PC as the reconstruction device then only 8-bits of are required. Hence although we could use the 24-bit ADS1210 for a lower design choice, the 12-bit ADS7833 could be used. The ADS7833 is not a $\Delta\Sigma$ converter, rather a three channel simultaneously sampling CMOS A/D converter.

$\Delta\Sigma$ Bridge Interface Application Circuit



This slide illustrates a method of connecting the ADS1210 to a bridge circuit. The internal reference of the converter is used to excite the bridge. Since the reference is unable to supply all the current necessary for this bridge, an external buffer amplifier is used as a voltage follower to drive the necessary current to the bridge. This amplifier should be capable of not only supplying the current, but also able to be run from a single supply, i.e. +5V. A good choice for this amplifier would be the OPA1013.

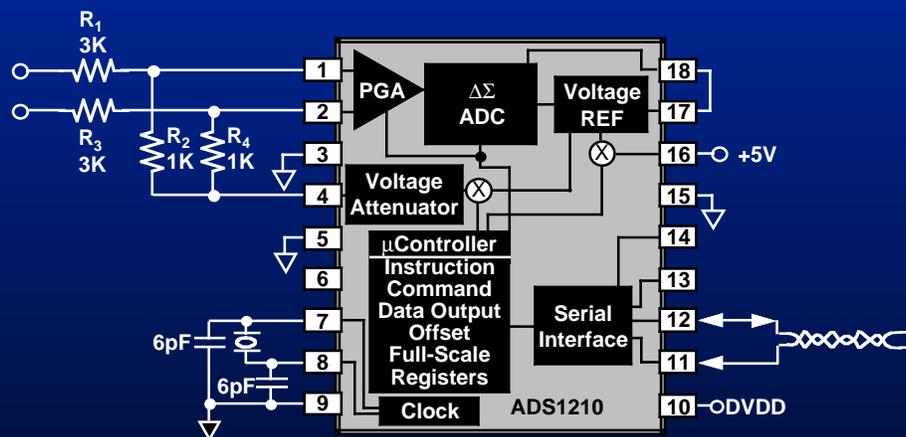
The PGA in the data converter has a compliance and common mode range that includes ground and the data converters supply rail. For this reason no signal conditioning is necessary between the bridge and the PGA.

In this circuit the data converter would be run in the bipolar mode if both stress and strain are applied to the bridge. That is, if the variable element in the bridge can go up and down around its unloaded value.

Since the ADS1210 contains both a full scale and offset register the data converter can accommodate gain and offset errors. The procedure to do this would be as follows:

- 1) With the bridge unloaded calibrate the converter for offset. The converter will store this number in its memory and subtract / add this number from all future measurements.
- 2) Fully load the bridge and perform the system calibration for full scale. This value will also be stored and all further measurements will be referenced to this value.

$\Delta\Sigma$ Differential ± 10 Volt Input Signal Conditioning Application Circuit



1.31

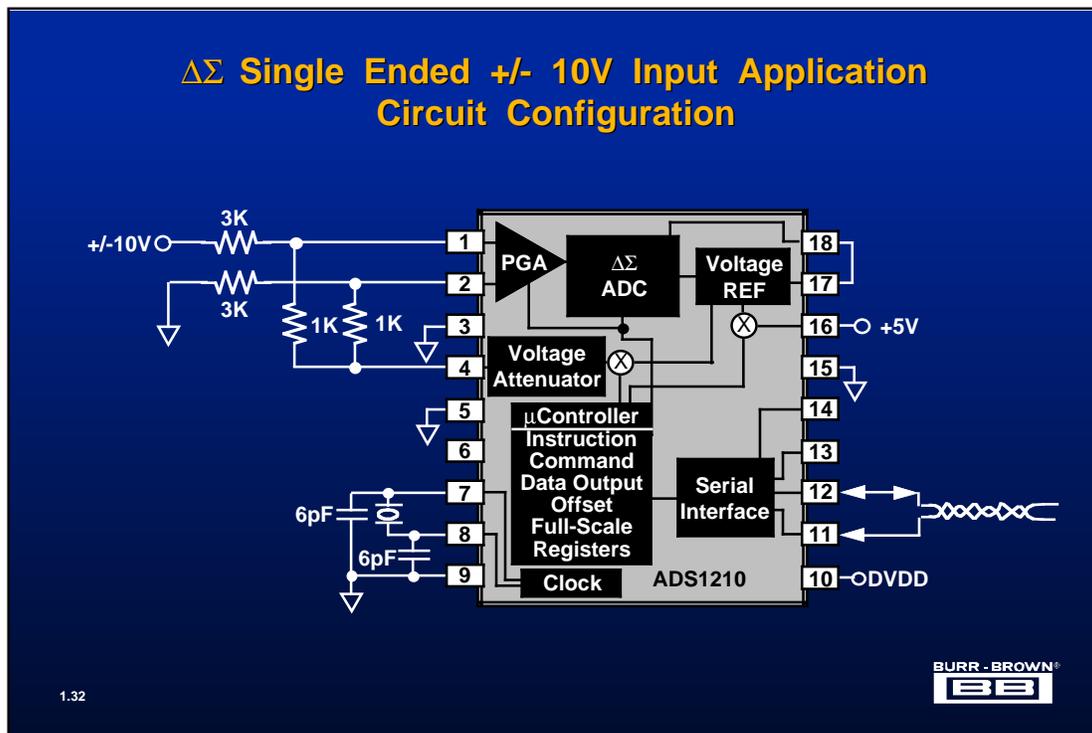
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Even though the input voltage range of the ADS1210 is limited to the range of 0 to +5V this range can be extended to -10 to +10V by using the internal bias voltage of 3.3V. The circuit above shows the connections and resistor values used to accomplish this. When either input is +10V the voltage as seen by the input is divided down to 5V. Conversely when either input is -10V the input as seen by the converter is 0V.

The resistors used in this arrangement must be well matched. The fact that these resistors will not drift at the same rate (since there are two different resistor values) should be remembered.

Since the ADS1210 has the ability to calibrate out an offset value, it is possible to improve the accuracy of this system by performing a system calibration with both inputs grounded. Calibrating for full scale involves applying +10V to the positive input and -10V to the negative input. Once this calibration has been performed there will still be an error if the resistor values are not exact, but the percentage by which the actual output of the data converter differs from the ideal, i.e. exact resistor values, will always be the same percentage. When 1% resistors are used, the maximum amount of offset error at the output of the converter is 0.5%, assuming the A/D converter is ideal. Thus with $R_1=3030\Omega$, $R_2=990\Omega$, $R_3=2970\Omega$, and $R_4=1010\Omega$, the output of the converter will be off by 0.49% from the ideal reading.

ΔΣ Single Ended +/- 10V Input Application Circuit Configuration



Another version of the previous circuit is shown here. In this case a single ended input is measured. Since a differential input is not present the gain of the PGA can be programmed for a gain of two to generate the full scale, 0 to 5V, input voltage range.

This idea brings up another design rule regarding these types of data converters in that the maximum input voltage range decreases as the gain of “PGA” changes. The reason for this is that the PGA is not an amplifier as such. In fact, as the “gain” goes up what is really happening is the reference used by the converter goes down. In the ADS1210 family there are a series of four “taps” for each of the gain settings. In a gain of 1 a voltage level of 2.5V is used, in a gain of 2 the level is 1.25 and so on. The rule to follow is:

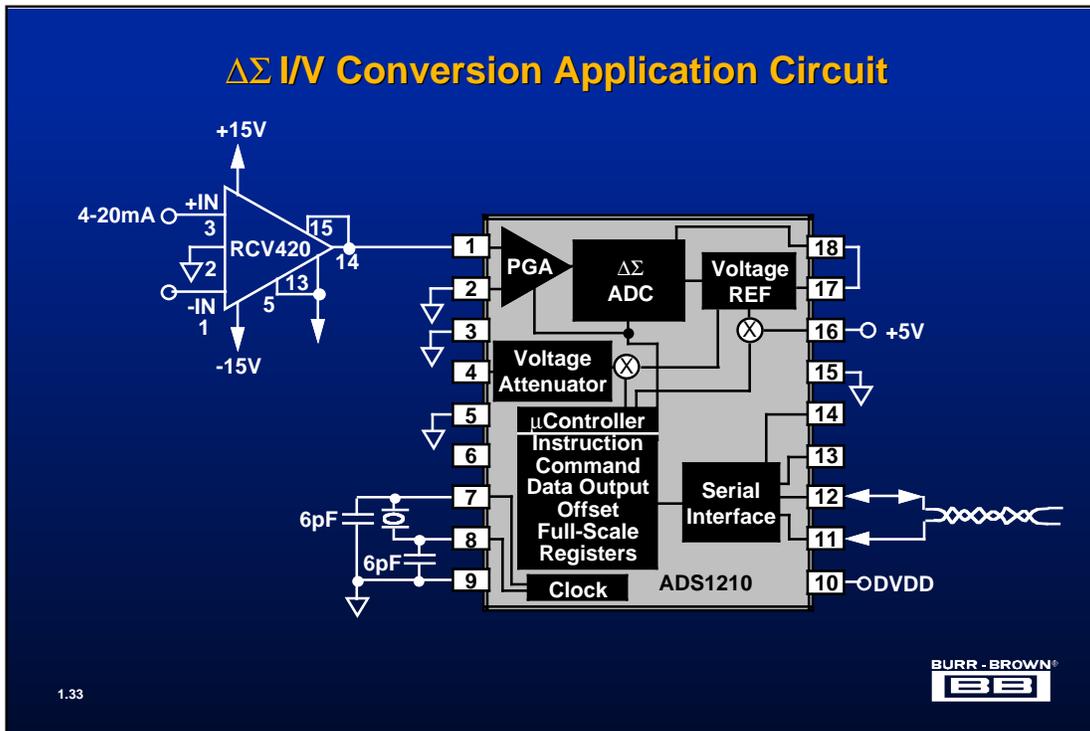
$$V_{IN} (\text{max}) \cdot \text{PGA gain} \leq 5V$$

for no external divider and,

$$\pm V_{IN} (\text{max}) \cdot \text{PGA} \leq \text{gain} \pm 10V$$

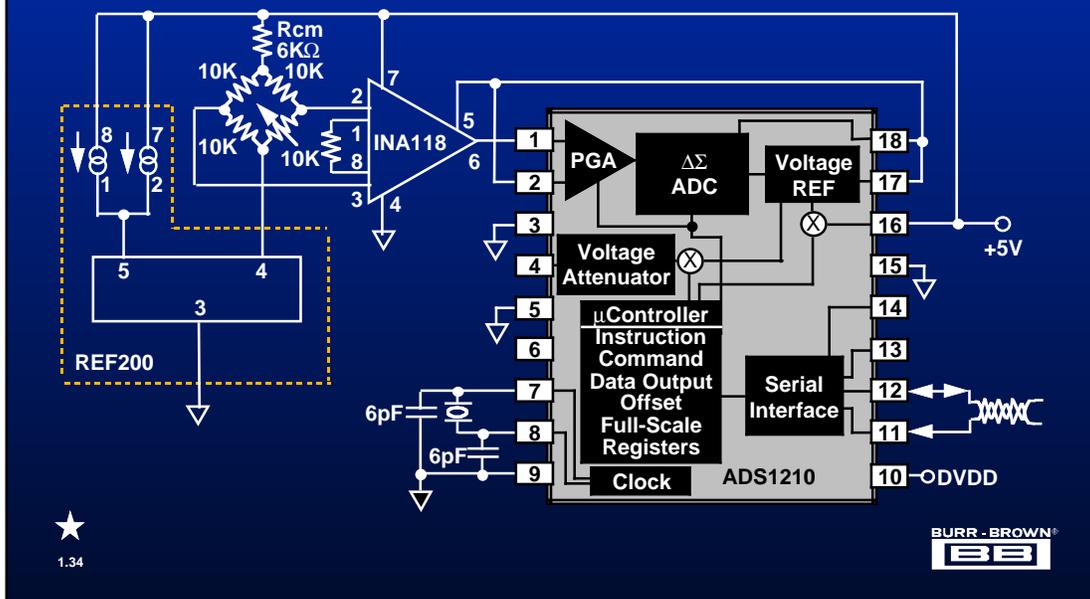
when the external divider is used

$\Delta\Sigma$ I/V Conversion Application Circuit



Converting a current, like that from a 4-20mA loop, into a representative voltage can be done using the ADS1210 together with the RCV420. The RCV420 is an integrated instrumentation amplifier and sense resistor network. The advantage of using this device to convert a current into a voltage instead of just sensing a differential voltage from a resistor lies in the accuracy and features inherent in the integrated device. This circuit provides for adjustment of gain and offset errors as well. The disadvantages of this approach is that the RCV420 requires a bipolar power supply and is of course more expensive than a resistor.

ΔΣ Single Supply, High Accuracy Bridge Transducer Interface with Current Excitation

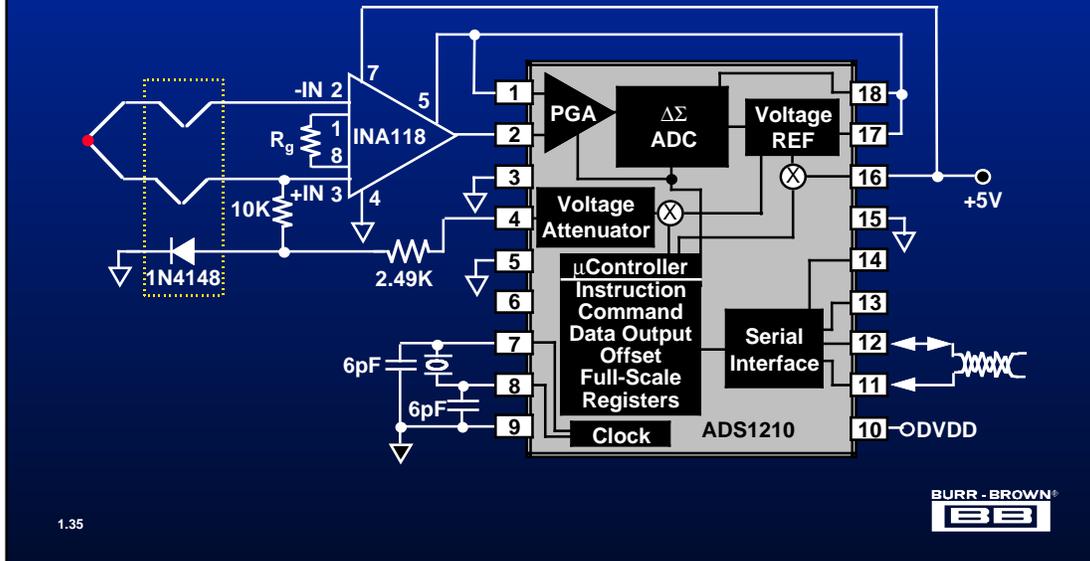


The integrated current source and current mirror device REF200 has many applications in single supply linear circuits including the ability to provide current bias for a bridge.

In the circuit shown above the two 100 μ A current sources are into pin 5 of the REF200 which produces an equivalent current flowing into pin 4. The reason for using the current source in this manner, instead of simply sourcing current into the bridge, is that the current sources themselves have a compliance voltage of 2V whereas the mirror has a compliance of 1.5V. This an additional 10% of supply range for the remaining circuitry.

The resistor R_{CM} is selected, as in the RTD application, to produce a common mode voltage for the INA118 of 2.8V, when the bridge is unloaded. Also the internal 2.5V reference is used as the comparison voltage for both the ADS1210 and the INA118. Again using the reference in this manner removes reference voltage shifts from the measurement and hence increases the overall accuracy of the system.

$\Delta\Sigma$ Single Supply, High Accuracy Thermocouple Interface with Cold Junction Compensation



1.35

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This application circuit illustrates a way to use a $\Delta\Sigma$ analog to digital converter to transform temperature into a digital word. Also this circuit employs cold junction compensation in the form of an isothermal block and the 1N4148 diode. The bias current for the diode is provided by the internal 3.3V bias network from the ADS1211.

Normally the voltage from the diode is divided down with a resistor network to compensate for the Seebeck coefficient of the type of thermocouple being used. In the case of the ADS1211 application, the cold junction temperature can be interpreted by one channel of the converter while another channel is dedicated to the measurement of the environment that the thermocouple is in. Thus via a software calculation or hardware algorithm, the compensation can be done mathematically.

Summary

- $\Delta\Sigma$ Converters are highly integrated
- Good for slowly moving signals
- Large > 20-bit accuracy