Linear Circuits for Digital Systems
Some Affable Analogs for Digital Devotees

Jim Williams

The pristine, regimented symmetry of digital circuit boards is occasionally interrupted by an irregular huddle of linear components. These aberrants are tolerated because they perform a variety of ancillary tasks necessary to keep the digital system running. While I certainly wouldn't wish lifetime employment on a digital circuit board to anyone*, the reality is that the need exists. Power control, clock circuits and memory management are areas where linear circuits are needed in digital systems. Recently introduced flash memories offer a good example of linear circuits supporting a predominantly digital function. Flash memory adds electrical chip-erase and reprogramming to conventional EPROM capability. A full chip erasure takes 1 second with 100µs byte-program times and 4 seconds for full chip programming. These features make flash memories an attractive non-volatile memory option. Additional information on these devices appears in Appendix A, "A Primer on Flash Memory," guest written by Saul Zales of Intel Corporation.

These devices require carefully controlled, high voltage programming power. A typical unit, the Intel 28F010 1 megabit flash memory, specifies V_{PP} ($V_{PROGRAM\ POWER}$) pulses of 12V ± 0.6V or 12.75V ± 0.2V, depending on part type. V_{PP} excursions beyond 14V (for 20ns or longer) will destroy the ETOX† process based device. Reliably generating such pulses in a 5V powered digital system involves several analog issues. High voltage must be derived and controlled within the tight tolerances noted (see Appendix B for an expanded discussion of this topic). Additionally, it is desirable to control the high voltage pulses from a 5V logic command.

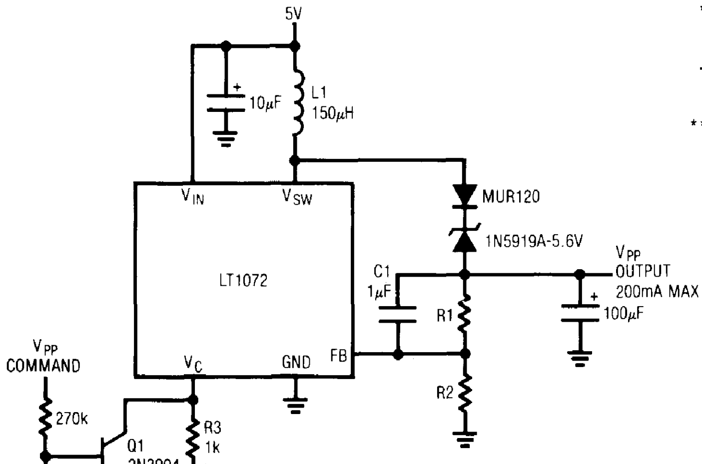
Basic Flash Memory Programming Voltage Supply

Figure 1's circuit meets almost all flash memory V_{PP} requirements. When the V_{PP} command goes low (Trace A, Figure 2) the LT1072** switching regulator drives L1, producing high voltage. DC feedback occurs via R1 and R2,

*I suppose it's not all that bad. Some of my best friends are digital circuits. If I had a daughter, I'd even consider letting her go out with one.

†ETOX is a trademark of Intel Corporation.

**See Appendix C and References for detailed information on the LT1072.



V_{PP} OUT	R1	R2	RESISTOR TOLERANCE
12.0V	10.7k	1.24k	1%
12.75V	11.5k	1.24k	0.1%

Figure 1. Basic Flash Memory V_{PP} Programming Voltage Supply

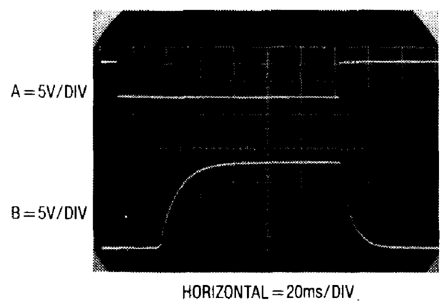


Figure 2. Waveforms for Basic Flash Programming Supply

V_{PP} Handshake Circuit

Both V_{PP} circuits shown require a small waiting period for the regulator to settle before proceeding with a V_{PP} operation. In almost all circumstances this is acceptable, but some situations may require verification that V_{PP} is within tolerance before pulsing begins. Figure 8's circuit, used in conjunction with either V_{PP} circuit, gives a handshake output when V_{PP} has settled. This simple circuit works by comparing the V_{PP} output against the known LT1004 reference voltage. The resistor values given allow for possible variations in V_{PP} voltage due to component tolerance stack-up. When this circuit is in use, the output of the V_{PP} generator circuit should be set within 0.4% of nominal value. This can be done by trimming, or using 0.05% resistors in place of the 0.1% units specified.

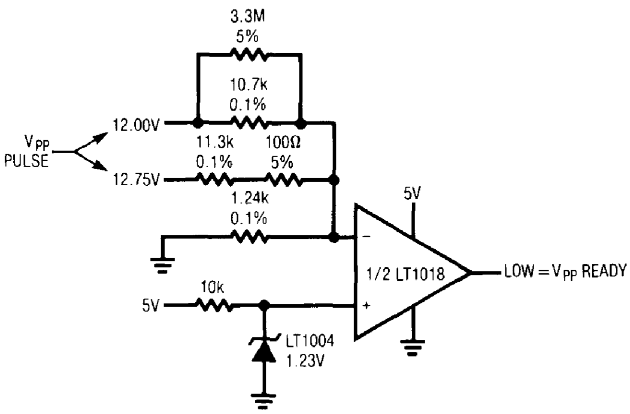


Figure 8. V_{PP} Handshake Circuit

EEPROM V_{PP} Pulse Generator

EEPROMs do not offer the advantages of flash memories, but are sometimes used. Their V_{PP} pulse requirements have commonalities with flash types. The 2816 specifies 21V ± 1V V_{PP} amplitude with a maximum allowable voltage of 22.5. A special EEPROM stipulation is that the V_{PP} pulse must have a 600μs rise time. Figure 9's circuit meets these requirements. The LT1072 generates the high voltage while A1 and A2 form the actual V_{PP} pulse. With the Erase/Write lock line low (Trace A, Figure 10), the LT1072 is in standby; no high voltage is produced and there is no circuit activity. Under these conditions the V_{PP} output line is pulled towards +5V via the 1N914 diode (see 2816 data-sheet for details). When the Erase/Write lock line (Trace A, Figure 10) goes high, the regulator output (Trace C) builds smoothly and regulates at 25V. The 2 pole LT1072 compensation allows the regulator output to rise relatively quickly. When the V_{PP} command line (Trace B) is pulsed high, the LT1004 reference clamps at 1.23V and the RC network delivers a 600μs edge to A1's input. A1 combines with power buffer A2 and the feedback resistors to produce a 21V pulse at the V_{PP} output (Trace D). Trace E is a time and amplitude expanded version of this pulse. The 600μs RC rise time condition is met, with the 21V amplitude assured by the LT1004 reference and closed loop operation. When the V_{PP} command goes low, the V_{PP} output returns cleanly to 4.5 V. The diode path speeds recovery of the 0.005μF capacitor at A1's input. A2 provides a 150mA (ten 2816 EEPROMs) output with short circuit protection. As in Figure 4, a diode path around the LT1010 prevents overshoot when the circuit is recovering from output shorts. When the Erase/Write lock line returns low, the regulator output decays towards zero. As with the other V_{PP} circuits, this design does not produce undesired outputs during power-up or down.

5V Powered 4-20mA Current Loop Generator

Figure 11's circuit also employs voltage step-up, but for a different purpose. Transmission of industry standard 4-20mA current loop signals to valves and other actuators is a common requirement. Resistive line losses and actuator impedances require current transmitters to be able to force a compliance voltage of at least 20V. Because of this, 5V powered systems usually cannot meet current loop transmitter requirements, but Figure 11 shows a way to do this. This 5V powered circuit utilizes a servo controlled DC-DC converter to generate the compliance voltage necessary for loop current requirements. It will drive 4-20mA into loads as high as 2200Ω (44V compliance) and is inherently short circuit protected. Its digital inputs permit easy interface to digital systems.

As in Figure 1, spurious V_{PP} outputs are suppressed during power-up or down. The LT1010 provides 150mA drive (5 28F010's) and short circuit protection. The diode path around the LT1010 prevents destructive overshoot when the circuit is recovering from output shorts. The diode at A1's input clips excessive negative voltages due to the 680pF unit's differentiated response. Figure 7's circuit is similar to Figure 4's, except that the LT1010 has been replaced with a discrete power output stage, Q2-Q3. Q3 furnishes up to 800mA (26 28F010 memories), with Q2 used for current limiting. The feedback values have been increased, preventing Q2's collector current from causing excessive heating in the grounded resistor. This could occur during prolonged short circuit conditons. The feedback capacitor is re-established accordingly. The circuit's AC dynamics, including a glitchless short circuit recovery, are identical to Figure 4.

In some systems high voltage is already available. In such cases the LT1070/72 circuitry may be deleted from Figures 4 and 7.

A good question might be: "Why not set the switching regulator output voltage at the desired V_{PP} level and use a simple low resistance FET or bipolar switch?". In theory, this approach will work. In practice, transmission line effects in printed circuit trace runs may cause memory destroying overshoots. Appendix B, "Preventing Memory Destruction," details this phenomenon.

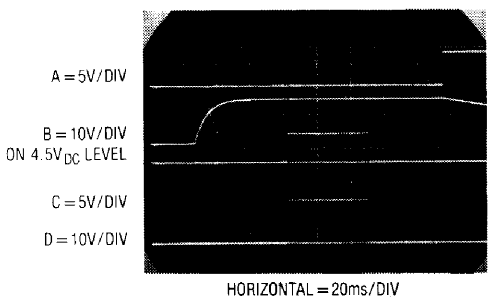


Figure 5. Operating Details of High Repetition Rate Flash Memory Programming Supply

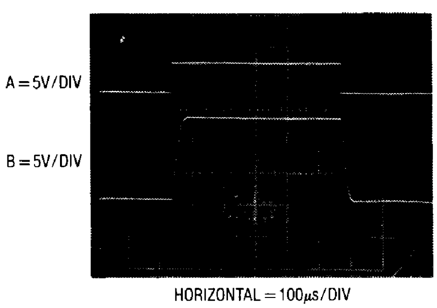
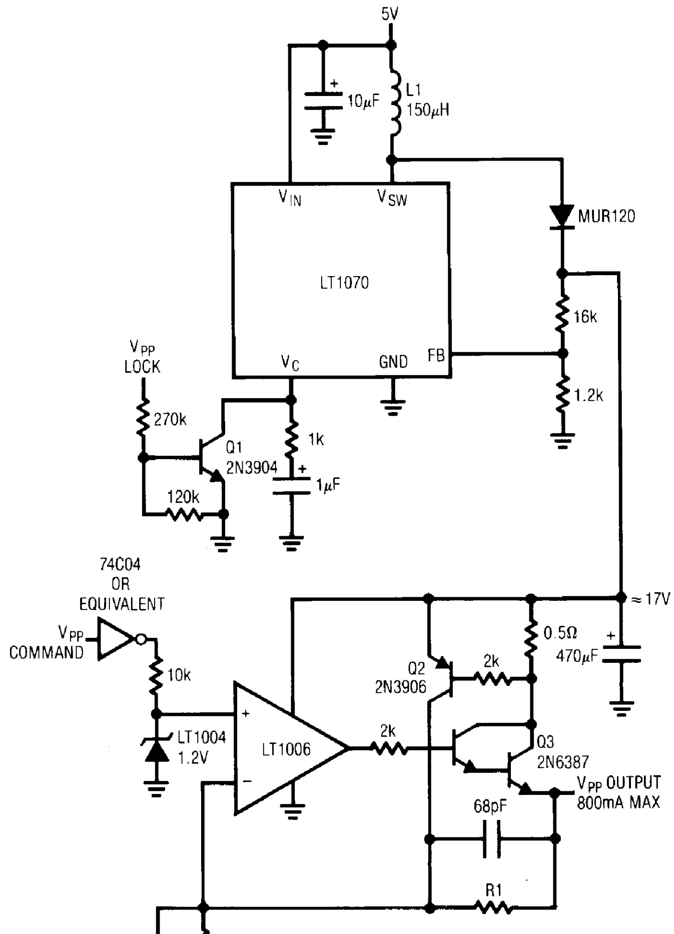


Figure 6. Expanded Scale Display of Figure 4's V_{PP} Output. Controlled Rise Time Eliminates Overshoots



V_{PP} OUT	R1	R2	RESISTOR TOLERANCE
12.0V	107k	12.4k	1%
12.75V	115k	12.4k	0.1%

Figure 7. High Power, High Repetition Rate V_{PP} Pulse Generator

with AC roll-off controlled by C1 and R3-C2. The result is a smoothly rising V_{PP} (Trace B) which settles to the required value. The specified R1 values allow either 12.0V or 12.75V outputs. The 5.6V zener permits the output to return to 0V when the V_{PP} command goes high. It may be deleted in cases where a 4.5V minimum output is acceptable or desirable (see Intel 28F010 datasheet). Precision resistors combine with the LT1072's tight internal reference to eliminate circuit trimming requirements. Alternately, 1% resistors and a trimmer may be used. Additionally, this circuit will not spuriously overshoot during power-up or down, preventing memory destruction. Figure 3's table details circuit changes permitting higher power outputs. The synchronous switch option can be used to eliminate the zener and its attendant power dissipation.

High Repetition Rate V_{PP} Programming Supplies

Figure 1's repetition rate is limited because the regulator must fully rise and settle for each V_{PP} command. Figure 4's circuit serves special cases which require higher repetition rate. Here, the switching regulator runs continuously, with the V_{PP} generated by the A1-A2 loop. If desired, the V_{PP} lock line can be driven, shutting down the regulator to preclude any possibility of inadvertent V_{PP} outputs. When V_{PP} lock goes low (Trace A, Figure 5) the LT1072 loop comes on (Trace B), stabilizing at about 17V. 2 pole compensation ensures a clean rise time. Pulling the V_{PP} command line low causes the 74C04 (Trace C) to bias the LT1004 reference. The LT1004 clamps at 1.23V with A1 and A2 giving a scaled output (Trace D). The 680pF capacitor controls loop slewing, eliminating overshoots. Figure 6 details the V_{PP} output. Trace A is the 74C04 output, with Trace B showing clean V_{PP} characteristics.

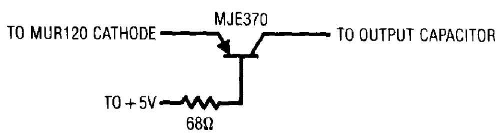
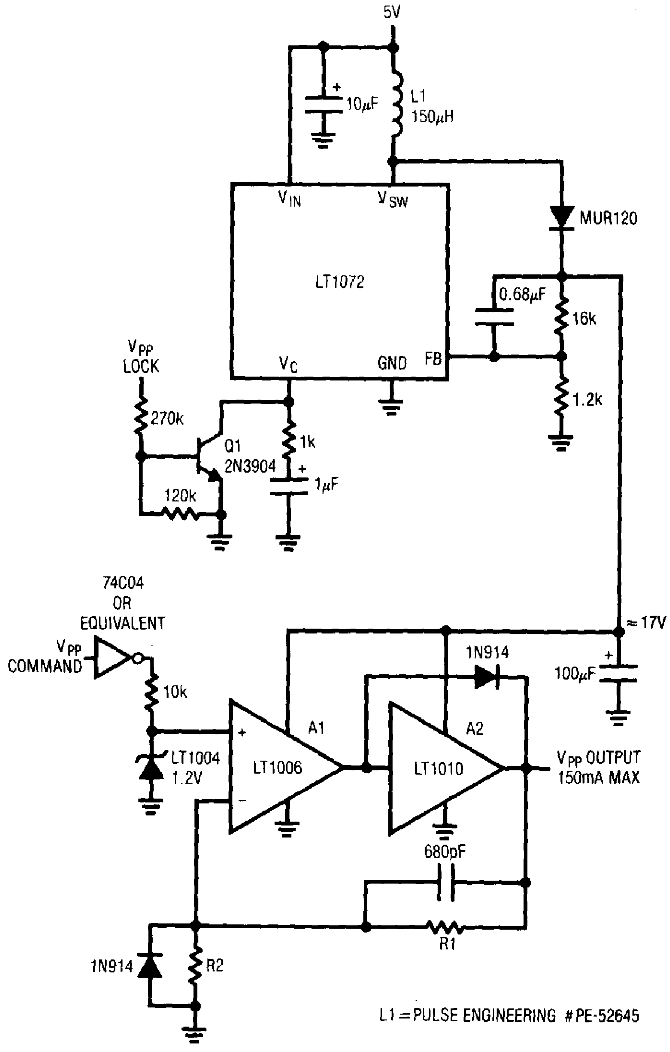


Figure 3. Synchronous Switch Option

Power Options for Basic V_{PP} Pulse Generator

OUTPUT CURRENT	C_{OUT}	REGULATOR	INDUCTOR	ZENER
400mA	200µF	LT1071	PE-52645	1N5339A or Synchronous Switch Option
800mA	400µF	LT1070	PE-51516	1N5339A or Synchronous Switch Option

Note: Assume each 28F010 device requires 30mA of V_{PP} current.



V_{PP} OUT	R1	R2	RESISTOR TOLERANCE
12.0V	10.7k	1.24k	1%
12.75V	11.5k	1.24k	0.1%

Figure 4. High Repetition Rate V_{PP} Programming Supply

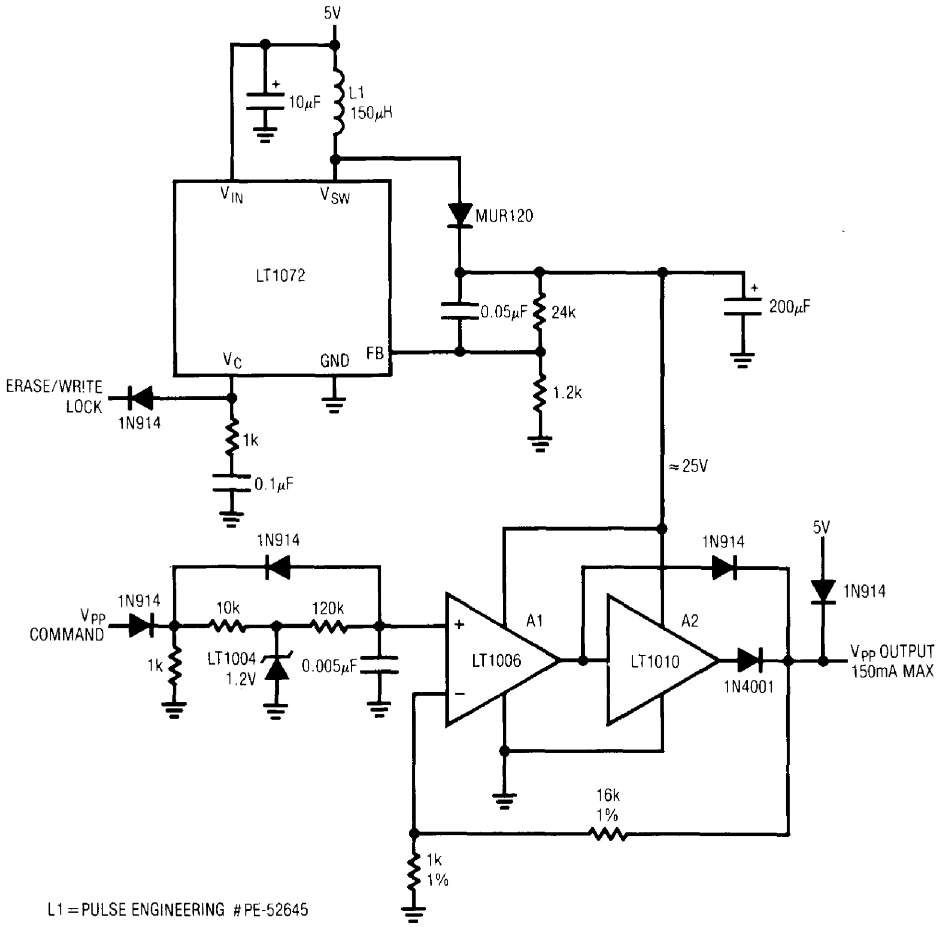


Figure 9. EEPROM V_{PP} Pulse Generator

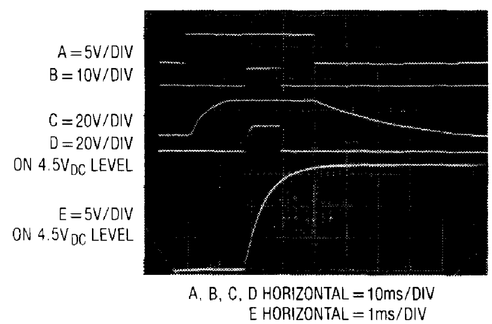


Figure 10. EEPROM Pulse Generator Waveforms

The AD558 8 bit D→A converter receives the circuit's digital inputs, producing a 2.56V full-scale output. A1's positive input voltage is determined by the D→A output and the 4mA trim network output. A1's output biases the LT1072's V_C pin. This forces the switching regulator to run at the output voltage necessary to balance A1's inputs. The feedback path for this action is through the load, across the 75Ω resistor and back to A1's negative input. The 240Ω-0.05μF combination stabilizes the loop. The 7.5V zener permits regulator output down to 0V. The resistors connected to the LT1072's feedback (FB) pin prevent circuit output from running away in the event the load opens up. Normally, A1 controls the loop, forcing the LT1072 to produce the voltage required to maintain the D→A directed current through the load. If the load opens, A1 receives no feedback, but the FB pin becomes active at 1.2V, forcing the loop to close locally around the LT1072. In this fashion the circuit automatically crosses over from a current to a voltage regulator, preventing excessive output voltages from occurring.

Figure 12 details LT1072 operation under normal conditions. Trace A is V_{SWITCH} pin voltage, while Trace B indicates its current. Trace C, the MUR120 diode current, clearly shows the switched packets of energy delivered to the 22μF output capacitor. The resultant output ripple voltage (Trace D) measures only 25mV at the load.

Figure 13 catches circuit output at the instant a load open has occurred. Normal current mode operation ceases just past the third vertical division. The " + " output line heads positive until the LT1072 FB pin rises to 1.2V. At this point (just past the 6th vertical division), the LT1072's internal feedback amplifier activates, causing local loop closure and regulating the output at about 57V. The non-linear slew characteristic is due to A1's feedback capacitor restrained response. Once A1's output rails, slew increases to a limit imposed by L1, the 22μF output capacitor and the LT1072's 40kHz switching rate.

To trim this circuit, connect any load below 2kΩ and set all DAC bits low. Adjust the 4mA trim for 0.300V across the 75Ω resistor. Next, put all DAC bits high and set the 20mA trim for 1.500V across the 75Ω resistor. Repeat this procedure until both points are fixed.

AC Line Dropout Detector

Digital systems driven from the AC line often require power dropout detection. Fast AC line dropout detection allows a memory store command to be issued before DC

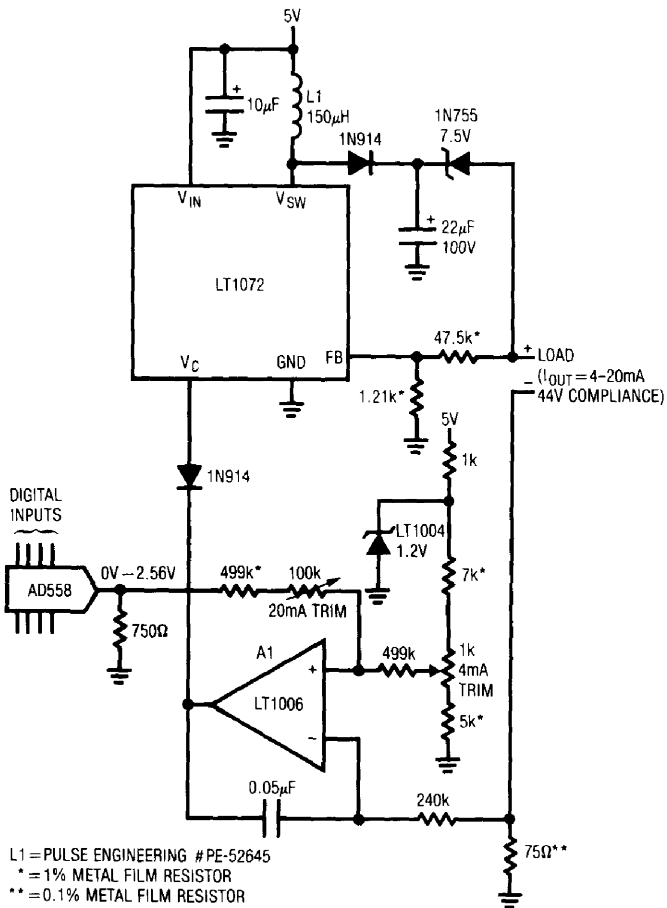


Figure 11. 5V Powered, Digitally Controlled 4-20mA Current Loop Generator

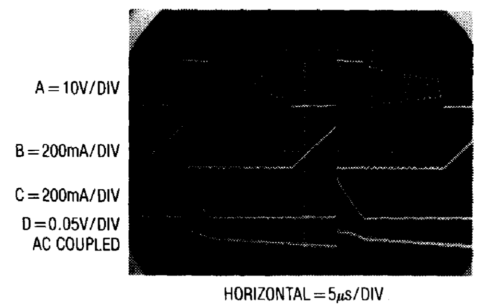


Figure 12. Figure 11's Waveforms

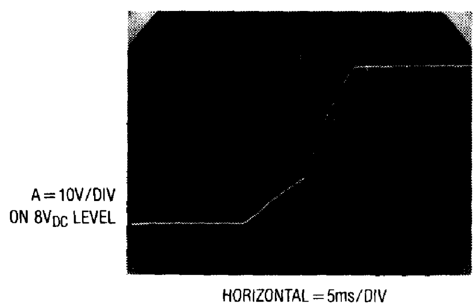


Figure 13. Open Load Characteristics for Figure 11's Current Source. LT1072 Crosses over into Constant Voltage Mode at 57V

power falls. Figure 14's circuit detects AC dropout by connecting an optoisolator across the power transformer's rectified secondary. Normally, the AC line (Trace A, Figure 15) turns on the LED every 8ms (1/2 cycle of the line), causing the output transistor to reset the 0.01μF capacitor (Trace B). When the line drops out, the capacitor charges via the 33k resistor. The resultant ramp voltage is compared by C1A to a +5V supply derived reference. In this case, the 2k-3k resistors bias C1A to go low (Trace C) within one cycle of AC line dropout. Typically, the DC regulator will supply 50ms-100ms of hold-up before it begins to sag. This hold-up period, which should be verified in any individual application, permits adequate time to execute a memory store operation. C1B serves as a final warning that power failure is imminent. It goes low when the 5V regulator input drops below the threshold set by the selected resistor shown on the schematic. This value should be chosen so that C1B trips when the regulator input approaches its specified dropout voltage.

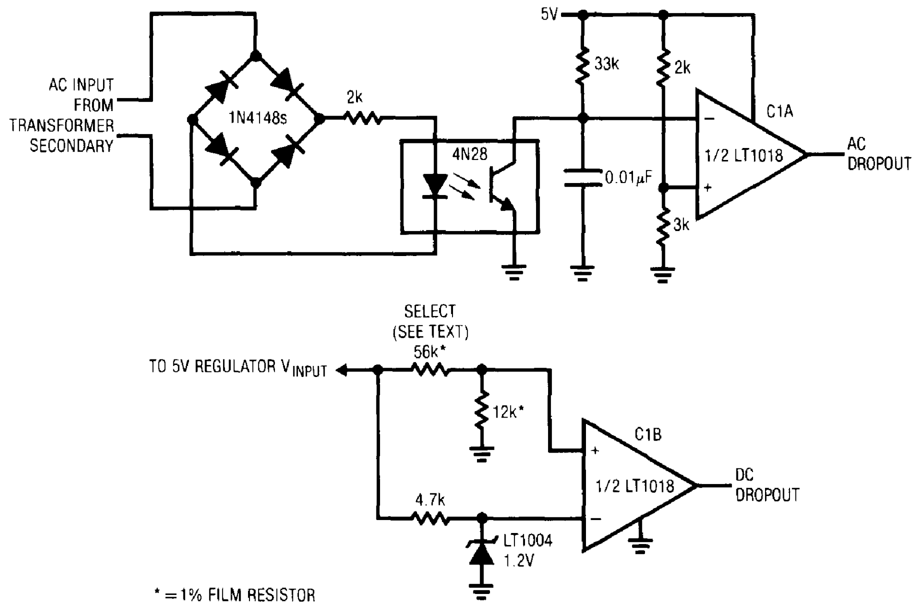


Figure 14. AC-DC Dropout Detector

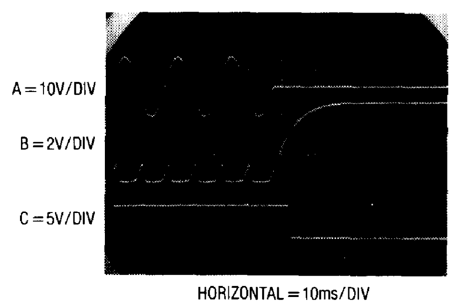


Figure 15. AC Line Dropout Detector Operates within a Half Cycle

Memory Save Circuit

Figure 16 is another circuit for saving memory contents when power goes down. This DC sensing circuit is useful where AC line dropout detection is not feasible. It functions by utilizing the different dropout voltages of two regulators. In operation, the LT1086 supplies 5V power to the main system, while the LT1020 drives the memory section. When input power, which could be from a battery or filter capacitor, falls (Trace A, Figure 17) the LT1086 drops out first (Trace B). This is detected by the LT1020's onboard auxiliary comparator, which goes low (Trace C). This alerts the memory section to store data. The LT1020 regulator output (Trace D) maintains memory power for additional time due to its extremely low dropout characteristics. It finally begins to fall about 50ms after the memory store command. The optional connections shown allow extended hold up times.

Overvoltage Protection Circuit

Figure 18's circuit represents the other extreme in power supply protection. It prevents system damage due to overvoltage produced by regulator failure. If the regulator fails in a way which effectively connects the raw DC supply to the 5V rail, overvoltage will occur. This failure mode is possible if the pass transistor shorts or the feedback loop opens up. C1A compares the 5V supply (Trace A, Figure 19) to the LT1004 reference via a resistive divider. If the supply rises beyond 5.5V (rise starts just past the first vertical division), C1A's output goes high (Trace B), turning on the SCR via Q1. SCR current (Trace C) peaks at almost 6A as it "crowbars" the supply, blowing the downstream fuse. C1B simultaneously pulls the supply feedback node low, ensuring minimum pass transistor on-resistance if the overvoltage is due to feedback or error amplifier malfunction. About 5µs elapses from the time the supply peaks (5.5V) until it begins to shut down. In this case the maximum overvoltage is 5.7V. The 4.3k-1.2k resistor string ratio can be altered for different trip values, and the optional filter used to suppress transients. Note that the LT1018's 1.2V minimum supply voltage combines with the diode in the SCR's gate to eliminate false tripping on power-up.

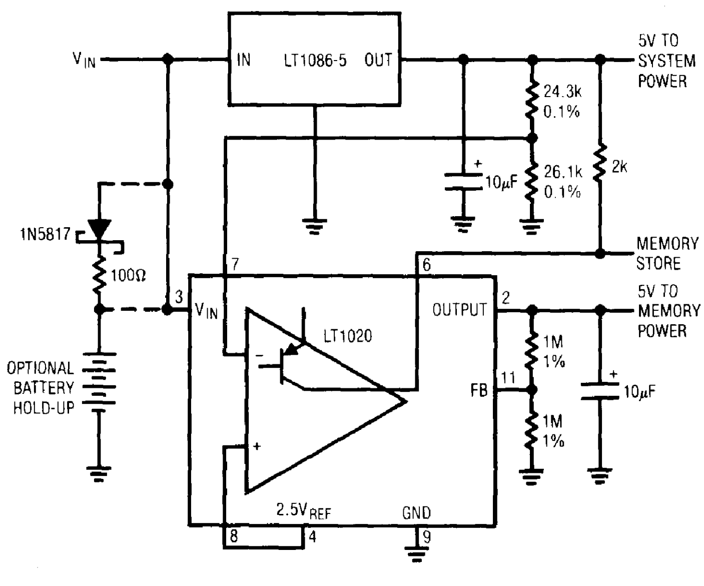


Figure 16. Memory-Save-On-Power Down

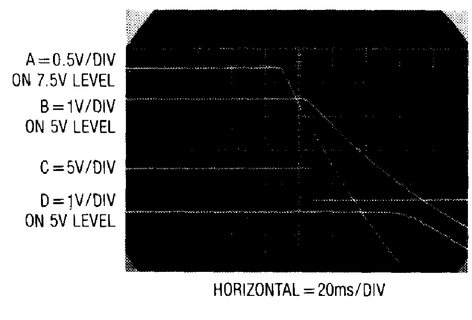


Figure 17. Differential Dropout Between Regulators Provides a Memory Store Pulse and Power Hold-Up

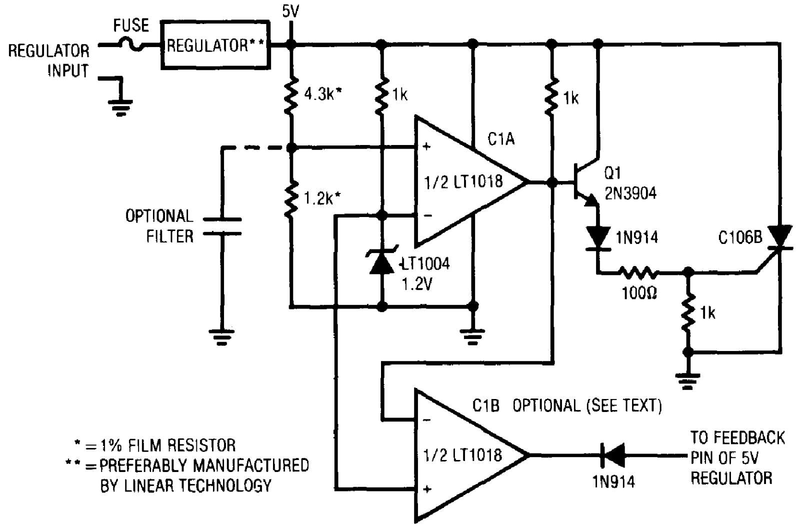


Figure 18. "Crowbar" Overvoltage Protection Circuit

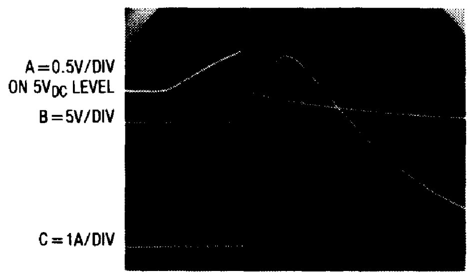


Figure 19. "Crowbar" Stops Overvoltage in 5μs

Power-On-Reset Generator

Another power related requirement involves generating a system reset pulse after supply turn-on. When supply power is applied to Figure 20, the 5V rail comes up (Trace A, Figure 21). The LT1004 clamps at 1.2V and C1A's positive input (Trace B) ramps at a time constant determined by the 0.5% resistors and the 0.1μF capacitor. When C1A's positive input ramps beyond the LT1004 potential, its output goes high, delivering a differentiated pulse to C1B's negative input (Trace C). C1B's output (Trace D) goes low for a period determined by the 0.01μF-680k differentiator. This pulse is used for system reset. The 1N914 gives quick reset for the 0.1μF delay capacitor and the Schottky diode clip's differentiator caused negative voltages at C1B's input. The turn-on threshold, in this case 4.8V, is set by the ratio of the 0.5% resistors. The output pulse delay time is controlled by the 0.1μF unit, which may be varied. Similarly, the RC combination at C1B sets output pulse width, and may be varied. The LT1018's 1.2V minimum supply voltage prevents spurious output during supply power-up.

"Watchdog" Timer Circuit

Figure 22's circuit is not for power supply management, but serves to prevent lock-up in processor based systems. This can occur if the system misses an instruction due to transient hardware or software events. Such a processor hang-up will usually cause predictable cessation of pulse events somewhere in the system. This circuit issues a reset command in response to such a cessation. In normal operation, a pulse train (Trace A, Figure 23) appears at the circuit input, causing C1A's output (Trace B) to pulse low. The diode path discharges the 0.01μF capacitor (Trace C) each time C1A's output goes low. Interruption of the input pulse train (after the 7th vertical division) allows the capacitor to charge beyond C1B's threshold, triggering it low. This pulse can be used to reset the system. C1B's negative input RC values may be adjusted to accommodate various input pulse train repetition rates.

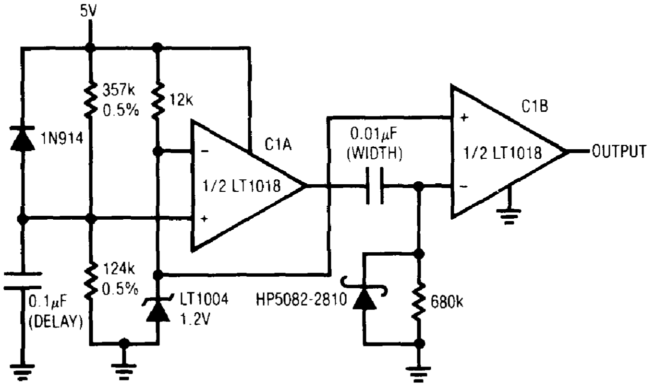


Figure 20. Power-On-Reset Pulse Generator

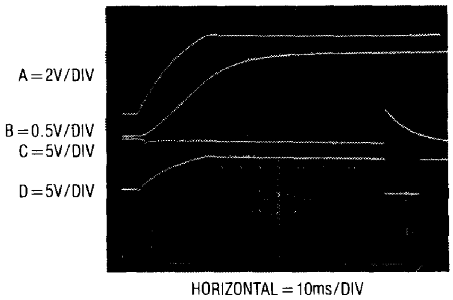


Figure 21. Power-On-Reset Pulse is Generated after Supply Stabilizes

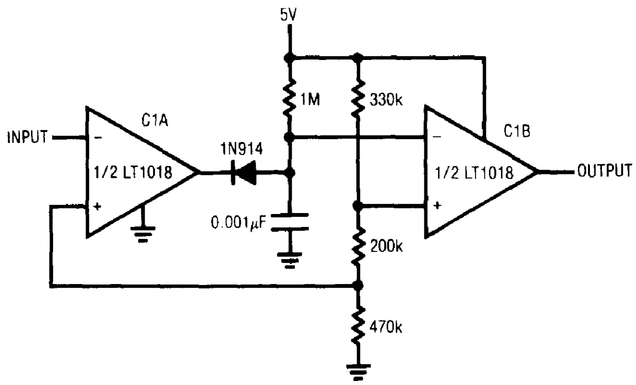


Figure 22. "Watchdog" Timer Circuit

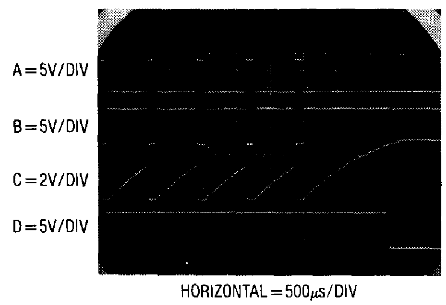


Figure 23. "Watchdog" Drops Low (Trace D) when Pulse Train Ceases

Clock Circuits

Almost all digital systems require a clock source. Generating accurate and reliable clock pulses usually involves quartz based circuits. Figure 24's two circuits cover a 1MHz–25MHz range. In Figure 24A, the LT1016 comparator is set up with DC negative feedback. The 2k resistors set the common-mode level at the device's positive input. Without the crystal, the circuit may be considered as a very wideband (50GHz GBW) amplifier biased at 2.5V. With the crystal inserted, positive feedback occurs and oscillation commences. Figure 24A is useful with AT-cut fundamental mode crystals up to 10MHz. Figure 24B is similar, but supports oscillation frequencies to 25MHz. Above 10MHz, AT-cut crystals operate in overtone mode. Because of this, oscillation can occur at multiples of the desired frequency. The damper network rolls off gain at high frequency, ensuring proper operation.

Figure 25's circuit is also similar, but optimized for lower frequency crystals. C1A is the oscillator, with C1B and Q1 used as a sink-source buffer if desired. These circuits also operate with lower cost and lower performance ceramic resonators substituted for the crystal.