design ideas

Edited by Bill Travis and Anne Watson Swager

Bridge-temperature measurement allows software compensation

John Wynne, Analog Devices Inc, Limerick, Ireland

Bridge transducers are notoriously temperature-sensitive. When the temperature changes, almost everything else varies with some parameters increasing and some decreasing. The TCS (temperature coefficient of span) is generally negative for piezoelectric pressure sensors, and the TCR (temperature coefficient of resistance) is positive. In other words, as the temperature rises, the sensitivity decreases, and the resistance of the bridge increases. In general, the TCS and TCR are close to each other. This fact has in the past motivated designers to add both active and passive external components to achieve some measure of temperature compensation. However, the calibration of such systems can be tedious; the resulting performance, problematic. Piezoelectric-bridge manufacturers have tried to ease the problem by equalizing the coefficients in their manufacturing processes. Another approach is to simply measure the temperature of the bridge and then use a μC to compensate in software, given certain basic properties, such as the bridge resistance at 25°C and the TCR. This approach is effective, but concerns that the temperature you measure may not be the real temperature of the bridge hamper it. For instance, placing the temperature sensor relative to mechanical attachment of the strain gauge has a crucial bearing on the accuracy of the reading. It's not unusual to see errors of 1°C or more in such situations. The idea presented here (**Figure 1**), suggested in **Reference 1**, is to determine the temperature of the bridge by measuring the voltage across the bridge as a result of a known excitation current flowing through it.

R_{REF}, reference voltage V_{REF}, and op amp IC_1 determine the excitation current, which equals V_{REF}/R_{REF}. The differential bridge output, seen between terminals OUT(+) and OUT(−), feeds directly into channel AIN1 of the AD7706 ADC. This signal is a pseudodifferential input with respect to the ADC's Common input and can accept full-scale signals as low as 20 mV while providing full 16-bit performance. The AD7706 has three pseudodifferential inputs, all having the Common input as reference. The Common input connects to the midpoint of the bridge and serves a reference point from which to make all

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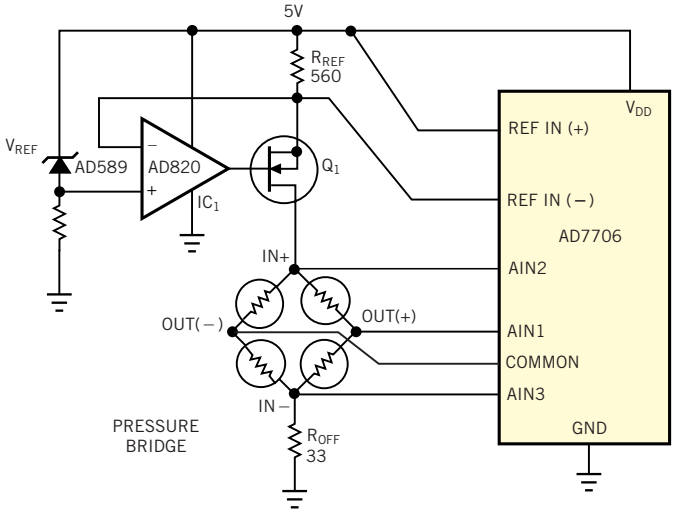
Figure 1



You can provide software compensation for bridge-temperature coefficients through accurate temperature measurements.

the necessary measurements. Computing the voltage across the bridge entails two additional measurements. Input channel AIN2 measures the voltage from the top of the bridge to its midpoint (Common terminal), and input channel AIN3 measures the voltage from the midpoint to the bottom of the bridge. You can then compute the voltage across the bridge. Assume that the resistance of the bridge is independent of the pressure under measurement at least to the extent that the error is small compared with the measured results.

The AD7706 is a complete, 16-bit (with 14-bit maximum integral nonlinearity) delta-sigma ADC intended for dc and low-frequency ac measurements. Because its power consumption is 1 mW maximum at 3V, you can use the device in loop-powered, battery-powered, and local applications. The on-chip programmable-gain amplifier has gain settings of 1 to 128 to accommodate both low- and high-level analog inputs without the need for external signal-conditioning hardware. You can find additional information about the IC at http://products.analog.com/products/info.asp?product=AD7706. (DI #2576)

REFERENCE

1. Paillard, Bruno, "Temperature compensating an integrated pressure sensor," *Sensors*, January 1998, pg 36.

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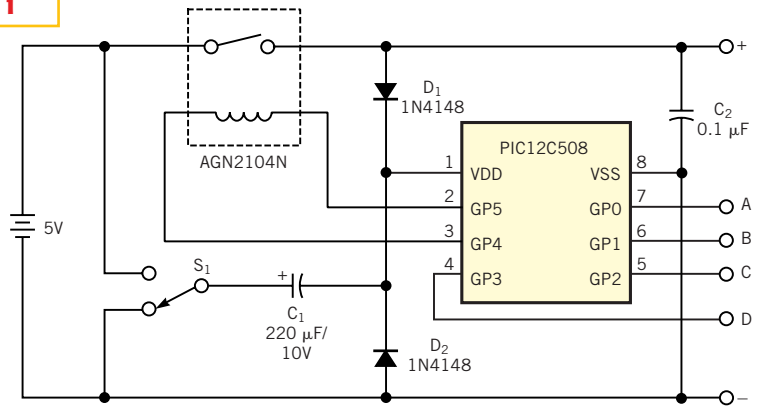
Timer automatically shuts off

Yongping Xia, Teldata Inc, Los Angeles, CA

THE CIRCUIT IN **Figure 1** is a programmable power switch that offers on-state periods of 5 sec to three hours. It consumes zero power in the off state and has zero voltage drop in the on state. S_1 is a power-on switch. When you press S_1, the battery powers an eight-pin PIC12C508 µC. Because the value of C_1 is fairly large, it powers the µC long enough for the processor to send out a pulse through GP5 and GP4 to turn on a latching relay. Once the relay is on, the µC derives power through D_1. C_1 discharges through D_2 when you release the button. After turning on the relay, the µC reads the four inputs GP0 through GP3 to determine the delay time (**Table 1**). Once the time is over, an inverted pulse appears on GP5 and GP4 and turns off the latching relay. Once the relay turns off, the circuit consumes no power. You can download the PIC12C508 assembly program for the timer from *EDN*'s Web site, www.ednmag.com. Click on "Search Databases" and then enter the Software Center to download the file for Design Idea #2571. (DI #2571)

Figure 1



This timer consumes no power in the off state and has zero voltage drop in the on state.

TABLE 1-DELAY TIMES

DCBA	Time
0000	10 sec
0001	15 sec
0010	20 sec
0011	30 sec
0100	45 sec
0101	One minute
0110	Two minutes
0111	Three minutes
1000	Five minutes
1001	10 minutes
1010	15 minutes
1011	30 minutes
1100	45 minutes
1101	One hour
1110	Two hours
1111	Three hours

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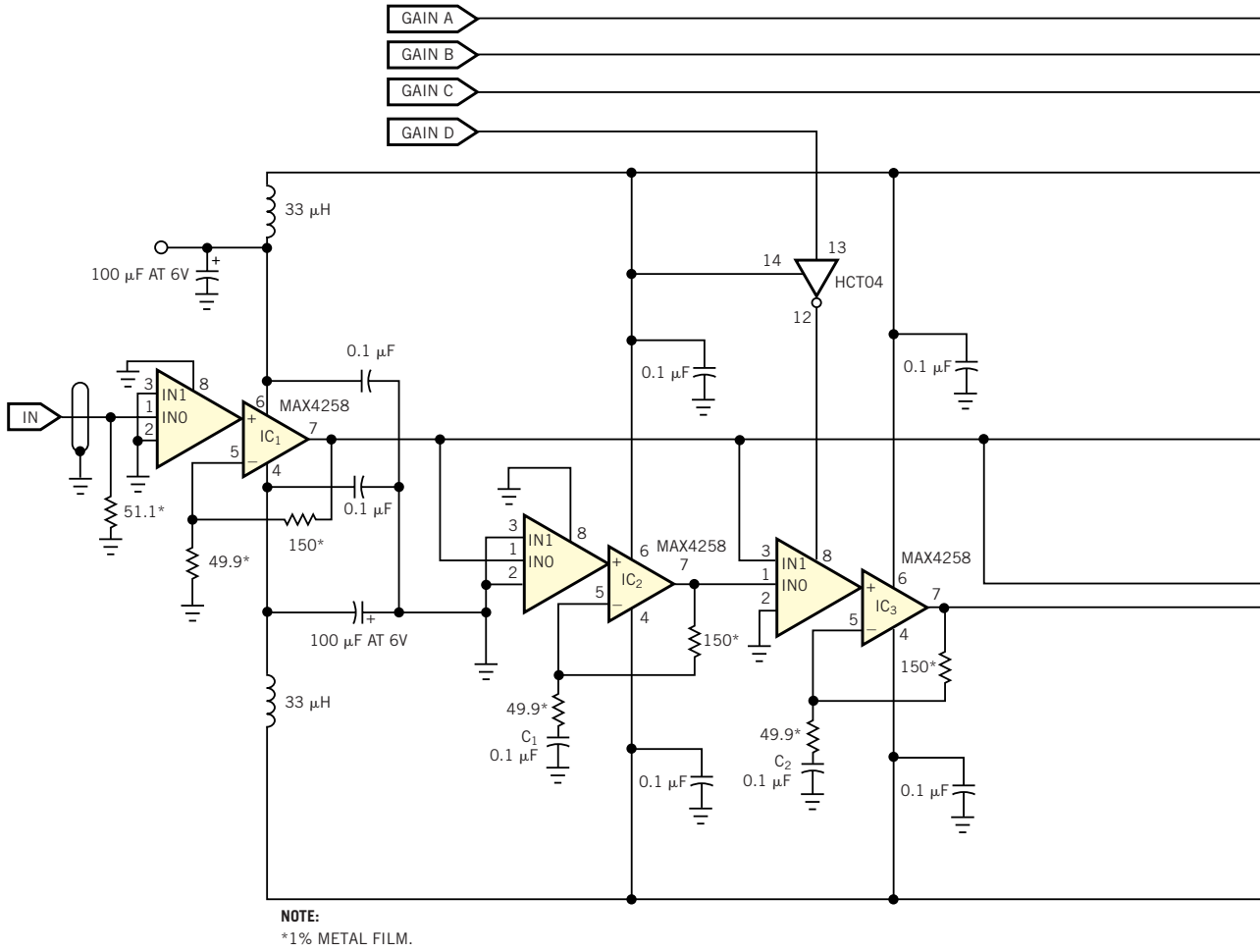
Video amplifier provides digital gain control

Stephen Woodward, University of North Carolina, Chapel Hill, NC

Programmable-gain amplifiers, many of them monolithic, are continuously improving, with lower noise and higher gain-bandwidth products. But for high-end applications, multichip circuits are still necessary. For example, the amplifier in **Figure 1** originally served as the photomultiplier preamplifier in a Doppler system intended for eventual operation in the Martian atmosphere. The design is based on a switchable array of six Maxim MAX4258 dual-channel video multiplexer-amplifiers, IC_1 through IC_6. Under control of a 4-bit input word, you can set the number of stages in the gain cascade to three, four, five, or six. Because each multiplexer-amp has a fixed gain of four, each unit change in the stage count changes the overall gain by 12 dB. In addition, you can interpose a 6-dB attenuator between the last and the next-to-last gain stages. The attenuator adds a factor-of-two resolution to the programmed gain and eight distinct gain settings (**Table 1**).

Gain-change settling time is lower than 30 nsec. The greater-than-100-MHz bandwidth of each stage results in an overall passband for all gain settings of greater than 60 MHz. The five lowpass-bandpass capacitors, C_1 through C_5, determine the lower end of the passband. In the original application, the frequen-

Figure 1



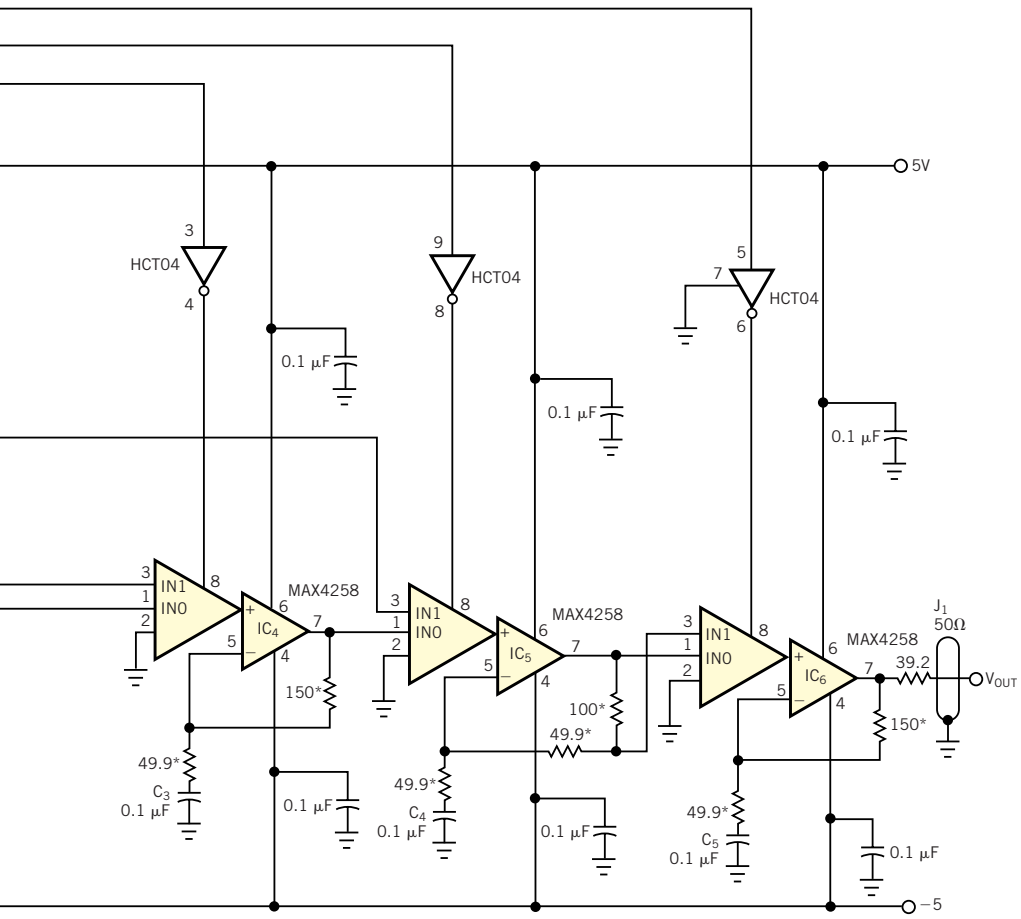
NOTE:
*1% METAL FILM.

You can obtain eight distinct gain settings with this low-noise, high-bandwidth video amplifier.

cies of interest don't extend much below 100 kHz. So, using 0.1-µF capacitors results in a roll-off of approximately 50 kHz. Larger values for these capacitors would reduce this figure. Omitting the capacitors for a dc response is not recommended, however, because the resulting amplification of IC_1's input offset would produce an output offset in the order of volts at high gain settings. You can generate the gain-programming word using any TTL-compatible, 8-bit parallel-I/O port, such as a PC's parallel printer port or an EIA-1284-compatible port. The HCT04 CMOS inverter chip in the gain-control pathway blocks any possible noise entry in the gain-control lines.

TABLE 1–DIGITAL GAIN SETTINGS

Code	D	C	B	A	Gain (into 50Ω, in decibels)
1	0	0	0	0	×16=24.1
2	0	0	0	1	×32=30.1
3	0	0	1	0	×64=36.1
4	0	0	1	1	×128=42.1
5	0	1	1	0	×256=48.2
6	0	1	1	1	×512=54.2
7	1	1	1	0	×1024=60.2
8	1	1	1	1	×2048=66.2



The overall input-referred voltage noise is approximately 2 nV per the square root of hertz, equivalent to the Johnson noise of a 250Ω resistor. Maximum output level is 15 dBm (3.6V p-p) into 50Ω and twice that into high-impedance loads. The combination of extreme gain and high-frequency response (gain-bandwidth products approaching 200 GHz) of this circuit mandates careful attention to issues of ground-plane and power-supply-bypass integrity. In addition, you must make every effort to minimize stray capacitance around the feedback-pin (Pin 5) components of all gain stages. (DI #2559)

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Simple circuit detects dc ringing

Jerzy Chrzaszcz, Warsaw Institute of Technology, Poland

Ring detection is a common task in telephony-related digital design. The goal is to sense an ac ringing voltage applied to the telephone line by a central office or PBX (private branch exchange) and then pass an appropriate signal to the µC or µP. **Figure 1a** shows a typical ac-coupled ring-detection circuit. The serially connected capacitor closes the ac path and the optoisolator provides galvanic isolation between the line and the logic. The output capacitor integrates the pulse train to form a ring envelope signal. More sophisticated designs may use the unfiltered output for ring-frequency discrimination. Unfortunately, some PBX systems signal ringing to extension phones by raising the dc line voltage. A traditional ac-coupled detector is thus useless. The circuit in **Figure 1b** consists of a full-wave rectifier, a current-limiting resistor, a zener diode, and a high-gain optoisolator with output pullup. By changing component values, you can easily meet circuit requirements for circuit isolation, input-voltage range, threshold voltage, and line load. (DI #2567)

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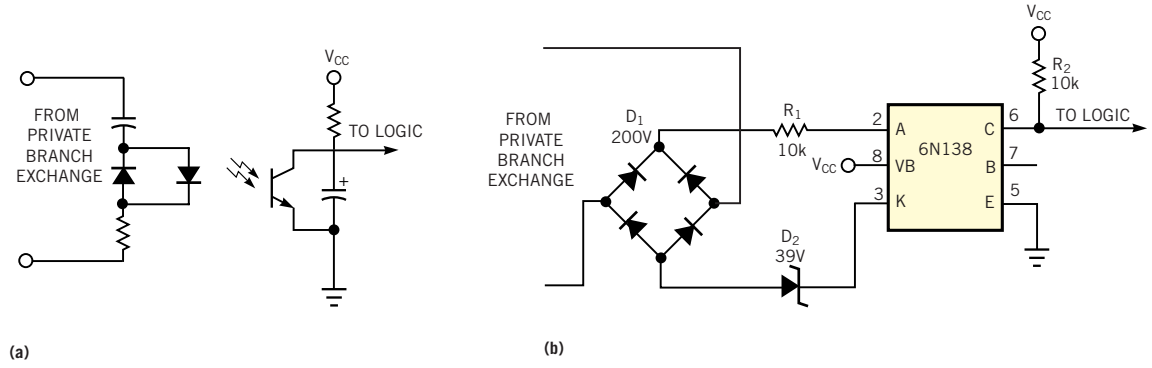
Figure 1



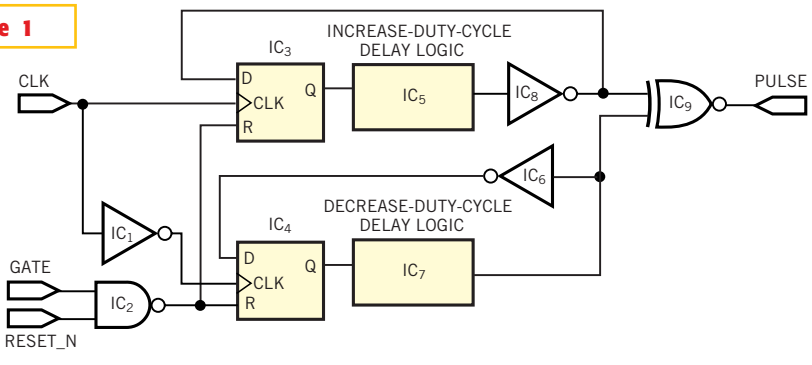
The ac-coupled circuit in (a) is useless in some PBX systems; the configuration in (b) takes over for PBX-generated dc ringing signals.

Gated clock has duty-cycle control

Paul Kemp, University of Colorado, Colorado Springs, CO

The circuit in **Figure 1** produces clock pulses with variable duty cycle from a gated clock. The output of the circuit, pulse, is always 180° out of phase with the clock input. When the delay-logic elements, IC_5 and IC_7, have the same propagation delays, the duty cycle of the circuit's output is 50%. The circuit produces gated clock pulses when the gate input, gate, is high and the active-low reset, reset_n, is high. Increasing the propagation delays of the increase-duty-cycle delay-logic element, IC_5, causes an increase in the duty cycle of the gated-clock output, pulse. The de-

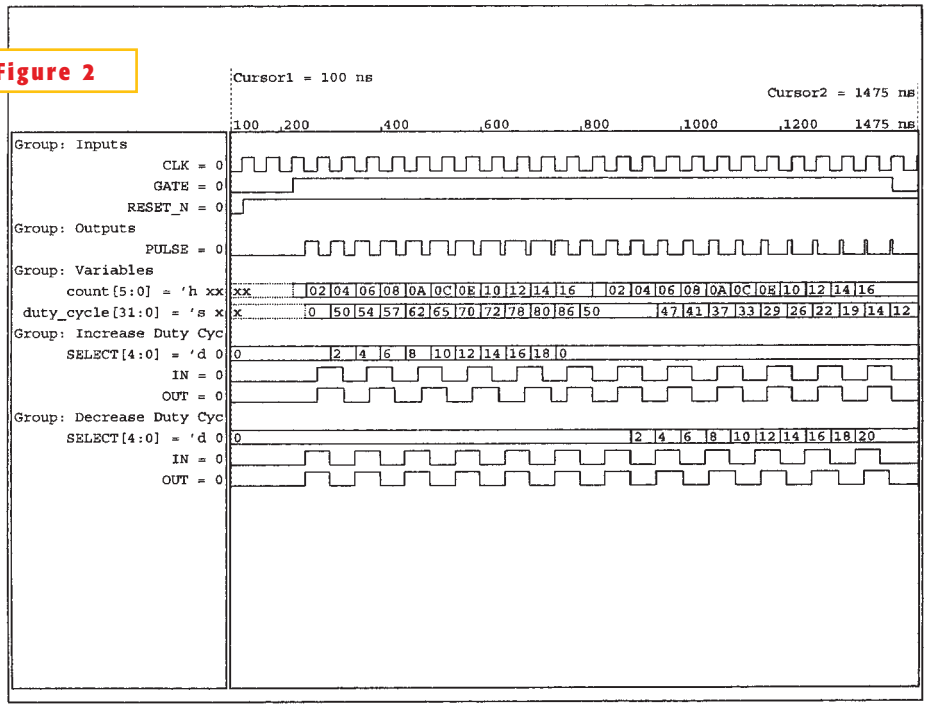
Figure 1



You can control the duty cycle of pulses from a gated clock.

crease-duty-cycle delay-logic element, IC_7, reduces the duty cycle of the gated-clock output. **Listing 1** is a Verilog model of the circuit; a Verilog testbench verifies the circuit's function. A pair of delay-logic elements is modeled with 20 delay lines of 1 nsec each. The testbench instantiated this operation. A simulation (**Figure 2**) used Cadence Verilog-XL. A 20-MHz clock serves as the input clock. The select signals in **Figure 2** for the increase-duty-cycle delay-logic element, IC_5, and the decrease-duty-cycle delay-logic element, IC_7, correspond to the number of 1-nsec delay elements inserted into the delay paths. Thus, a select value of 12 corresponds to a 12-nsec delay. You can download **Listing 1** and the Verilog testbench from *EDN*'s Web site, www.ednmag.com. Click on "Search Databases" and then enter the Software Center to download the file for Design Idea #2554. (DI #2554)

Figure 2



Verilog simulates the function of the circuit in Figure 1.

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LISTING 1—GATED-CLOCK DUTY-CYCLE CONTROLLER

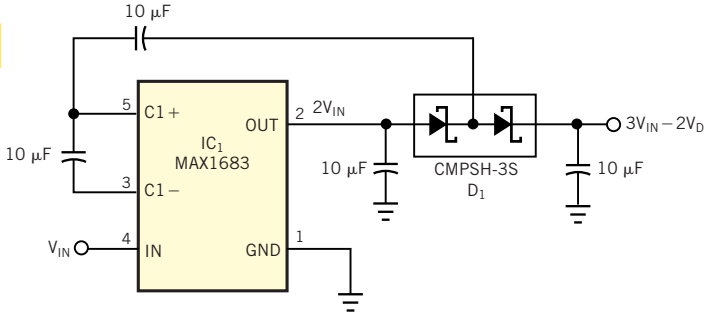
```
`timescale 1ns/1ps   // 1ns time units with 1ps resolution

module pulse_shaper (
                     CLK,           // I
                     GATE,          // I
                     GATE_DEC_DLY,  // I
                     GATE_INC_DLY,  // I
                     RESET_N,       // I
                     GATE_DEC,      // O
                     GATE_INC,      // O
                     PULSE          // O
                    );

//   Input Declarations
input        CLK;           // System clock
input        GATE;          // Active high signal produces variable duty cycle
pulses
input        GATE_DEC_DLY;  //
input        GATE_INC_DLY;  //
input        RESET_N;       // Active low asynchronous reset


//   Output Declarations
output       PULSE;         // Variable duty cycle output pulse
output       GATE_DEC;      //
output       GATE_INC;      //


//   Register Declarations
reg          GATE_DEC;      //
reg          GATE_INC;      //

//   Parameter Declarations
parameter    dly = 1;

// Generate a pulse from the system clock (CLK) and GATE signals.
assign #dly PULSE = GATE_INC_DLY ^ GATE_DEC_DLY;

always @(posedge CLK or negedge RESET_N or negedge GATE) begin
  if (~RESET_N) begin
    GATE_INC <= #dly 1'b0;
    end
  else if (~GATE) begin
    GATE_INC <= #dly 1'b0;
    end
  else begin
    GATE_INC <= #dly ~GATE_INC_DLY;
    end
  end

always @(negedge CLK or negedge RESET_N or negedge GATE) begin
  if (~RESET_N) begin
    GATE_DEC <= #dly 1'b0;
    end
  else if (~GATE) begin
    GATE_DEC <= #dly 1'b0;
    end
  else begin
    GATE_DEC <= #dly ~GATE_DEC_DLY;
    end
  end

endmodule
```

Tripler converts 5 to 15V

Ken Yang, Maxim Integrated Products, Sunnyvale, CA

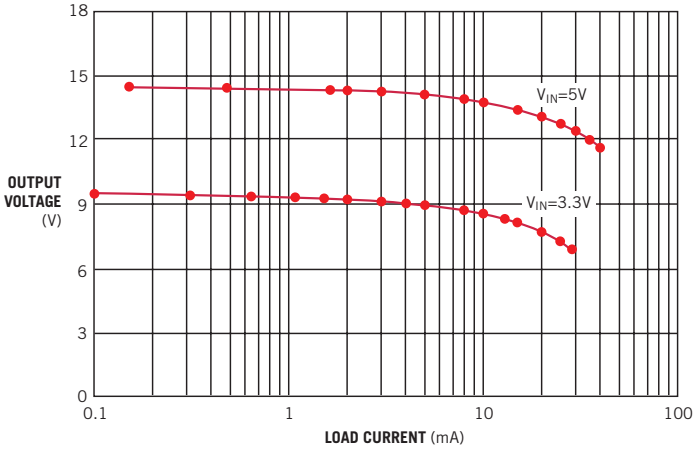
By configuring a charge-pump voltage doubler as a tripler, you can readily derive 15V from 5V (**Figure 1**). A 15V rail is useful for powering op amps, LCD-bias circuits and other low-current applications. The connections shown configure the IC_1 voltage doubler as a tripler. The no-load output voltage of the circuit is approximately $3V_{IN}-2V_D$, where V_D is the voltage drop across one diode. Use Schottky diodes as shown to minimize V_D and its effect on output voltage. Because the circuit's finite output impedance causes the output voltage to drop with load current (**Figure 2**), a practical limit for load current is approximately 30 mA. (DI #2570)

Figure 1



This circuit (almost) triples the input voltage for low-current applications.

Figure 2



Finite output impedance causes a decline in voltage with increasing load current.

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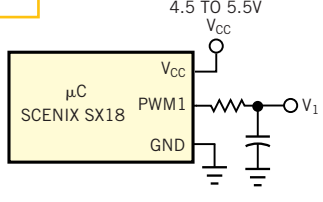
Generate stabilized PWM signals

Martin Ossmann, FH, Aachen, Germany

A standard technique for generating analog voltages using µCs is to use a PWM output and filter the signal with a simple RC filter (**Figure 1**). The voltage of the PWM signal is directly proportional to the µC's supply voltage, so it is not necessarily clean or stable. To overcome this problem, you can use the circuit in **Figure 2**. Here, a 74HC14 Schmitt-trigger array serves as an output stage for three PWM signals from an SX18 µC. (The idea applies to other µCs, too.) The 74HC14 derives its supply voltage, V_{CCA}, from the stabilization circuit comprising the inexpensive shunt regulator, SR_1. You can adjust V_{CCA} by trimming R_1. The test circuit used V_{CCA}=4.096V. The PWM signals now have a stable amplitude that varies less than 0.1% when the µC's supply varies from 4.5 to 5.5V. Resistors R_3 to R_5 limit the current flowing from the µC through the 74HC14's input-protection diodes when V_{CCA} is too low. The values

Figure 1

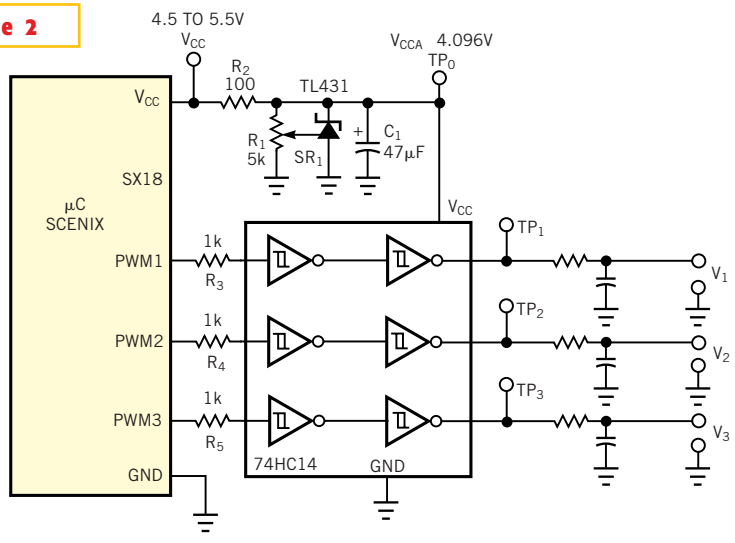


This classic PWM circuit suffers from supply-voltage sensitivity.

of R and C depend on the application. The test circuit uses 10 kΩ and 4.7 µF. If you feed multiple analog (or PWM) signals through a single IC, you usually encounter crosstalk. To characterize the circuit in **Figure 1** for internal crosstalk and unmatched delays, conduct the following tests.

Generated three PWM signals with different frequencies and 1-to-1 duty cycles. With a 0-dB reference-level square-wave signal at test point TP_1, crosstalk to test points TP_2 and TP_3 measures −70 dB. The first harmonic of the PWM signal (theoretically zero for a 1-to-1 duty cycle) is down 65 dB at test point TP_1. At test point TP_0, spurs are down 75 dB. So, the circuit in **Figure 1** has very good crosstalk characteristics. Also, if the duty cycle of one PWM channel changes, the influence on the voltage that other channels generates is less than 0.1%. You must take care to ensure that the switching delays of the 74HC14 do not change with varying V_{CC} applied to the µC. If the switching delays change with V_{CC} because of the changing levels of the driving signals, V_{CC} influences the generated output voltage, even if V_{CCA} is constant. You can use the circuit for precise generation of voltages, thanks to the temperature stability of the TL431. You can also use it for inexpensive implementations of sigma-delta converters, or to generate voltage-stabilized rectangular waveforms. (DI #2573)

Figure 2



Schmitt triggers with a stabilized supply make the PWM signals insensitive to supply voltage.

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Switched-capacitor converter suits portable applications

Clinton Jensen, National Semiconductor, Santa Clara, CA

Basic switched converters generally provide one simple voltage conversion. The most common application for these circuits are to double, invert, and sometimes halve the input voltage. Because they are unregulated and have no stability problems, you can configure them to perform multiple conversions as well. However, because they have no inherent regulation, it is a good idea to use a regulated voltage as the input source. Multiple converters exhibit some voltage change at the output as a function of loading (because of the output resistance), but this drop is often acceptable. The circuit in **Figure 1** is a triple-output switched-capacitor circuit. You can configure the circuit using any switched-capacitor IC that's capable of inversion. This example uses the LM2664, but you can use larger ICs, such as the LM2661 or LM2663, to obtain higher current. The circuit in **Figure 1** can simultaneously invert, double, and halve the input voltage over an input range of 1.8 to 5.5V. The combined current capability of the three outputs equals the maximum load current of the IC in either of the standard topologies: inverting or doubling (40 mA for the LM2664 and 200 mA for the LM2663).

The output resistance for any output is equal to or less than the typical output resistance of the basic doubler or inverter. This last statement holds true only if you realize that the doubling output is actually $2V_{IN} - 2V_{FD}$, where V_{FD} is the forward drop of the diodes used. The doubling output simply uses two diodes to make a discrete charge pump in conjunction with the switch that connects CAP+ to V_{IN} during one cycle and to ground during the next cycle. The extra diode drops may be a problem in some applications, but they would be insignificant if you connected a linear, low-dropout regulator to the doubled output. The halving output uses the concept of an unregulat-

ed inductive step-down switcher with a constant 50% duty cycle. At no load, the output from a 50%-duty-cycle pulse filtered through the inductor and output capacitor is half the peak voltage of the square wave. The same switch used for the doubling function produces the square wave. In the topology of **Figure 1**, you always obtain the inverting function that is inherent to the IC, and you can use or omit the other two outputs as needed. (DI #2578)

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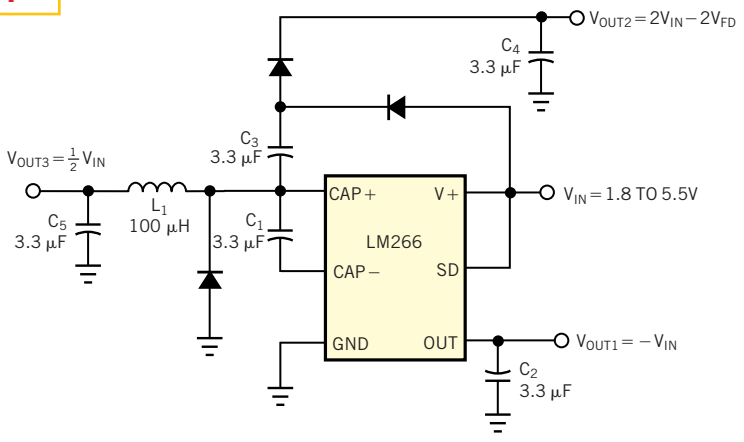
Figure 1



One switched-capacitor IC simultaneously inverts, doubles, and halves the input voltage.

Current-limit switch is digitally programmable

Budge Ing, Maxim Integrated Products, Sunnyvale, CA

CURRENT-LIMIT SWITCHES are virtually ubiquitous in system controls. They provide a safe means for regulating the current delivered to a load circuit. The switches allow the load current to increase to a programmed limit but no higher. Typically, the current limit is a function of the voltage across an external resistor, produced by the current from a fixed source internal to the switch IC. This voltage serves as the reference for an internal current-limiting amplifier. By replacing the resistor with a digital potentiometer, you can easily program the current limit (**Figure 1**). IC_1 is a current-limit switch with a maximum programmable limit of 1A. The limit equals $1380/R_{SET}$, where R_{SET} is the resistance between pins 5 and 6 of IC_2. IC_2 is a 50-kΩ digital potentiometer whose resistance is programmable in 32 equal increments. With $\overline{CS}$ held low, high-to-low transitions at $\overline{INC}$ (Pin 1) increments IC_2's internal counter.

These transitions increase the resistance between W and L when U/$\overline{D}$ is low and reduce it when U/$\overline{D}$ is high. IC_1 includes a thermal-shutdown capability that turns the load current completely off when the chip temperature exceeds 135°C. It restores the load current when the temperature cools by 10°C. If the short-circuit fault is still present, the switch cycles off and on, yielding a pulsed load current. An open-drain Fault output (Pin 8) switches low when the load demands current beyond the programmed limit, enabling an external system to monitor the condition of the current switch. (DI #2577)

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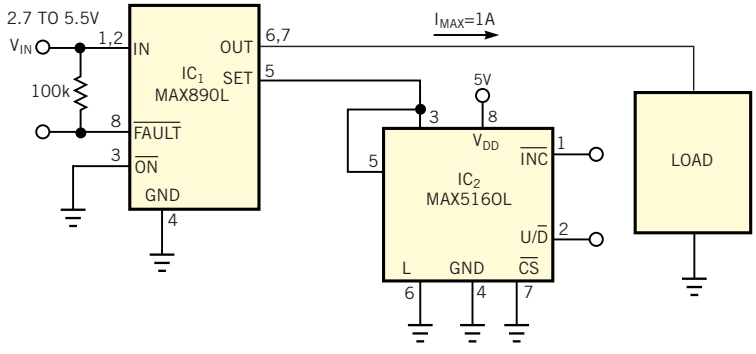
Figure 1



You can program a current limit to 1A in 32 equal increments by using a digital potentiometer.