design ideas

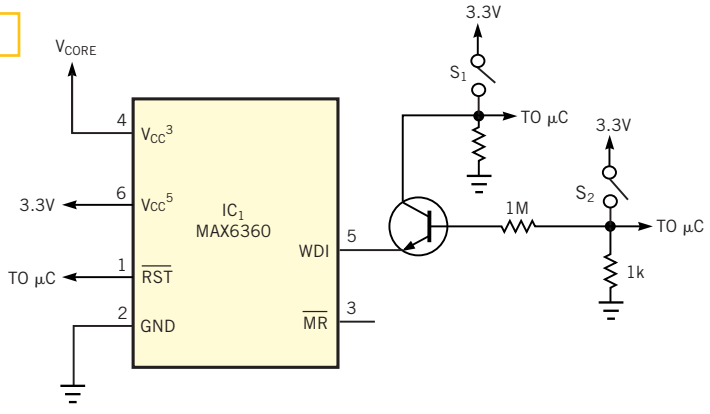
Edited by Bill Travis and Anne Watson Swager

Watchdog timer allows entry to test mode

Greg Sutterlin and Larry Barnes, Maxim Integrated Products, Sunnyvale, CA, and Craig Gestler, Mining Safety Appliances Co, Mars, PA

MANUALS FOR microprocessor-based devices often include instructions for entering a "secret mode" in which you can test or reset the device. These instructions typically ask you to depress and hold one or two switches for a minimum time interval. You can adopt several measures to avoid accidentally triggering the test mode: Depress two keys, hold both keys simultaneously and continuously through the minimum interval, and make the interval two to five seconds long. You can implement such designs with a handful of resistors, capacitors, and diodes and a comparator or two. Such circuitry may remain useless or lack customer appreciation, but it raises cost and complexity while lowering system reliability. A better alternative is to implement the function with minimal additional components (**Figure 1**).

Figure 1



You can activate IC_1 only by depressing S_1 and S_2 simultaneously for at least 2.9 sec.

Microprocessor-based devices usually include a voltage supervisor that monitors the V_{CC} level and, in some cases, the core voltage. When either voltage drops below its threshold, the supervisor issues a reset to the microprocessor. IC_1 in **Figure 1** monitors two voltages, provides a power-on reset, and includes a watchdog timer. If you don't need the watchdog function elsewhere in the system, it can help to implement the switch-delay circuitry. Fortunately, the watchdog timer self-resets when the WDI (watchdog input) Pin 5 is floating, an indication that the circuit is disabled. Thus, you can implement the switch-delay circuitry by enabling and disabling the watchdog timer. Simply provide an interface between WDI and the switches that enable the test mode. The nominal time-out period for IC_1's watchdog timer is 2.9 sec.

WDI must float when both switches are open and when you depress only one. When you depress both, WDI must assume either the active-high or the active-low state as specified in the data sheet. Note that WDI can remain floating while sinking 5 µA. The npn transistor isolates WDI from the switches' pulldown resistors. When S_2 closes, current flows through the base of the transistor to WDI, which remains floating because the 1-MΩ resistor limits the current to less than 5 µA. The transistor turns on and forces WDI to the active-high level only when you depress S_1 as well. If you depress the switches in reverse order, WDI switches high only when you close S_2. You must close both switches to activate the watchdog timer. After the timer activates, IC_1 imposes a 2.9-sec delay before asserting a reset (Pin 1). If you release either or both switches during this 2.9-sec period, the timer resets. Thus, for the minimal cost of an npn transistor and three resistors, the supervisor IC can monitor two voltages, provide a power-on-reset signal, and implement a dual-switch delay function. To monitor one voltage, you can replace IC_1 with a MAX823.

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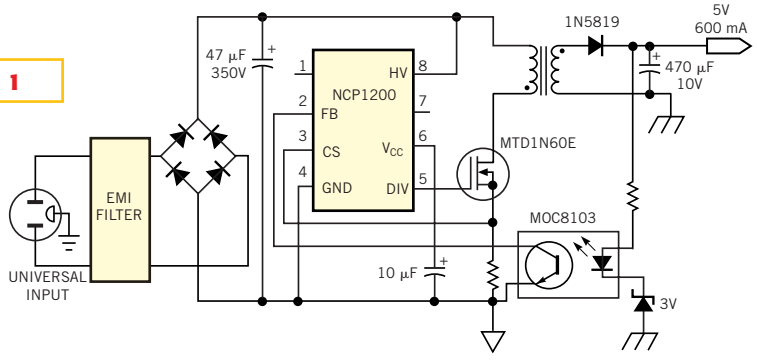
Transistors offer thermal protection for controller

Christophe Basso, On Semiconductor, Toulouse, France

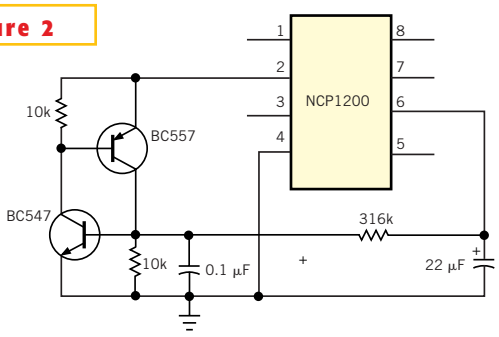
When a switch-mode power-supply controller, such as On Semiconductor's NCP1200, operates at a high ambient temperature, you should protect the entire power supply against lethal thermal runaway. The NCP1200 operates directly from the power mains without an auxiliary winding; therefore, the die in the IC dissipates power (**Figure 1**). Unfortunately, the internal temperature-shutdown circuitry cannot perform its protection function because the die is not at ambient temperature but at a temperature that's higher than ambient by a few tens of degrees. To overcome this problem, you can implement a thermistor-based design, but this solution compromises the system's cost. Fortunately, you can use standard bipolar transistors to implement a low-cost thermal-shutdown circuit. **Figure 2** shows how to build a classic thyristor circuit using two inexpensive bipolar transistors: a BC557B pnp and a BC547B npn. The idea is to use the negative-temperature coefficient of the silicon (~−2 mV/°C) to fire the thyristor.

Figure 1



A controller IC implements a low parts-count offline power supply.

Figure 2



Two bipolar transistors configure a thyristor-based temperature-shutdown circuit.

In the inactive state, both the upper and the lower transistors in **Figure 2** are in the off state because of the presence of the 10-kΩ resistors. The thyristor structure connects between the feedback pin, FB, and ground. One feature of the NCP1200 is to skip unwanted switching cycles when the power demand diminishes. The IC performs this function internally by constantly monitoring the FB pin. When the voltage on this pin falls below a certain level, the IC internally blanks the cycles, and the power transistor turns off. If the thyristor permanently pulls the FB pin to ground, the NCP1200 no longer delivers pulses. Once latched, the thyristor prevents any restart, until you disconnect the power supply from the power mains. The 316-kΩ resistor combines with the 10-kΩ resistor to form a voltage divider from the V_{CC} rail. This rail, on average, varies from lot to lot from 10.3 to 10.6V, for a total ΔV of 300 mV. This variation translates to less than 10 mV at the transistor's base. When the temperature rises, the BC547's turn-on V_{BE} diminishes until it reaches the divider voltage on its base. (This voltage is approximately 320 mV, but you can alter it to accommodate other temperature levels.) At this point, the BC547 conducts current, and the BC557's base voltage starts toward ground. The BC557's collector current further biases the BC547's base, and the thyristor latches, thereby permanently stopping the NCP1200's pulses. Once you remove the supply from the power mains, the thyristor resets. The 0.1-µF capacitor prevents spurious noise from triggering the thyristor.

We conducted tests on the thyristor-based temperature-protection scheme using BC547B and BC557B transistors. The "B" extension is important because it corresponds to a narrow h_{FE} range of 200 to 450. This design uses transistors in TO-92 packages, mounted close to each other. If only one transistor heats up, thermal results vary. Therefore, you should mount these two components close to each other on the pc-board-component side so that they will operate at approximately the same junction temperatures. From 20 bipolar-transistor combinations, you can obtain the results shown in **Table 1**. You can see that the latch-off threshold temperature varies by only approximately 5°C for all combinations of transistors (**Reference 1**).

TABLE 1–TEMPERATURE SHUTDOWN VERSUS V_{BE}

V_{BE} (mV, npn)	V_{BE} (mV, pnp)	$T_{LATCH-OFF}$ (°C)
665	654	110 to 115
666	656	110 to 115
667	656	110 to 115
666	657	110 to 115
670	659	110 to 115
664	653	115
666	652	115
667	655	110 to 115
667	657	110
669	653	110

Reference

1. "Bipolars provide safe latch-off against opto failures," *EDN*, Dec 7, 2000, pg 190.

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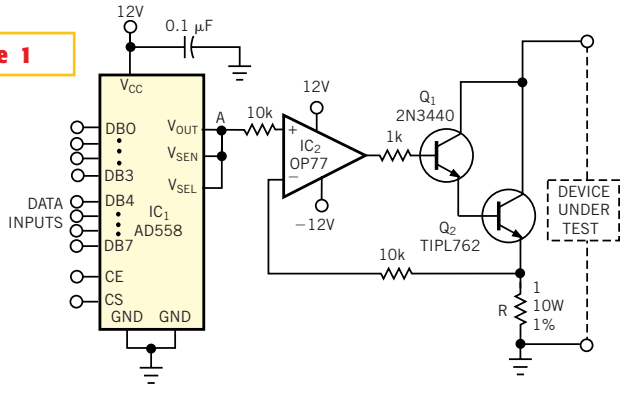
Variable load tests voltage sources

Michele Frantisek, Brno, Czech Republic

THE CIRCUIT IN **Figure 1** serves as a variable, current-sink load for testing voltage sources. You use digital commands to set the load current of the device under test over a wide range, independently of the device under test's output voltage. The circuit comprises an AD558 DAC, IC_1, which provides a reference voltage at Point A. Practically any type of DAC converter works well in this application. The AD558 is a single-supply type with an internal reference; these features simplify the design. IC_1 generates an output voltage of 0 to 2.55V (**Table 1**). The control inputs CE and CS in IC_1 allow you to control the DAC from a microprocessor bus. If your application does not involve a data bus, connect CE and CS to ground to obtain direct access to the DAC's data inputs.

Figure 1



A simple circuit allows digital control of current, independent of voltage.

TABLE 1–DAC OUTPUT VOLTAGE VERSUS INPUT CODE

Digital input of IC_1		
Binary	**Hexadecimal**	**Voltage at Point A (V)**
0000 0000	00	0
0000 0001	01	0.01
0000 1111	0F	0.15
0001 0000	10	0.16
1000 0000	80	1.28
1111 1111	FF	2.55

The second part of the circuit in **Figure 1** consists of an op amp, IC_2, driving transistors Q_1 and Q_2. IC_2 compares the reference voltage at Point A with the voltage across resistor R. IC_2's output voltage controls Q_1 and Q_2 such that the voltage across R equals the reference voltage at point A. The voltage across R is proportional to the current from the device under test and is independent of the output voltage of the device under test. The value of R in **Figure 1** is 1Ω; thus, the circuit provides a sink current of 1A when the voltage at point A is 1V. With the values shown in **Figure 1**, you can control currents of 0 to 2.55A over a device under test voltage range of 5 to 250V. Be sure to limit the power dissipation in Q_2 to 120W.

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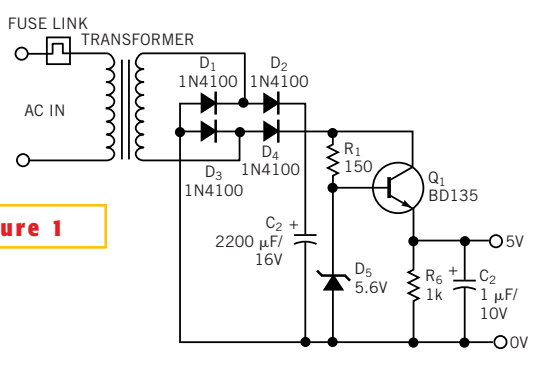
Linear supply uses switch-mode regulation

David Magliocco, CDPI, Scientrier, France

YOU CAN USE simple circuits to implement small, regulated plug-in power supplies. In **Figure 1**, a basic and versatile 5V supply uses a zener diode and an emitter-follower transistor. You must calculate and design the transformer such that Q_1 is close to saturation at low mains voltages and nominal output current. Additionally, you must choose R_1 to ensure proper bias for the zener diode. The transistor dissipates appreciable power when the mains voltage is high. **Figure 2** shows that Q_1 must handle nearly 0.75W at nominal input voltage and output current. A TO-92 small-signal transistor, such as a BC337, is adequate for 300 mA, but a medium-power device, such as a BD135, is a better choice. To cut costs, this design uses no heat

Figure 1



This simple plug-in power supply is effective but has no current limiting.

sink. Inasmuch as the circuitry is inside a nonventilated plug-in plastic case, the junction temperature of the BD135 attains temperatures greater than 100°C.

Assuming that you need current limiting, if you use a linear current-limiting circuit, Q_1 needs to dissipate nearly 2.5W in the case of a short-circuited output. The probable result is the melting of the plastic case and the failure of Q_1. To avoid that disaster, you can use switch-mode current limiting. **Figure 3** shows the circuit of **Figure 1** with some additional components, and **Figure 2** shows the benefits of the limiting. Q_1 and Q_2 act as one emitter follower, but with lower base current. A small-signal Schottky diode, BAT85, which receives its bias from R_3 and R_2, provides an approximate 0.25V reference voltage for comparator IC_{1A}'s noninverting input. The inverting input reads the voltage drop created by the output current across R_3. As long as the output current remains less than 300 mA, the output of the comparator is in a high-impedance state (open-collector), and the circuit works like a linear regulator.

If the output current reaches 300 mA, the comparator's output switches low and thus turns off Q_1 and Q_2. The current through L_1 decreases exponentially and flows through Schottky diode D_1. As the emitter of Q_1 is then at approximately 0.5V, the bias current in D_2 decreases. The voltage drop across D_2 drops by approximately 10%. As a consequence, the output current decreases until it reaches 270 mA. Then, the comparator switches back to a high-impedance state, turning on Q_1 and Q_2 and again biasing D_2 with R_1 and R_2. The current in L_1 increases exponentially until it again reaches 300 mA. L_1 is a 300-µH inductor using a powdered-iron core. **Figure 4** illustrates the current-limiting action of the switch-mode circuitry.

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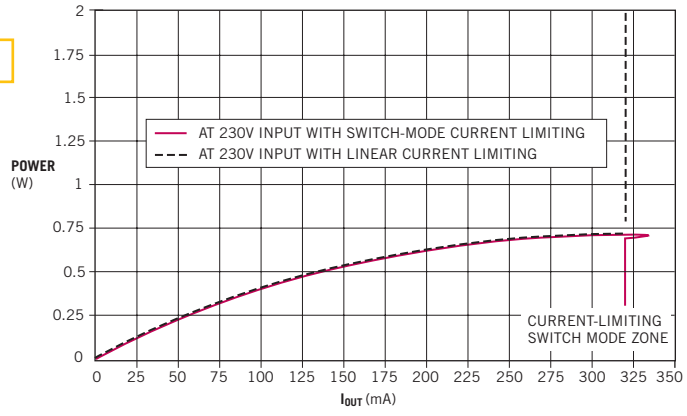
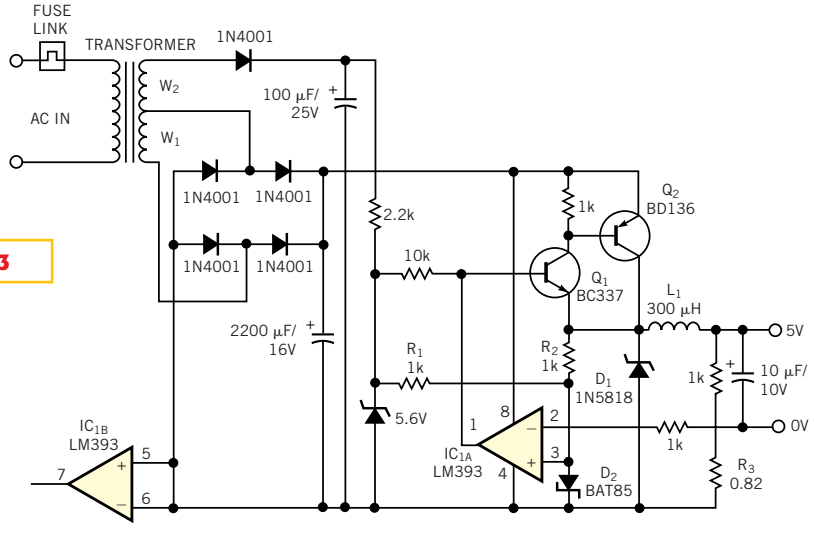
Figure 2



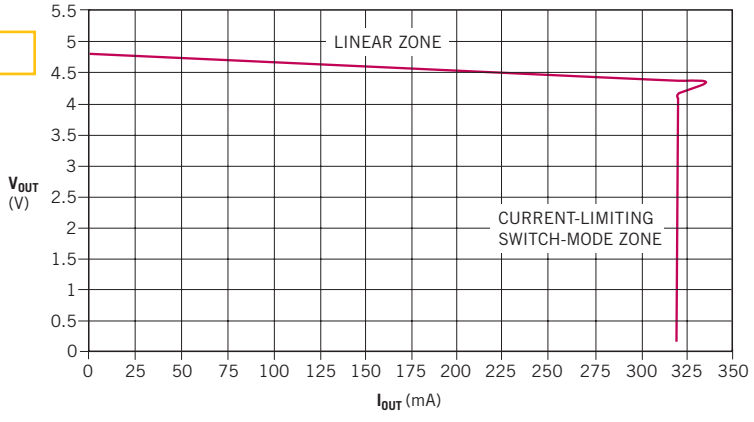
Without switch-mode current limiting, the circuit of Figure 1 can crash and burn.

Figure 3



The addition of a few components protects Figure 1's circuit against overcurrent conditions.

Figure 4



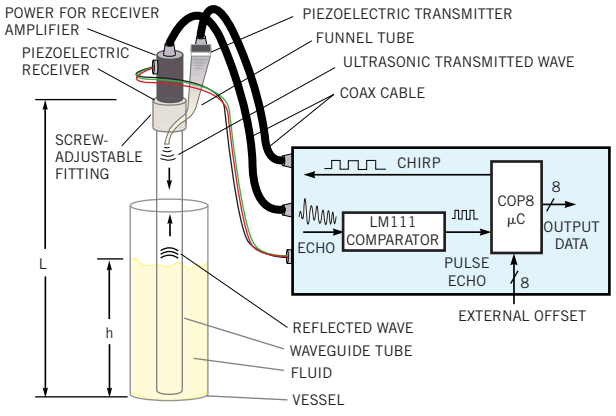
Switch-mode current limiting restricts current in Figure 3's circuit to about 320 mA.

Sonarlike method detects fluid level

Robert LeBoeuf and Eric Masse, National Semiconductor, Salem, NH

Figure 1 illustrates a simple, cost-effective method of measuring the height of fluid in a column by using ultrasonic waves. Two piezoelectric transducers generate and listen to the ultrasonic acoustical wave. First, the transmitter piezo element receives stimulation from a square wave that lasts three or four cycles. This technique produces the most efficient transfer of electrical energy to acoustical energy. The acoustical wave produced at the transmitter funnels down into the waveguide tube. The wave then concentrates at the tip of the funnel tube and disperses into the waveguide tube. Part of the wave, or "crosstalk," travels up toward the receiver. The other part travels down toward the fluid. The receiver detects and ignores the crosstalk component of the wave. Part of the crosstalk wave is absorbed in the reflection from the receiver, and the remaining energy propagates down toward the fluid. The receiver then listens to the wave that echoes off the surface of the fluid. The first of these waves that strikes the receiver is the component that has propagated toward the fluid. This component is the *primary echo*. The crosstalk wave arrives shortly thereafter with a reduction in amplitude; this wave constitutes the *secondary echo*.

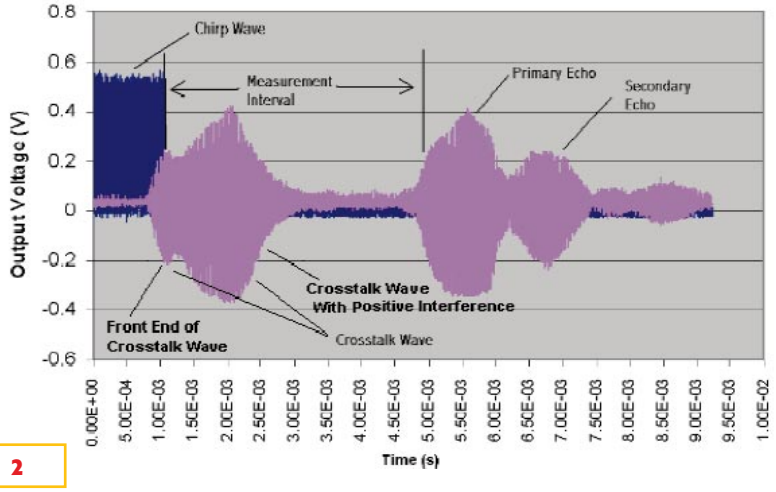
Figure 1



A fluid-level measurement system uses ultrasonic sonar principles.

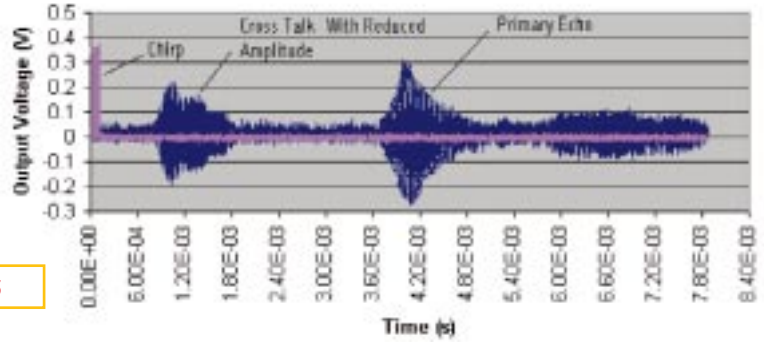
The COP8 µC measures the time it takes to propagate a wave from an arbitrary point on the surface of the fluid to the receiver. You can choose any arbitrary point; the µC can offset, or compensate for, the point with the aid of external data. The mechanical system in **Figure 1** has two major advantages. The first advantage is a cost savings in using two separate piezo elements. Piezo elements for only receivers and only transmitters are less expensive in the ensemble than a piezo element designed for both. The other advantage is the crude "mechanical diode" that the funnel tube forms. A high-intensity wave propagates from the tunnel, but the receiver recaptures only a small fraction of it. **Figure 2** shows a typical waveshape using Panasonic (www.panasonic.com) EFRTSB40KS and EFRRSB40KS piezo elements. Upon application of the

Figure 2



To make a measurement, the receiver must ignore the crosstalk wave and concentrate on the primary echo.

Figure 3



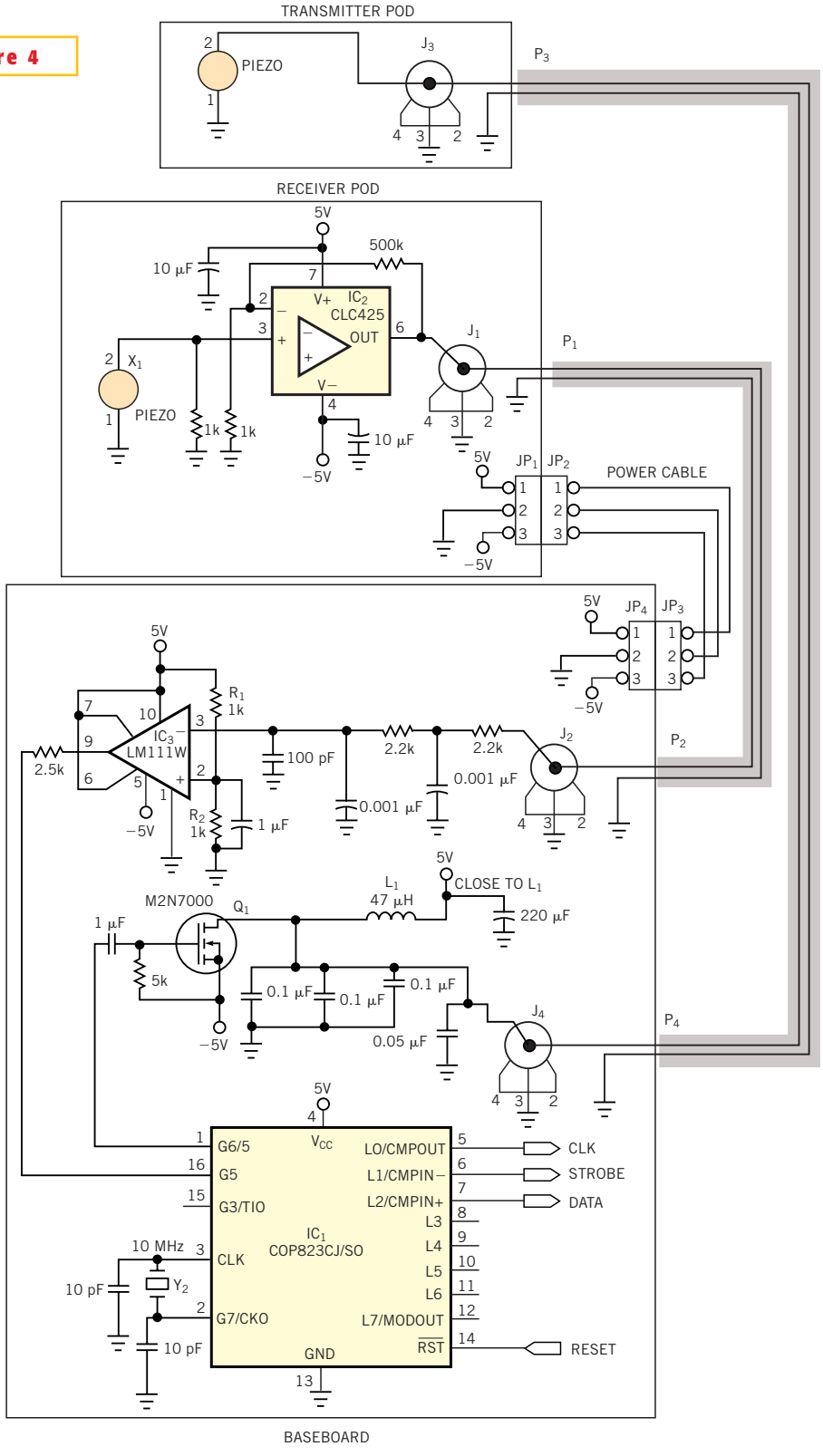
Some adjustments in the system produce a more distinct primary echo.

chirp wave, the receiver immediately detects the crosstalk wave. After an interval, the receiver detects the primary echo, followed closely by the secondary echo.

Reducing the amplitude of the crosstalk wave is convenient (**Figure 2**) This reduction allows shorter waveguide tubes, increasing the versatility of the design. One simple way of reducing crosstalk is to adjust the receiver's distance from the funnel tip, thus moving the receiver to an antinode. Another possible adjustment is to reduce the length of the chirp. **Figure 3** shows the acoustical waves after making the cited adjustments. In the circuit of **Figure 4**, the COP8, IC_1, pulses I/O port G5 at the piezo element's resonant frequency of approximately 40.3 kHz. This signal switches Q_1 and energizes the series-LC tank circuit, which has the same resonant frequency as the piezo element. This tank circuit boosts the voltage across the piezo element from 5 to 25V p-p. The receiver then detects and discards the crosstalk wave. After a short interval, the crosstalk vanishes, and the COP8 begins listening to the output of the comparator and begins counting program cycles and, thus, time.

When the echo reaches the piezo receiver X_1, IC_2 amplifies the echo 1000 times. The amplified signal then routes to the LM111 comparator, IC_3. The first echo component to reach the amplitude of the threshold set by R_1 and R_2 trips IC_3 to a logic one, and the COP8 stops counting. **Figure 5** illustrates this process. The COP8 starts listening at the rising edge of the trace labeled "COP8 Timed Interval," just after the crosstalk becomes silent. When the echo's amplitude crosses the comparator's trip voltage, the

Figure 4



The ultrasonic fluid-level measurement system uses standard, readily available components.

comparator's output switches high, and the COP8 stops timing. Armed with this timing data, converting the figures to a distance is trivial. One constraint is that the leading edge of the echo must occur after the disappearance of the crosstalk. This constraint demands an offset distance or an origin that meets the constraint. Assuming the constraint is satisfied, the distance is $d=V_{AIR}(t/2)$. The velocity of sound in air at room temperature is 345m/sec, or 0.345 mm/μsec. Solving for distance, d=0.172t mm, with t in microseconds.

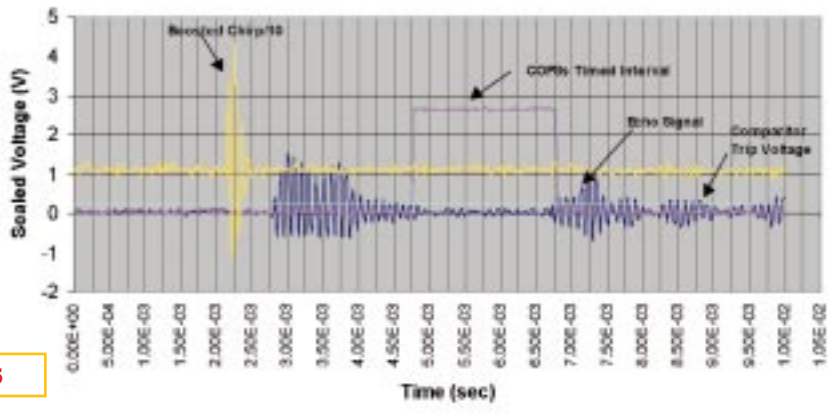


Figure 5

The COP8 doesn't start listening until its timed interval arrives after the disappearance of the crosstalk wave.

If you apply this distance to the waveform in **Figure 5**, the distance from the origin to the fluid's surface is 0.172 mm/μsec×(6750 μsec−4750 μsec)−=344 mm, or 13.54 in. The COP8 μC controls the fluid-level detector. Its first function in producing the waveform is to "chirp" the piezo transmitter. The μC uses its 16-bit programmable timer to perform this step. The timer's clock speed is the same as that of an instruction cycle, which is one-tenth of the oscillator speed (10 MHz). You set the appropriate timer control for PWM. This process produces a square wave of 40 kHz with 50% duty cycle. This figure represents the resonant frequency of the piezo elements (**Figure 5**). You should minimize the crosstalk because it is unusable for the measurement. The system should generate only three or four pulses to perform this step. More pulses create longer crosstalk and problems if the piezo receiver receives the crosstalk and primary echo at the same time. The timer in the μC starts and then experiences a short delay. During this delay, port G3 generates the square wave. The short delay limits the amount of pulses to the piezo transmitter.

While the waveform from the transmitter propagates down the tube, a delay ensures that the COP8 does not trigger during the crosstalk. The μC's timer characteristic then goes into input-capture mode. Because the LM111 has a common-emitter transistor output, the programming of port G2 uses the weak internal pullup, and then an interrupt occurs on a negative edge. At some predetermined time, the crosstalk is finished, and the timer starts and counts down until the interrupt occurs. When the negative edge arrives on the port pin, the results of the timer transfer to the upper and lower R1B. It remains on the port pin to convert the number in the R1B registers. Because the timer counts down, you need to subtract the number from the starting point to determine the actual time. The difference in fluid level determines whether you need a prescaler. Because the speed of the timer is 1 μsec, any value greater than 1 msec shows up as an over-range condition on the display. This example with a 2-ft change in fluid level uses a prescaler with a factor of four, meaning that the resolution decreases by a factor of four.

Once you determine the prescaler, you need to convert the data in the two 8-bit registers to a three-digit decimal equivalent for the three seven-segment LED displays. The conversion process is similar to counting. You set up three 8-bit registers and increment them each time the two 8-bit registers decrement. Consider the lower 8 bits of the hexadecimal number. Each time the lower 8-bit register reaches zero, the upper register decrements, and the lower bit begins at 0xFFh again. This process repeats until the hexadecimal registers equal zero. Each time a hexadecimal number decrements, a decimal-digit register increments. When the decimal-digit register reaches nine, the next decimal register increments, and so on. This operation produces three registers with a decimal-equivalent number.

The COP8 can then send the data to the display panel. You set the flags in the control register for microwire/plus serial I/O. This setting configures ports G4 and G5 as data out and clock, respectively. You configure ports G0 and G1 as output enable and strobe, respectively. You then use a look-up table to send the correct data to the display driver. The data loads into the serial-I/O register. The busy flag in the PSW register initiates the data transfer. The transfer continues at clock speed until all 8 bits complete the transfer. The process occurs for all three digits, starting with the least significant digit. You can download the assembly code for the COP8 from *EDN*'s Web site, www.ednmag.com. Click on "Search Databases," then enter the software center to download the file for Design Idea #2718. You can find additional information about the COP8 at www.national.com/cop8.

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