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DESIGNERS NOW HAVE NEW REASONS TO USE CERAMIC, RATHER THAN TANTALUM, CAPACITORS. BUT BE CAREFUL.

Ceramic capacitors in dc/dc-input filters: OK, but watch out for those transients

More and more portable devices now use ceramic capacitors for filtering of dc/dc-converter inputs. Ceramic capacitors offer the advantages of small size, low ESR (equivalent series resistance) and high rms-current capability. Recently, designers have found a different reason for considering ceramic capacitors for filtering—a shortage of tantalum capacitors.

Unfortunately, using ceramic capacitors for input filtering can cause problems. Applying a voltage step to a ceramic capacitor causes a large current surge that stores energy in the power-lead inductances. The transfer of this energy to the capacitor produces a voltage spike whose amplitude can easily exceed twice that of the original voltage step (**Figure 1**, **Table 1**).

The input-voltage-transient problem is related to the power-up sequence. First plugging the wall adapter into an ac outlet and powering it up and then, plugging the wall adapter output into a portable device can cause input-voltage transients that damage the dc/dc converters within the portable device.

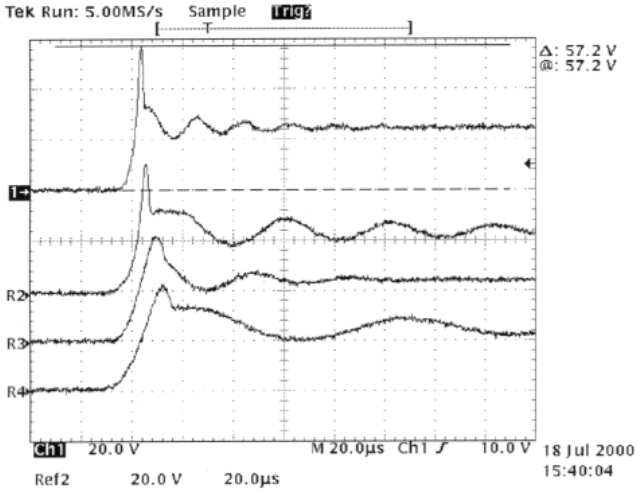
BUILDING THE TEST CIRCUIT

To illustrate the problem, we connected a typical laptop-computer dc/dc converter to a 24V wall adapter of the type used with laptop computers. The dc/dc converter was a synchronous buck converter that generates 3.3V from a 24V input.

Figure 2 shows the block diagram of the test setup, **Figure 3** shows a simplified equivalent circuit of the block diagram, and **Figure 4** provides a more detailed view of the dc/dc converter, including the synchronously switched-MOSFET output stage. The output capacitor in the wall adapter is usually on the order of 1000 µF. You can assume that the capacitor has ESR in the 10- to 30-mΩ range.

The equivalent circuit of **Figure 4** comprises an ideal voltage source, V_{IN}; an equivalent source resistance, R_{IN}, which includes lead and filter-inductor resistance; an ideal switch, S_1; an equivalent-lumped-circuit inductance, L_{EQ}; input capacitance, C_{IN}; and an equivalent lumped resistance, R_{EQ}.

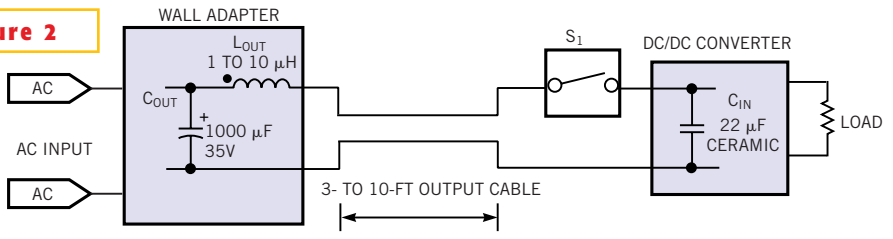
Figure 1



Input-voltage transients across ceramic capacitors at the input of dc/dc converters can easily exceed double the steady-state input voltage.

R_{IN}, L_{EQ}, C_{IN}, and R_{EQ} constitute a series-resonant tank. L_{EQ} includes all of the circuit's inductances, including the lead inductance, EMI-filter inductance, and the input capacitor (C_{IN})'s ESL (equivalent series inductance). R_{EQ} includes the ESR of the filter capacitor and also the lead resistance between the capacitor and the rest of the circuit. Note that the load connected to V_{OUT} is not present during the start-up transient because a typical dc/dc converter doesn't turn on and start to load V_{OUT} during the 50- to 100-µsec transient period.

Figure 2



This block diagram is typical of that of a system consisting of a wall adapter and a portable device, such as a laptop computer.

The input capacitor, C_{IN}, must be a low-ESR device that can carry the input-ripple current. In a typical laptop application, this capacitor has a value of 10 to 100 µF. The exact capacitor value depends on several factors, but the main requirement is its ability to handle the dc/dc converter's input-ripple current, which is usually 1 to 2A. Therefore, the appropriate capacitors are one 10- to 22-µF ceramic capacitor, two or three 22-µF tantalum capacitors, or one or two 22-µF OSCON (organic-semiconductive electrolyte) capacitors. **Table 2** compares the main parameters of these three types of capacitors. Note that the ripple-current rating for the selected 22-µF capacitor (Marcon/United Chemi-Con, THCR70-E1H266ZT) is rather conservative.

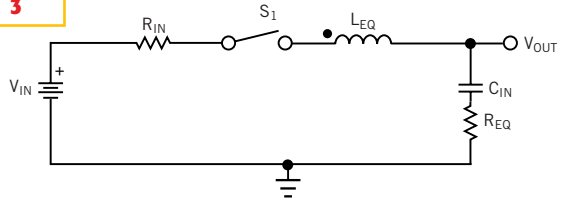
Power dissipation in a capacitor is: $P_{LOSS}=I_{RMS}^2 \cdot ESR$.

Based on the capacitor's ESR, the rated 2A ripple current dissipates only 40 mW in the selected Marcon device. This ripple current would dissipate 128 mW in the AVX TPS capacitor and 260 mW in the Sanyo OSCON capacitor.

TURNING ON THE SWITCH

When you turn **Figure 2**'s switch S_1 to the on position, the mayhem starts. Because the wall adapter is plugged in, 24V is present across its low-impedance output capacitor. On the other hand, the voltage across the input capacitor, C_{IN}, is 0V. The applied input voltage then starts driving current through L_{OUT}. C_{IN} starts charging, and the voltage across C_{IN} ramps up toward the 24V input. Once the voltage across C_{IN} reaches the wall adapter's output voltage, the energy in L_{OUT} raises the voltage across C_{IN} further above 24V. The voltage across C_{IN} eventually reaches its peak and then falls back to 24V. The voltage across C_{IN} may ring for some time around 24V. The actual waveform depends on the circuit-element values.

Figure 3



At start-up, the load on Figure 2's dc/dc converter is absent from the equivalent circuit because the converter does not immediately supply load power.

If you intend to simulate this circuit, keep in mind that the real circuit elements are seldom linear under transient conditions. For example, the capacitors may experience a change of capacitance. (Under rated input voltage, Y5V ceramic capacitors lose 80% of their initial capacitance, causing even higher peak voltages—$V=\sqrt{2W/C}$, where W is stored energy.) Also, the ESR of the input capacitors depends on the rise time of the waveform. Put another way, the ESR decreases with increasing frequency. **Figure 5a** shows the ESR versus frequency (and also the impedance versus frequency) of two values of Marcon's ceramic capacitors. **Figure 5b** provides the equivalent data for four values of Oscon capacitors. The inductance of the EMI-suppression inductors can also drop during transients because of the magnetic material's saturation.

TESTING A PORTABLE APPLICATION

We tested the input-voltage transients with typical values of C_{IN} and with output-filter-inductor (L_{OUT}) values typical

TABLE 1—PEAK VOLTAGES OF WAVEFORMS IN FIGURE 1

Trace	L_{OUT} (µH)	C_{IN} (µF)	V_{IN} peak (V)
Ch1	1	10	57.2
R2	10	10	50
R3	1	22	41
R4	10	22	41

TABLE 2—COMPARISON OF THREE TYPES OF CAPACITORS

Capacitor type and manufacturer	Capacitance (µF)	Rated voltage (V)	Ripple current (A)	ESR at 100 kHz (mΩ)
Marcon THCR, Y5U ceramic	22	50	2 at 85°C	10
AVX TPS, tantalum 22	35	0.8 at 85°C	200	
Sanyo OSCON*, 30SC22M	22	30	1.8 at 45°C	80

*OSCON: Solid-electrolytic capacitor with organic-semiconductive electrolyte

of those in wall adapters used in laptop applications. **Figure 1** shows input-voltage transients for C_{IN} values of 10 and 22 µF with wall-adapter L_{OUT} values of 1 and 10 µH.

The top waveform shows the worst-case transient with a 10-µF capacitor and 1-µH inductor. With a 24V-dc input, the voltage across C_{IN} peaks at 57.2V. The dc/dc converter may not survive repeated exposure to 57.2V.

The waveform with 10 µF and 10 µH (trace/R2). looks a bit better. The peak is still approximately 50V. The flat part of the waveform following the peak indicates that the synchronous MOSFET, Q1, is avalanching and dissipating some of the energy. Traces R3 and R4 peak at approximately 41V and are for a 22-µF capacitor and 1- and 10-µH inductors.

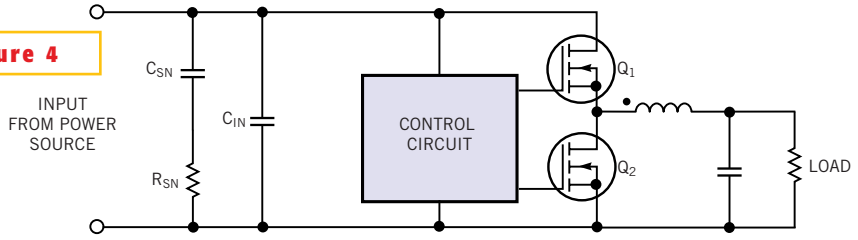
The peak voltage should increase with increasing inductance, and it should decrease with increasing inductor resistance. In the waveforms of **Figure 1**, the peak of R2 is lower than the peak of Ch1 because of the load circuit's clamping action. If you take a closer look at R2, the voltage would have kept increasing were it not for the load MOSFET's (Q1's)sudden clamping at 30V.

The same thing appears to happen in traces R3 and R4. However, because of the slower rise time and the higher resistance of the 10-µH inductor, the two waveforms peak at the same voltage. Once again, you can see the clamping of the MOSFETs cutting back the peak voltage in R4.

The waveforms of **Figure 6** show what happens when you use a relatively linear capacitor (R1: X5R dielectric) and a strongly nonlinear capacitor (R2: Y5U dielectric). The bias voltage across the two 10-µF capacitors was 0V. In a lossless linear circuit, the peak voltage would reach $2 \cdot V_{IN}$. With losses, the peak voltage is less than $2 \cdot V_{IN}$ (in R1, VPEAK= $1.5 \cdot V_{IN}$).

When we applied a bias voltage to the Y5U capacitor in R2, the capacitance decreased and the slew rate increased, resulting in an increase of the filter circuit's resonant frequency. Also, you can see the effect of the decreased capacitance on the peak voltage. With the nonlinear Y5V capacitor, the peak voltage reaches $3 \cdot V_{IN}$, showing the effect of the significantly

Figure 4

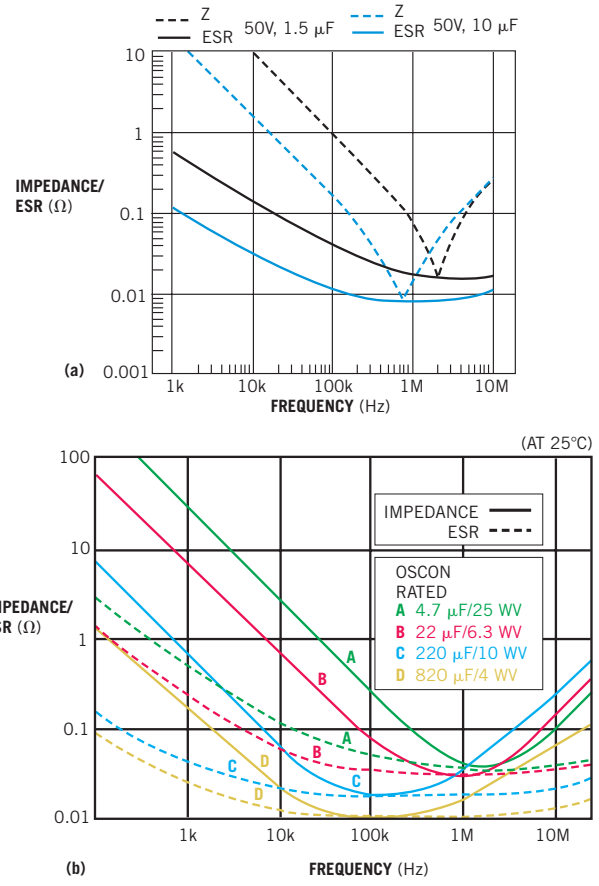


A properly designed transient-snubber network (R_{SN}, C_{SN}) is the key to eliminating transients that can destroy the components in the dc/dc converter.

TABLE 3–PEAK VOLTAGES OF WAVEFORMS IN FIGURE 7

Trace	C_{IN} (µF)	Capacitor type	V_{IN} peak (V)
R1	22	Ceramic	40.8
R2	22	Ceramic with 30V TVS	32
R3	22	AVX TPS tantalum	33
R4	22	Sanyo OSCON	35

Figure 5



The curves show the ESR and impedance magnitude versus frequency of several values of Marcon (a) and OSCON capacitors (b).

lower capacitance at the higher bias voltage.

INPUT-VOLTAGE TRANSIENTS

Different types of input capacitors produce different transient-voltage waveforms (**Figure 7**, **Table 3**). The top trace (R1) the reference waveform for 22 µF and 1 µH; it peaks at 40.8V.

Waveform R2 in **Figure 7** shows what happens when you add a transient-voltage suppressor across the input. The input-voltage transient is clamped but not eliminated. It is difficult to set the voltage suppressor's breakdown voltage low enough to protect the dc/dc converter and far enough from the operating dc level of the input source (24V). This design uses a P6KE30A transient-voltage suppressor that is too close to starting to conduct at 24V. Unfortunately, using a transient-voltage suppressor with a higher voltage rating would not provide a sufficiently low clamping voltage.

This example obtained waveforms R3 and R4 by using a 22-µF, 35V AVX TPS-type tantalum capacitor and a 22-µF, 30V Sanyo OSCON capacitor. These two capacitors bring the transients to manageable levels. However, these capacitors are bigger than the ceramic capacitors, and you need more than one capacitor to meet the input-ripple-current requirements.

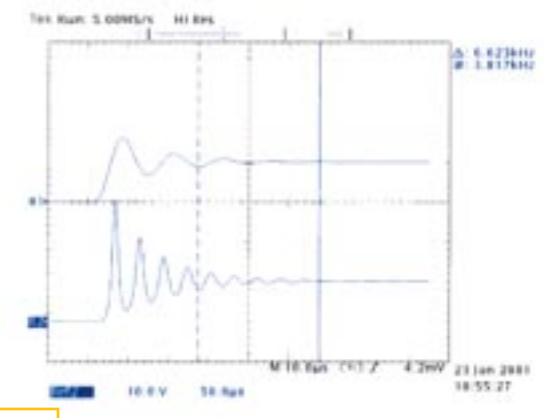


Figure 6

The amplitude and ringing frequency of a dc/dc converter's input-voltage transients depend on the characteristics of the input capacitor's ceramic dielectric material. With the nonlinear material (lower trace), voltage bias on the capacitor decreases the capacitance, increasing both the transient amplitude and the ringing frequency.

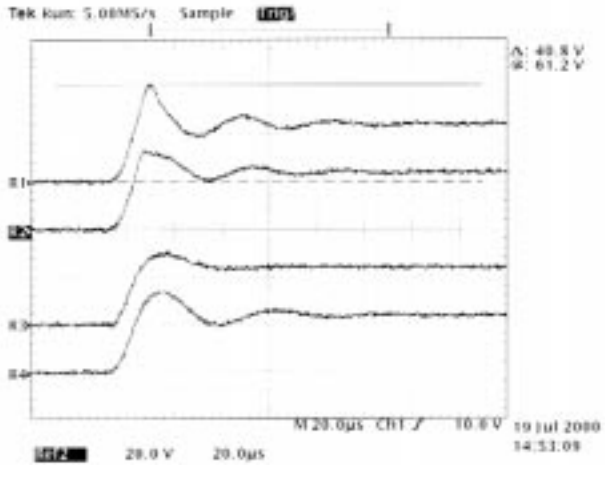


Figure 7

Changing the value and type of the input-filter capacitor profoundly affects the transient amplitude.

OPTIMIZING INPUT CAPACITORS

In **Figure 8** and **Table 4**, you can see that the input transients vary with the type of input capacitors used. To optimize the input capacitors, you need to understand what happens during transients. Just as in an ordinary resonant RLC circuit, the circuit can be underdamped, critically damped, or overdamped. To minimize the size of the input-filter circuit, you need to use an underdamped resonant tank. However, you want a critically damped circuit because its output rises nicely to the input voltage without voltage overshoots or ringing.

To keep the input-filter design small, you would like to use ceramic capacitors because of their high ripple current ratings and low ESR. To start the design, you must first determine the minimum value of the input capacitor. In this example, a 22-µF, 35V ceramic capacitor should be sufficient. The top trace of **Figure 8** shows the input transients generated with this capacitor. Clearly, you will have a problem if you use components that are rated for only 30V.

Now, try to damp the input circuit to obtain the optimum transient characteristic. Waveform R2 shows what happens when you add another 22-µF ceramic capacitor with a 0.5Ω resistor in series (**Figure 4**). The input-voltage transient now nicely levels off at 30V.

You can also achieve damping by adding a capacitor of a type that already has ESR on the order of 0.5Ω. Waveform R3 shows the transient response when you add an AVX 22-µF, 35V TPS-type tantalum capacitor across the input. For comparison, waveform R4 once again shows the input-voltage transient with a 30V transient-voltage suppressor.

Finally, the bottom trace (Ch1) of **Figure 8** shows an ideal waveform. It also turns out that the circuit that produced this waveform represents the least expensive approach. The circuit uses a 47-µF, 35V aluminum electrolytic capacitor from Sanyo (35CV47AXA). In conjunction with the 1-µH inductor, this capacitor has just the right values of capacitance and ESR to provide critical damping of the 22-µF ceramic capacitor.

TABLE 4–PEAK VOLTAGES OF WAVEFORMS IN FIGURE 8 WITH 22-µF INPUT CERAMIC CAPACITOR AND ADDED SNUBBER

Trace	Snubber Type	V_{IN} peak (V)
R1	None	40.8
R2	22-µF, ceramic +0.5Ω in series	30
R3	22-µF, tantalum, AVX, TPS series	33
R4	30V TVS, P6KE30A	35
Ch1	47-µF, 35V aluminum electrolytic capacitor	25

The 35CV47AXA exhibits an ESR value of 0.44Ω and an rms current rating of 230 mA. In an application with 1 to 2A of rms ripple current, you clearly can't use this capacitor alone without the 22-µF ceramic capacitor. Also, the 35CV47AXA measures just 6.3×6 mm.

Other approaches would have been more expensive and would have required more parts. In an attempt to minimize space and cost, you could add one 22-µF capacitor to the second-best circuit. However, to obtain the same results, you would have had to add two 22-µF capacitors and a resistor, R_{SN}. Ceramic-capacitors cost 50 cents to 80 cents, whereas aluminum-electrolytic capacitors cost only 10 cents to 20 cents. Therefore, the second-best approach costs at least four times as much as the best approach

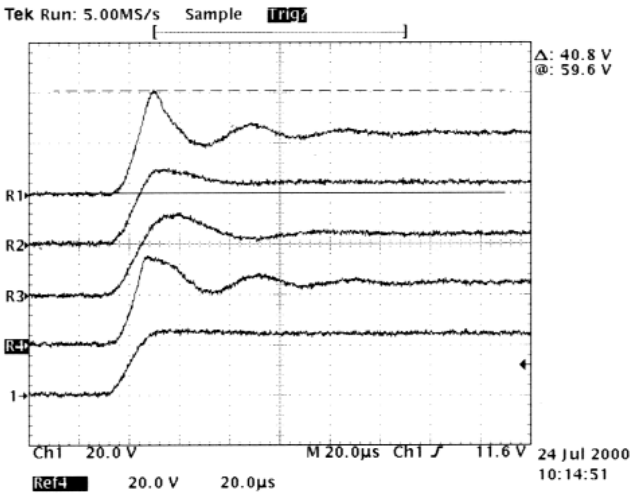


Figure 8

The bottom trace shows that a properly designed snubber network completely eliminates transients at the dc/dc converter's input.

You should pay attention to input-voltage transients in dc/dc converters. Simple designs for preventing these transients can be effective. A good design minimizes both cost and size without compromising performance.□

AUTHOR'S BIOGRAPHY

Goran Perica is an applications engineer at Linear Technology Corp, where he has worked for three years. In his current position, he designs power-conversion circuits for the telecommunication, computer, and industrial markets. He has a master's degree in electrical engineering from the University of Ljublana, Slovenia. His spare-time pursuits include enjoying music and hiking with his wife and two ex-racing greyhounds.