# AN535
**Application Note**

# Phase-Locked Loop Design Fundamentals

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*The fundamental design concepts for phase-locked loops implemented with integrated circuits are outlined. The necessary equations required to evaluate the basic loop performance are given in conjunction with a brief design example.*

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# Phase-Locked Loop Design Fundamentals

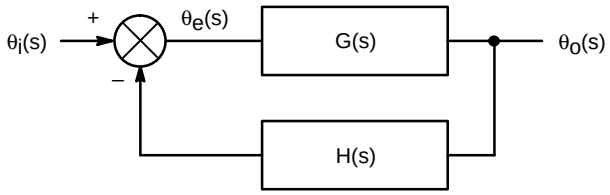
## Introduction

The purpose of this application note is to provide the electronic system designer with the necessary tools to design and evaluate Phase-Locked Loops (PLL) configured with integrated circuits. The majority of all PLL design problems can be approached using the Laplace Transform technique. Therefore, a brief review of Laplace is included to establish a common reference with the reader. Since the scope of this article is practical in nature all theoretical derivations have been omitted, hoping to simplify and clarify the content. A bibliography is included for those who desire to pursue the theoretical aspect.

## Parameter Definition

The Laplace Transform permits the representation of the time response f(t) of a system in the complex domain F(s). This response is twofold in nature in that it contains both transient and steady state solutions. Thus, all operating conditions are considered and evaluated. The Laplace transform is valid only for positive real time linear parameters; thus, its use must be justified for the PLL which includes both linear and nonlinear functions. This justification is presented in Chapter Three of Phase Lock Techniques by Gardner.[1]

The parameters in Figure 1 are defined and will be used throughout the text.




$\theta_i(s)$ Phase Input
$\theta_e(s)$ Phase Error
$\theta_o(s)$ Output Phase
G(s) Product of the Individual Feed Forward Transfer Functions
H(s) Product of the Individual Feedback Transfer Functions

**Figure 1. Feedback System**

Using servo theory, the following relationships can be obtained.[2]

$$\theta_e(s) = \frac{1}{1 + G(s)\ H(s)}\ \theta_i(s) \qquad (1)$$

$$\theta_o(s) = \frac{G(s)}{1 + G(s)\ H(s)}\ \theta_i(s) \qquad (2)$$

These parameters relate to the functions of a PLL as shown in Figure 2.

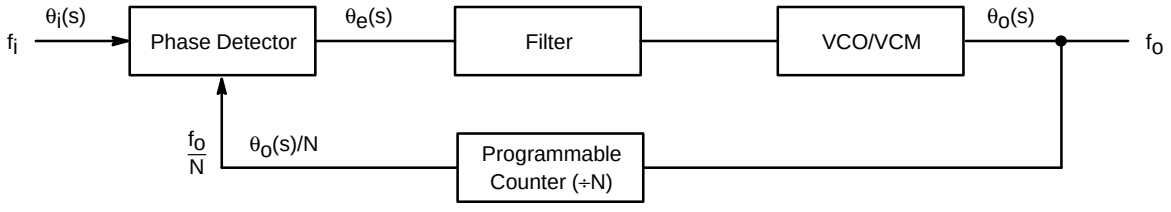



**Figure 2. Phase Locked Loop**

The phase detector produces a voltage proportional to the phase difference between the signals $\theta_i$ and $\theta_o/N$. This voltage upon filtering is used as the control signal for the VCO/VCM (VCM – Voltage Controlled Multivibrator).

Since the VCO/VCM produces a frequency proportional to its input voltage, any time variant signal appearing on the control signal will frequency modulate the VCO/VCM. The output frequency is

$$f_o = N\ fi \qquad (3)$$

during phase lock. The phase detector, filter, and VCO/VCM compose the feed forward path with the feedback path containing the programmable divider. Removal of the programmable counter produces unity gain in the feedback path (N = 1). As a result, the output frequency is then equal to that of the input.

Various types and orders of loops can be constructed depending upon the configuration of the overall loop transfer function. Identification and examples of these loops are contained in the following two sections.

## Type — Order

These two terms are used somewhat indiscriminately in published literature, and to date there has not been an established standard. However, the most common usage will be identified and used in this article.

The **type** of a system refers to the number of poles of the loop transfer function G(s) H(s) located at the origin. Example:

$$\text{let} \qquad G(s)\ H(s) = \frac{10}{s(s + 10)} \qquad (4)$$

This is a *type one* system since there is only one pole at the origin.

The **order** of a system refers to the highest degree of the polynomial expression

$$1 + G(s)\ H(s) = 0 \triangleq \text{C.E.} \qquad (5)$$

which is termed the **Characteristic Equation** (C.E.). The roots of the characteristic equation become the closed loop poles of the overall transfer function.

Example:

$$G(s)\ H(s) = \frac{10}{s(s + 10)} \qquad (6)$$

then

$$1 + G(s)\ H(s) = 1 + \frac{10}{s(s + 10)} = 0 \qquad (7)$$

therefore

$$\text{C.E.} = s(s + 10) + 10 \qquad (8)$$

$$\text{C.E.} = s^2 + 10s + 10 \qquad (9)$$

which is a *second order* polynomial. Thus, for the given G(s) H(s), we obtain a type 1 second order system.

## Error Constants

Various inputs can be applied to a system. Typically, these include step position, velocity, and acceleration. The response of type 1, 2, and 3 systems will be examined with the various inputs.

$\theta_e(s)$ represents the phase error that exists in the phase detector between the incoming reference signal $\theta_i(s)$ and the feedback $\theta_o(s)/N$. In evaluating a system, $\theta_e(s)$ must be examined in order to determine if the steady state and transient characteristics are optimum and/or satisfactory. The transient response is a function of loop stability and is covered in the next section. The steady state evaluation can be simplified with the use of the final value theorem associated with Laplace. This theorem permits finding the steady state system error $\theta_e(s)$ resulting from the input $\theta_i(s)$ without transforming back to the time domain.[3]

Simply stated

$$\lim_{t \to \infty} [\theta(t)] = \lim_{s \to o} [s\theta_e(s)] \qquad (10)$$

Where

$$\theta_e(s) = \frac{1}{1 + G(s)\ H(s)}\ \theta_i(s) \qquad (11)$$

The input signal $\theta_i(s)$ is characterized as follows:

$$\text{Step position:}\ \ \theta_i(t) = C_p \quad t \geq 0 \qquad (12)$$

$$\text{Or, in Laplace notation:}\ \ \theta_i(s) = \frac{C_p}{s} \qquad (13)$$

where $C_p$ is the magnitude of the phase step in radians. This corresponds to shifting the phase of the incoming reference signal by $C_p$ radians:

$$\text{Step velocity:}\ \ \theta_i(t) = C_v t \quad t \geq 0 \qquad (14)$$

$$\text{Or, in Laplace notation:}\ \ \theta_i(s) = \frac{C_v}{s^2} \qquad (15)$$

where $C_v$ is the magnitude of the rate of change of phase in radians per second. This corresponds to inputting a frequency that is different than the feedback portion of the VCO frequency. Thus, $C_v$ is the frequency difference in radians per second seen at the phase detector.

$$\text{Step acceleration:}\ \ \theta_i(t) = C_a t^2 \quad t \geq 0 \qquad (16)$$

$$\text{Or, in Laplace notation:}\ \ \theta_i(s) = \frac{2\ C_a}{s^3} \qquad (17)$$

$C_a$ is the magnitude of the frequency rate of change in radians per second per second. This is characterized by a time variant frequency input.

Typical loop G(s) H(s) transfer functions for types 1, 2, and 3 are:

$$\text{Type 1} \qquad G(s)\ H(s) = \frac{K}{s(s + a)} \qquad (18)$$

Type 2 $$G(s)\ H(s) = \frac{K(s + a)}{s^2} \quad (19)$$

Type 3 $$G(s)\ H(s) = \frac{K(s + a)(s + b)}{s^3} \quad (20)$$

The final value of the phase error for a type 1 system with a step phase input is found by using Equations 11 and 13.

$$\theta_e(s) = \left(\frac{1}{1 + \frac{K}{s(s+a)}}\right)\left(\frac{C_p}{s}\right)$$

$$= \frac{(s + a)C_p}{(s^2 + as + K)} \quad (21)$$

$$\theta_e(t = \infty) = \lim_{s \to o}\left[s\left(\frac{s + a}{s^2 + as + K}\right) C_p\right] = 0 \quad (22)$$

Thus, the final value of the phase error is zero when a step position (phase) is applied.

Similarly, applying the three inputs into type 1, 2, and 3 systems and utilizing the final value theorem, the following table can be constructed showing the respective steady state phase errors.

**Table 1. Steady State Phase Errors for Various System Types**

| | Type 1 | Type 2 | Type 3 |
|---|---|---|---|
| Step Position | Zero | Zero | Zero |
| Step Velocity | Constant | Zero | Zero |
| Step Acceleration | Continually Increasing | Constant | Zero |

A zero phase error identifies phase coherence between the two input signals at the phase detector.

A constant phase error identifies a phase differential between the two input signals at the phase detector. The magnitude of this differential phase error is proportional to the loop gain and the magnitude of the input step.

A continually increasing phase error identifies a time rate change of phase. This is an unlocked condition for the phase loop.

Using Table 1, the system type can be determined for specific inputs. For instance, if it is desired for a PLL to track a reference frequency (step velocity) with zero phase error, a minimum of type 2 is required.

## Stability

The root locus technique of determining the position of system poles and zeroes in the s-plane is often used to graphically visualize the system stability. The graph or plot illustrates how the closed loop poles (roots of the characteristic equation) vary with loop gain. For stability, all poles must lie in the left half of the s-plane. The relationship of the system poles and zeroes then determine the degree of stability. The root locus contour can be determined by using the following guidelines.[2]

Rule 1 – The root locus begins at the poles of G(s) H(s) (K = 0) and ends at the zeroes of G(s) H(s) (K = ∞), where K is loop gain.

Rule 2 – The number of root loci branches is equal to the number of poles or number of zeroes, whichever is greater. The number of zeroes at infinity is the difference between the number of finite poles and finite zeroes of G(s) H(s).

Rule 3 – The root locus contour is bounded by asymptotes whose angular position is given by:

$$\frac{(2n + 1)}{\#P - \#Z}\ \pi;\ n = 0, 1, 2, \ldots \quad (23)$$

Where #P (#Z) is the number of poles (zeroes).

Rule 4 – The intersection of the asymptotes is positioned at the center of gravity C.G.:

$$C.G. = \frac{\Sigma P - \Sigma Z}{\#P - \#Z} \quad (24)$$

Where ΣP (ΣZ) denotes the summation of the poles (zeroes).

Rule 5 – On a given section of the real axis, root loci may be found in the section only if the #P + #Z to the right is odd.

Rule 6 – Breakaway points from negative real axis is given by:

$$\frac{dK}{ds} = 0 \quad (25)$$

Again, where K is the loop gain variable factored from the characteristic equation.

Example:

The root locus for a typical loop transfer function is found as follows:

$$G(s)\ H(s) = \frac{K}{s(s + 4)} \quad (26)$$

The root locus has two branches (Rule 2) which begin at s = 0 and s = –4 and ends at the two zeroes located at infinity (Rule 1). The asymptotes can be found according to Rule 3. Since there are two poles and no zeroes, the equation becomes:

$$\frac{2n + 1}{2}\ \pi = \begin{cases} \frac{\pi}{2} & \text{for } n = 0 \\ \frac{3\pi}{2} & \text{for } n = 1 \end{cases} \quad (27)$$

The position of the intersection according to the Rule 4 is:

$$s = \frac{\Sigma P - \Sigma Z}{\#P - \#Z} = \frac{(-4 - 0) - (0)}{2 - 0}$$

$$s = -2 \qquad (28)$$

The breakaway point, as defined by Rule 6, can be found by first writing the characteristic equation.

$$C.E. = 1 + G(s)\,H(s) = 0$$

$$= 1 + \frac{K}{s(s+4)} = s^2 + 4s + K = 0 \qquad (29)$$

Now solving for K yields

$$K = -s^2 - 4s \qquad (30)$$

Taking the derivative with respect to s and setting it equal to zero, then determines the breakaway point.

$$\frac{dK}{ds} = \frac{d}{ds}(-s^2 - 4s) \qquad (31)$$

$$\frac{dK}{ds} = -2s - 4 = 0 \qquad (32)$$

or

$$s = -2 \qquad (33)$$

is the point of departure. Using this information, the root locus can be plotted as in Figure 3.

The second order characteristic equation, given by Equation 29, has be normalized to a standard form[2]

$$s^2 + 2\zeta\omega_n s + \omega^2_n \qquad (34)$$

where the damping ratio $\xi = \cos\phi$ ($0° \le \phi \le 90°$) and $\omega_n$ is the natural frequency as shown in Figure 3.

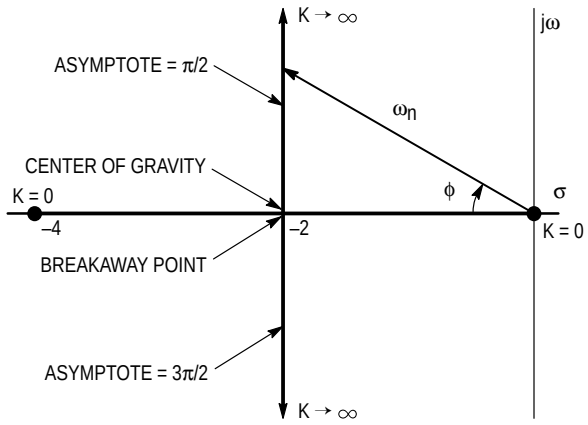



**Figure 3. Type 1 Second Order Root Locus Contour**

The response of this type 1, second order system to a step input, is shown in Figure 4. These curves represent the phase response to a step position (phase) input for various damping ratios. The output frequency response as a function of time to a step velocity (frequency) input is also characterized by the same set of figures.

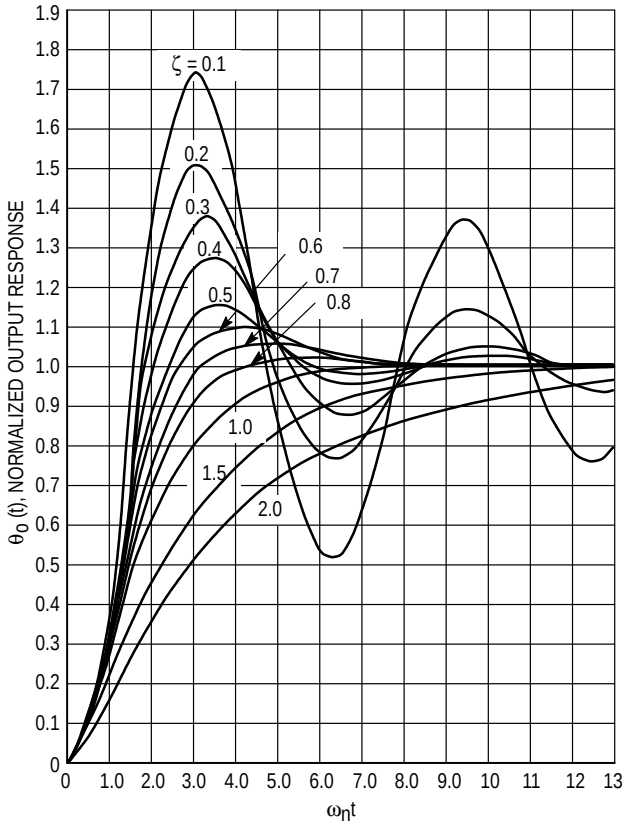



**Figure 4. Type 1 Second Order Step Response**

The overshoot and stability as a function of the damping ratio $\xi$ is illustrated by the various plots. Each response is plotted as a function of the normalized time $\omega_n t$. For a given $\xi$ and a lock-up time t, the $\omega_n$ required to achieve the desired results can be determined. Example:

Assume $\xi = 0.5$
error < 10%
for t > 1ms

From $\xi = 0.5$ curve error is less than 10% of final value for all time greater than $\omega_n t = 4.5$. The required $\omega_n$ can then be found by:

$$\omega_n t = 4.5 \qquad (35)$$

or

$$\omega_n = \frac{4.5}{t} = \frac{4.5}{0.001} = 4.5\text{krad/s} \qquad (36)$$

$\xi$ is typically selected between 0.5 and 1 to yield optimum overshoot and noise performance.

Example:

Another common loop transfer function takes the form:

$$G(s)\ H(s) = \frac{(s + a)k}{s^2} \qquad (37)$$

This is a type 2 second order system. A zero is added to provide stability. (Without the zero, the poles would move along the $j\omega$ axis as a function of gain and the system would at all times be oscillatory in nature.) The root locus shown in Figure 5 has two branches beginning at the origin with one asymptote located at 180 degrees. The center of gravity is s = a; however, with only one asymptote, there is no intersection at this point. The root locus lies on a circle centered at s = –a and continues on all portions of the negative real axis to left of the zero. The breakaway point is s = –2a.

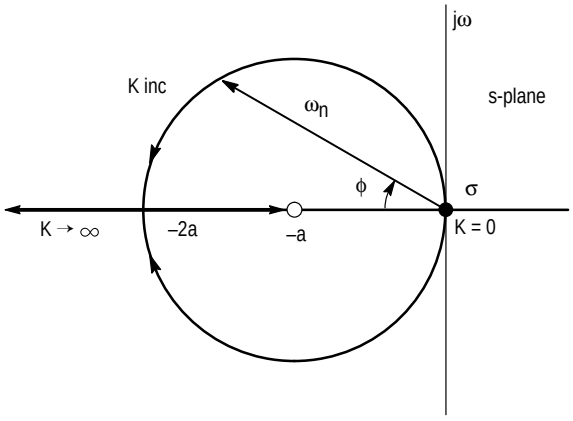



**Figure 5. Type 2 Second Order Root Locus Contour**

The respective phase or output frequency response of this type 2 second order system to a step position (phase) or velocity (frequency) input is shown in Figure 6. As illustrated in the previous example, the required $\omega_n$ can be determined by the use of the graph when $\xi$ and the lock-up time are given.

## Bandwidth

The –3dB bandwidth of the PLL is given by:

$$\omega - 3dB = \omega_n\left(1 - 2\zeta^2 + \sqrt{2 - 4\zeta^2 + 4\zeta^4}\right)^{1/2} \qquad (38)$$

for a type 1 second order[4] system, and by:

$$\omega_{-3dB} = \omega_n\left(1 + 2\zeta^2 + \sqrt{2 + 4\zeta^2 + 4\zeta^4}\right)^{1/2} \qquad (39)$$

for a type 2 second order[1] system.

## Phase-Locked Loop Design Example

The design of a PLL typically involves determining the type of loop required, selecting the proper bandwidth, and establishing the desired stability. A fundamental approach to

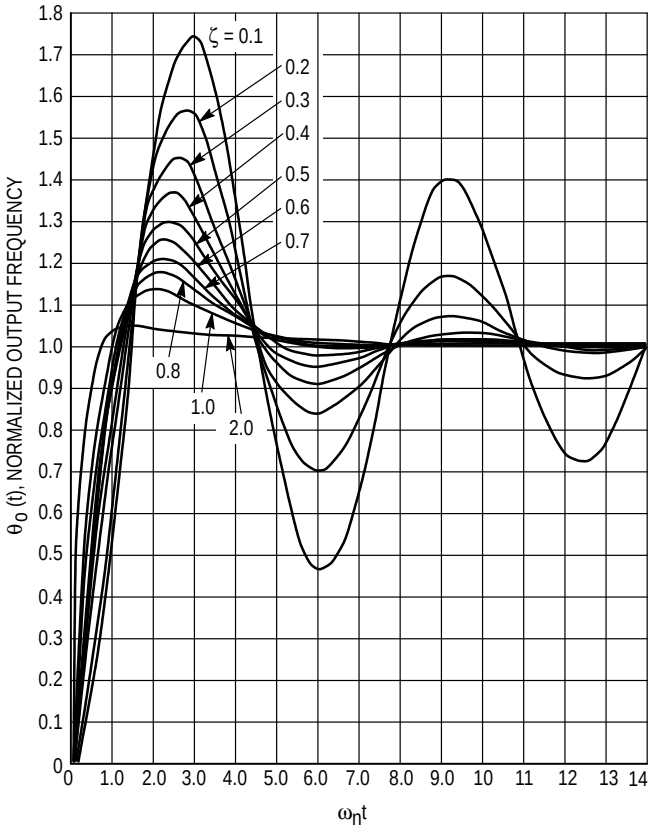



**Figure 6. Type 2 Second Order Step Response**

these design constraints is now illustrated. It is desired for the system to have the following specifications:

| | |
|---|---|
| Output Frequency | 2.0MHz to 3.0MHz |
| Frequency Steps | 100KHz |
| Phase Coherent Frequency Output | — |
| Lock-Up Time Between Channels | 1ms |
| Overshoot | <20% |

NOTE: These specifications characterize a system function similar to a variable time base generator or a frequency synthesizer

From the given specifications, the circuit parameters shown in Figure 7 can now be determined.

The devices used to configure the PLL are:

| | |
|---|---|
| Frequency-Phase Detector | MC4044/4344 |
| Voltage Controlled Multivibrator (VCM) | MC4024/4324 |
| Programmable Counter | MC4016/4316 |

The forward and feedback transfer functions are given by:

$$G(s) = K_p\ K_f\ K_o \qquad H(s) = K_n \qquad (40)$$

where $K_n = 1/N$ (41)

The programmable counter divide ratio $K_n$ can be found from Equation 3.

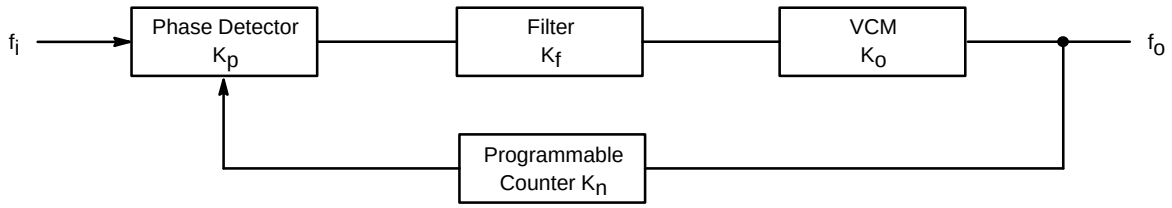



**Figure 7. Phase-Locked Loop Circuit Parameters**

$$N_{min} = \frac{f_{o\,min}}{f_i} = \frac{f_{o\,min}}{f_{step}} = \frac{2MHz}{100KHz} = 20 \qquad (42)$$

$$N_{max} = \frac{f_{o\,max}}{f_{step}} = \frac{3MHz}{100KHz} = 30 \qquad (43)$$

$$K_n = \frac{1}{20} \text{ to } \frac{1}{30} \qquad (44)$$

A type 2 system is required to produce a phase coherent output relative to the input (See Table 1). The root locus contour is shown in Figure 5 and the system step response is illustrated by Figure 6.

The operating range of the MC4024/4324 VCM must cover 2MHz to 3MHz. Selecting the VCM control capacitor according to the rules contained on the data sheet yields C = 100pF. The desired operating range is then centered within the total range of the device. The input voltage versus output frequency is shown in Figure 8.

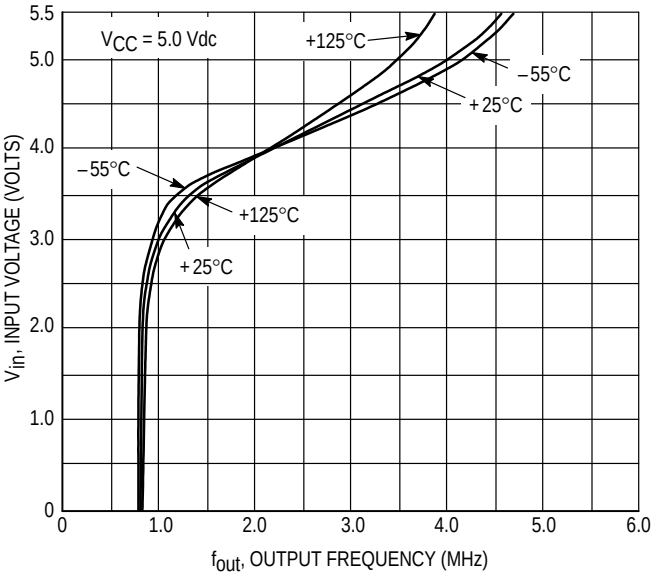



**Figure 8. MC4324 Input Voltage versus Output Frequency** (100pF Feedback Capacitor)

The transfer function of the VCM is given by:

$$K_o = \frac{K_v}{s} \qquad (45)$$

Where $K_v$ is the sensitivity in radians per second per volt. From the curve in Figure 8, $K_v$ is found by taking the reciprocal of the slope.

$$K_v = \frac{4MHz - 1.5MHz}{5V - 3.6V}\ 2\pi \text{ rad/s/V}$$

$$K_v = 11.2 \times 10^6 \text{ rad/s/V} \qquad (46)$$

Thus

$$K_o = \frac{11.2 \times 10^6}{s} \text{ rad/s/V} \qquad (47)$$

The s in the denominator converts the frequency characteristics of the VCM to phase, i.e., phase is the integral of frequency.

The gain constant for the MC4044/4344 phase detector is found by[5]

$$K_p = \frac{DFHigh - UFLow}{2(2\pi)} = \frac{2.3V - 0.9V}{4\pi} = 0.111V/rad \qquad (48)$$

Since a type 2 system is required (phase coherent output) the loop transfer function must take the form of Equation 19. The parameters thus far determined include $K_p$, $K_o$, $K_n$ leaving only $K_f$ as the variable for design. Writing the loop transfer function and relating it to Equation 19

$$G(s)H(s) = \frac{K_p\ K_v\ K_n\ K_f}{s} = \frac{K(s + a)}{s^2} \qquad (49)$$

Thus, $K_f$ must take the form

$$K_f = \frac{s + a}{s} \qquad (50)$$

in order to provide all of the necessary poles and zeroes for the required G(s) H(s). The circuit shown in Figure 9 yields the desired results.

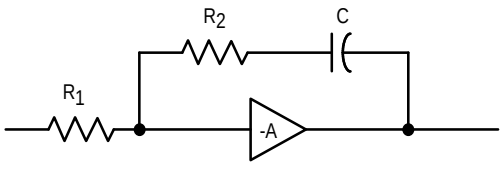



**Figure 9. Active Filter Design**

$K_f$ is expressed by

$$K_f = \frac{R_2Cs + 1}{R_1Cs} \text{ for large} A \qquad (51)$$

where A is voltage gain of the amplifier.

$R_1$, $R_2$, and C are then the variables used to establish the overall loop characteristics.

The MC4044/4344 provides the active circuitry required to configure the filter $K_f$. An additional low current high β buffering device or FET can be used to boost the input impedance, thus minimizing the leakage current from the capacitor C between sample updates. As a result, longer sample periods are achievable.

Since the gain of the active filter circuitry in the MC4044/4344 is not infinite, a gain correction factor $K_c$ must be applied to $K_f$ in order to properly characterize the function. $K_c$ is found experimentally to be $K_c = 0.5$.

$$K_{fc} = K_f K_c = 0.5 \left(\frac{R_2Cs + 1}{R_1Cs}\right) \qquad (52)$$

(For large gain, Equation 51 applies.)

The PLL circuit diagram is shown in Figure 11 and its Laplace representation in Figure 10.

The loop transfer function is

$$G(s)\,H(s) = K_p K_{fc} K_o K_n \qquad (53)$$

$$G(s)H(s) = K_p(0.5) \left(\frac{R_2Cs + 1}{R_1Cs}\right) \left(\frac{K_v}{s}\right) \left(\frac{1}{N}\right) \qquad (54)$$

The characteristic equation takes the form

$$C.E. = 1 + G(s)\,H(s) = 0$$

$$= s^2 + \frac{0.5\,K_p\,K_v\,R_2}{R_1N}s + \frac{0.5\,K_p\,K_v}{R_1CN} \qquad (55)$$

Relating Equation 55 to the standard form given by Equation 34

$$s^2 + \frac{0.5\,K_p\,K_v\,R_2}{R_1N}s + \frac{0.5\,K_p\,K_v}{R_1CN}$$

$$= s^2 + 2\zeta\omega_n s + \omega_n^2 \qquad (56)$$

Equating like coefficients yields

$$\frac{0.5\,K_p\,K_v}{R_1CN} = \omega_n^2 \qquad (57)$$

$$\text{and} \quad \frac{0.5\,K_p\,K_v\,R_2}{R_1N} = 2\zeta\omega_n \qquad (58)$$

With the use of an active filter whose open loop gain (A) is large ($K_c = 1$), Equations 57 and 58 become

$$\frac{K_p\,K_v}{R_1CN} = \omega_n^2 \qquad (59)$$

$$\frac{K_p\,K_v\,R_2}{R_1N} = 2\zeta\omega_n \qquad (60)$$

The percent overshoot and settling time are now used to determine $\omega_n$. From Figure 6, it is seen that a damping ratio $\zeta = 0.8$ will produce a peak overshoot less than 20% and will settle within 5% at $\omega_n t = 4.5$. The required lock-up time is 1ms.

$$\omega_n = \frac{4.5}{t} = \frac{4.5}{0.001} = 4.5\text{krad/s} \qquad (61)$$

Rewriting Equation 57

$$R_1C = \frac{0.5\,K_p\,K_v}{\omega_n^2 N} \qquad (62)$$

$$= \frac{(0.5)\ (0.111)\ (11.2 \times 10^6)}{(4500)^2\ (30)}$$

$$R_1C = 0.00102$$

(Maximum overshoot occurs at $N_{max}$ which is minimum loop gain)

Let $C = 0.5\mu F$

Then $R_1 = \frac{0.00102}{0.5 \times 10^{-6}} = 2.04k\Omega$

Use $R_1 = 2k\Omega$

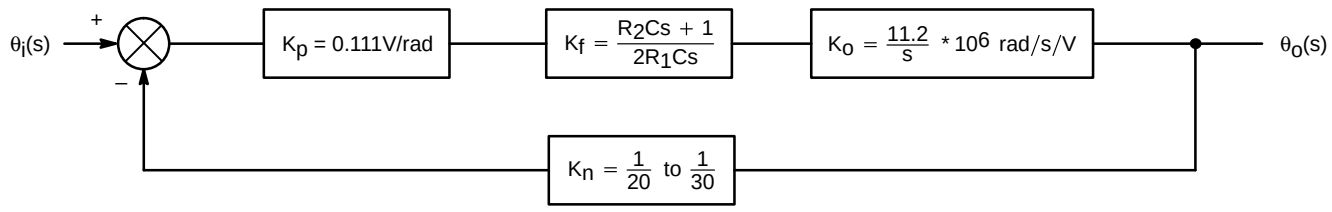



**Figure 10. Laplace Representation of Diagram in Figure 11**

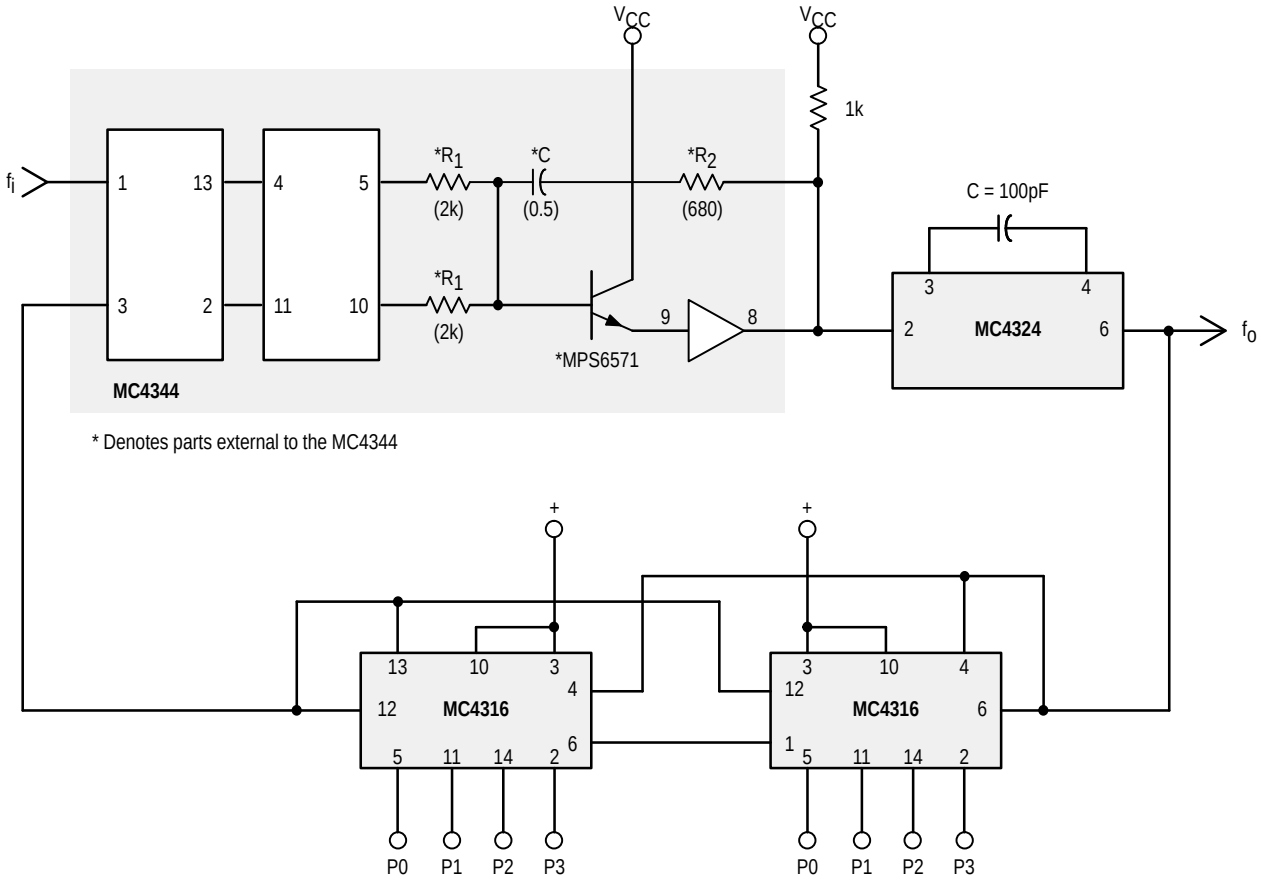



**Figure 11. Circuit Diagram of Type 2 Phase-Locked Loop**

$R_1$ is typically selected greater than 1kΩ.

Solving for $R_2$ in Equation 58

$$R_2 = \frac{2\zeta\ \omega_n\ R_1 N}{K_p\ K_v\ (0.5)} = \frac{2\zeta}{C\ \omega_n} \qquad (63)$$

$$= \frac{2(0.8)}{(0.5 \times 10^{-6})(4.5k)}$$

$$= 711\Omega$$

Use $R_2 = 680\Omega$

All circuit parameters have now been determined and the PLL can be properly configured.

Since the loop gain is a function of the divide ratio $K_n$, the closed loop poles will vary its position as $K_n$ varies. The root locus shown in Figure 12 illustrates the closed loop pole variation.

The loop was designed for the programmable counter N = 30. The system response for N = 20 exhibits a wider bandwidth and larger damping factor, thus reducing both lock-up time and percent overshoot (see Figure 14).

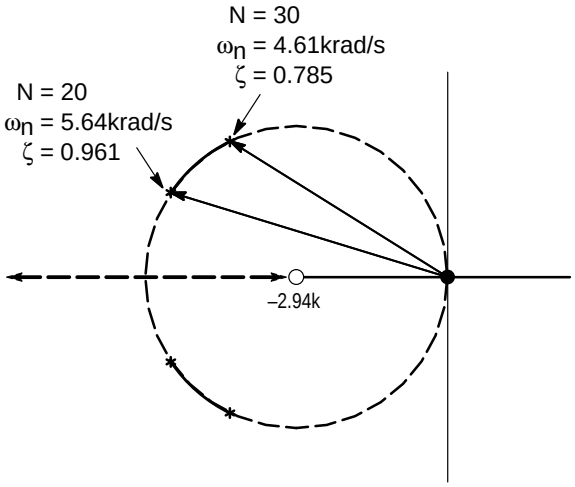



**Figure 12. Root Locus Variation**

NOTE: The type 2 second order loop was illustrated as a design sample because it provides excellent performance for both type 1 and 2 applications. Even in systems that do not require phase coherency, a type 2 loop still offers an optimum design.

## Experimental Results

Figure 13 shows the theoretical transient frequency response of the previously designed system. The curve N = 30 illustrates the frequency response when the programmable counter is stepped from 29 to 30, thus producing a change in the output frequency from 2.9MHz to 3.0MHz. An overshoot of 18% is obtained and the output frequency is within 5kHz of the final value one millisecond after the applied step. The curve N = 20 illustrates the output frequency change as the programmable counter is stepped from 21 to 20.

Since the frequency is proportional to the VCM control voltage, the PLL frequency response can be observed with an oscilloscope by monitoring pin 2 of the VCM. The average frequency response as calculated by the Laplace method is found experimentally by smoothing this voltage at pin 2 with a simple RC filter whose time constant is long compared to the phase detector sampling rate, but short compared to the PLL response time. With the programmable counter set at 29 the quiescent control voltage at pin 2 is approximately 4.37 volts. Upon changing the counter divide ratio to 30, the control voltage increases to 4.43 volts as shown in Figure 14. A similar transient occurs when stepping the programmable counter from 21 to 20. Figure 14 illustrated that the experimental results obtained from the configured system follows the predicted results shown in Figure 13. Linearity is maintained for phase errors less than $2\pi$, i.e. there is no cycle slippage at the phase detector.

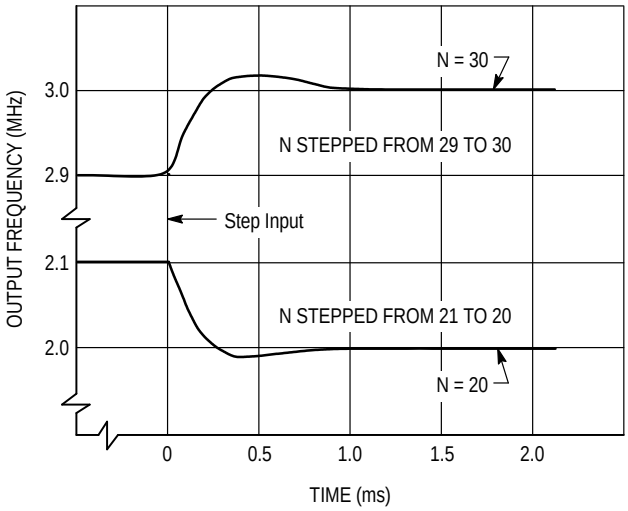



**Figure 13. Frequency-Time Response**

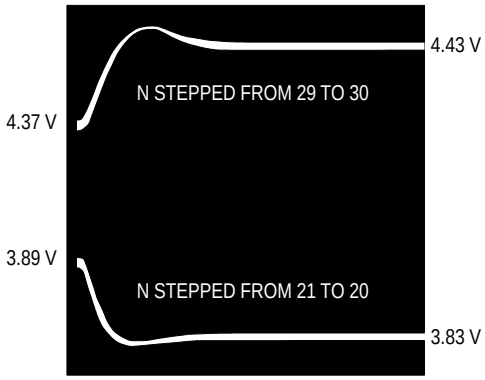



**Figure 14. VCM Control Voltage** (Frequency) **Transient**

Figure 15 is a theoretical plot of the VCM control voltage transient as calculated by a computer program. The computer program is written with the parameters of Equations 58 and 59 (type 2) as the input variables and is valid for all damping ratios of $\zeta \leq 1.0$. The program prints or plots control voltage transient versus time for desired settings of the programmable counter. The lock-up time can then be readily determined as the various parameters are varied. (If stepping from a higher divide ratio to a lower one, the transient will be negative.) Figures 14 and 15 also exhibit a close correlation between experimental and analytical results.

## Summary

This application note describes the basic control system techniques required for phase-locked loop design. Criteria for the selection of the optimum type of loop and methods for establishing the desired performance characteristics are presented. A design example is illustrated in a step-by-step approach along with the comparison of the experimental and analytical results.

***THE PARAMETERS LISTED BELOW APPLY TO THE FOLLOWING PLOT**

| | |
|---|---|
| PHASE DETECTOR GAIN CONSTANT | P1 = 0.111 VOLTS PER RADIAN |
| VCM GAIN CONSTANT | V1 =1.12 E+7 RAD PER VOLT |
| FILTER INPUT RESISTOR | R1 = 3900 OHMS ($R1_C$ = 2k) |
| FILTER FEEDBACK RESISTOR | R2 = 680 OHMS |
| FILTER CAPACITOR | C1 = 0.5 MICROFARADS |
| DIVIDER VALUE | N1-N2 = 29 – 30 |
| REFERENCE FREQUENCY | F1 = 100000 CPS |
| OUTPUT FREQUENCY CHANGE | F5 = 100000 CPS |

| | |
|---|---|
| P2 = 0.111 | C2 = 0.5 |
| V2 = 1.12 E+7 | N3-N4 = 21 – 20 |
| R3 = 3900 ($R1_C$ = 2k) | F2 (F6) = 100000 (100000) |
| R4 = 680 | |

**P L O T  O F  F U N C T I O N S**

**(NOTE: Y(T) IS '+', Z(T) IS '*', AND '∅' IS COMMON)**

**FOR T: TOP = 0 BOTTOM = 0.0015 INCREMENT = 0.0005**
**FOR FCTS: LEFT = 0 RIGHT = 0.12 INCREMENT = 0.002**

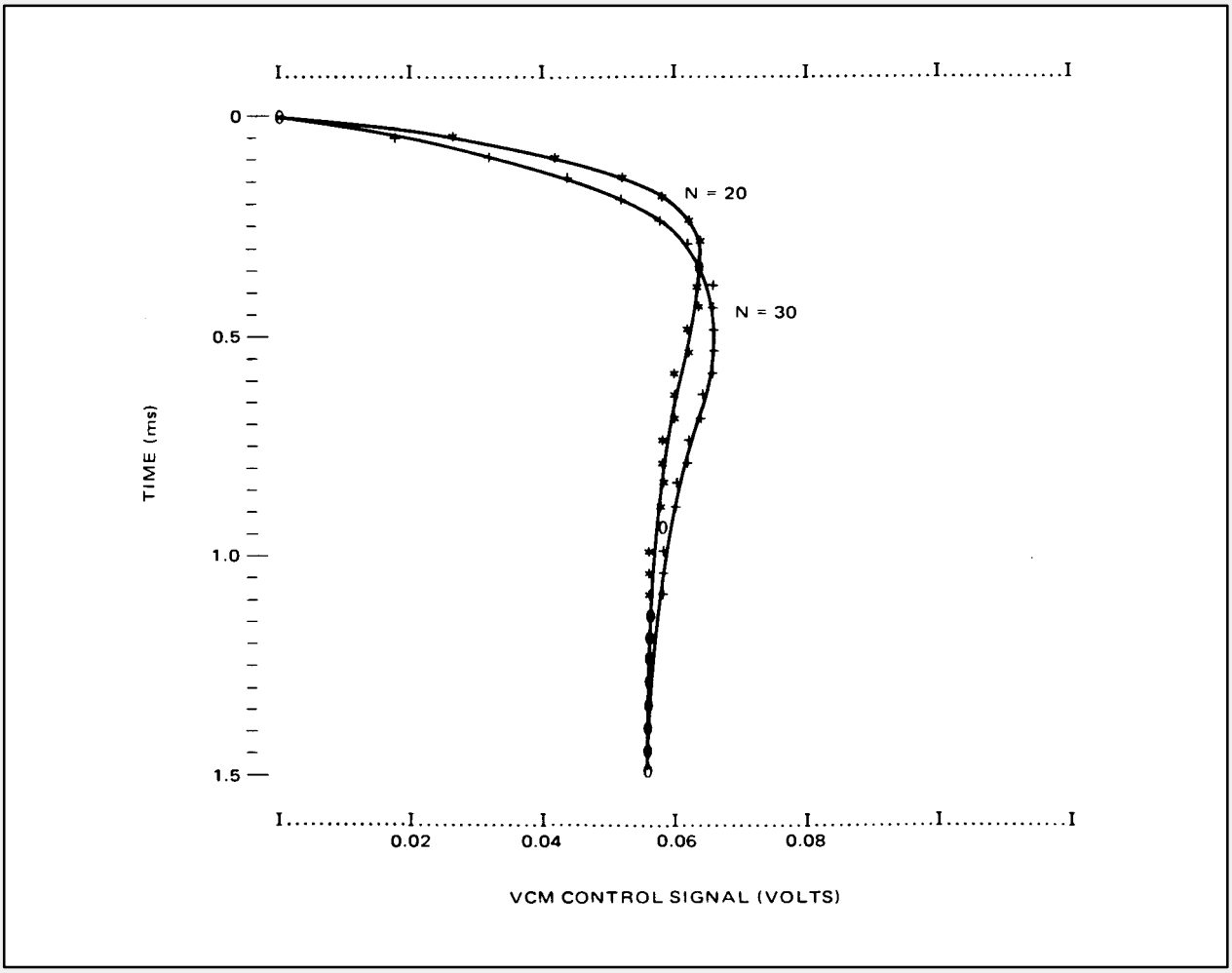



**Figure 15. VCM Control Signal Transient**

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