An Agile, Low-Power CMOS Digitally Synthesized 0-13 MHz Sinewave Generator

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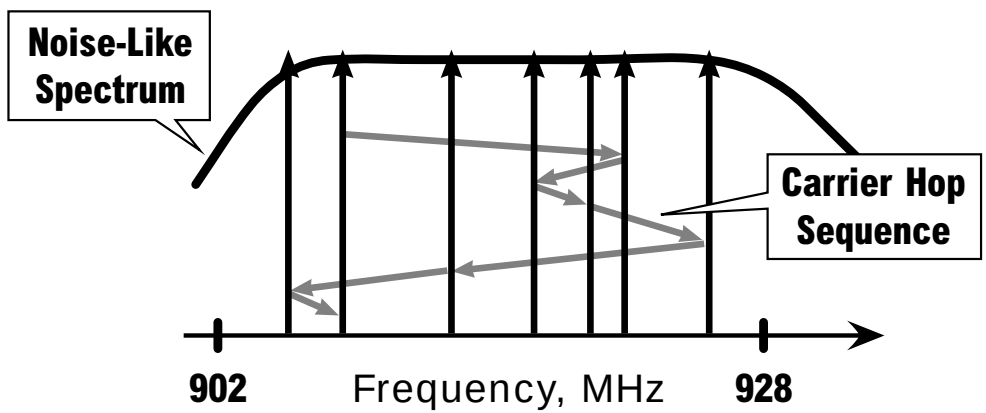
Outline

- Agile Frequency Synthesis in Wireless Transceivers
- Direct Digital Frequency Synthesizer
- D/A Converter
- Measurements of Spectral Purity
- Conclusions

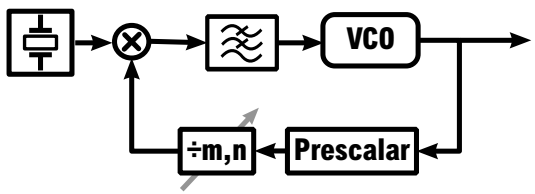
Frequency-Hopped Spread Spectrum

- Spread-spectrum communications allow a large number of users can share the same spectrum; intended user searches for particular spreading code
- FCC has allocated 902-928 MHz band for unlicensed, spread-spectrum use
- Techniques of spectrum spreading: *direct-sequence* or *frequency-hopping*
- Frequency-hopped spread-spectrum allows wideband spreading at any data rate (⇨ low power dissipation), but needs **agile frequency source**



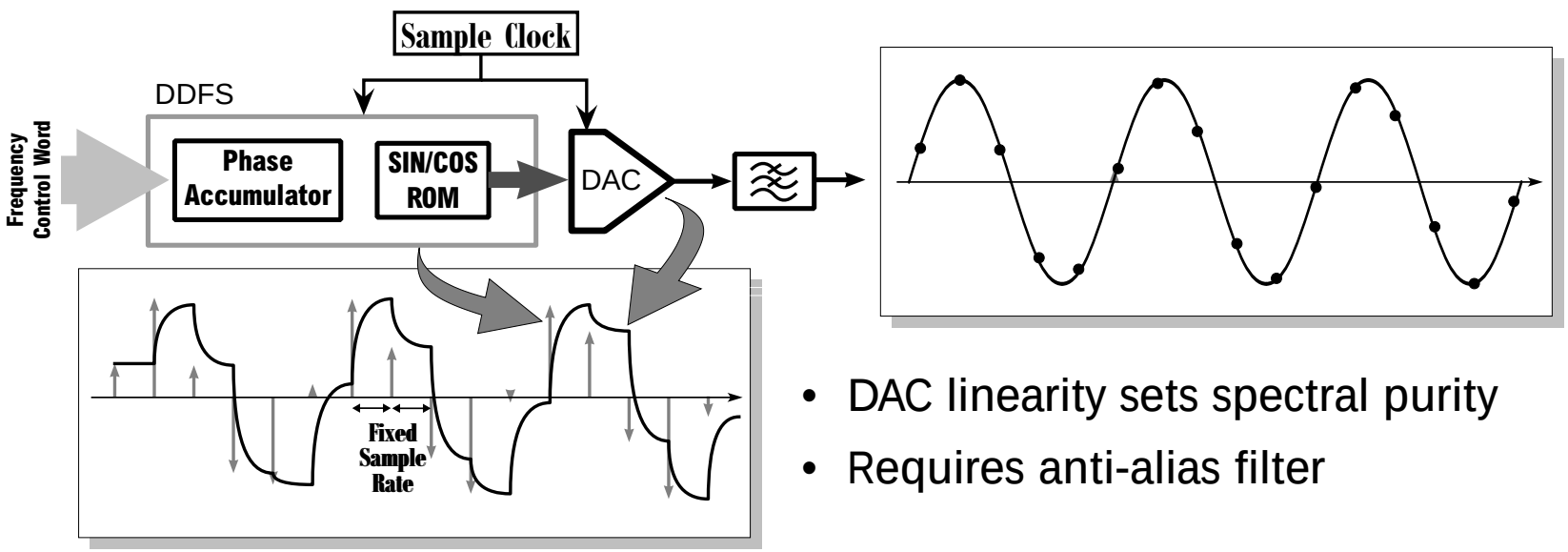
Methods of Frequency Synthesis

Phase-Locked Loop



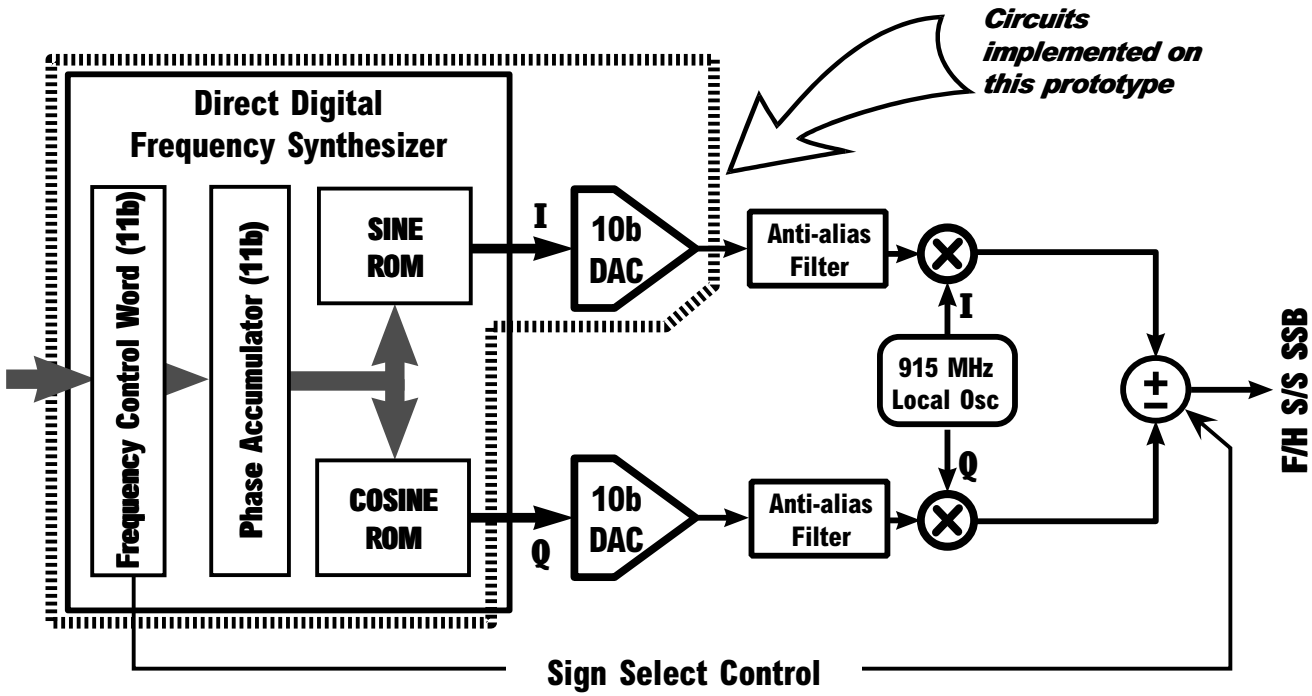
- Frequency agility limited by loop settling time
- Signal purity and wide tuning range compromise VCO design

Digital Synthesizer & D/A Converter



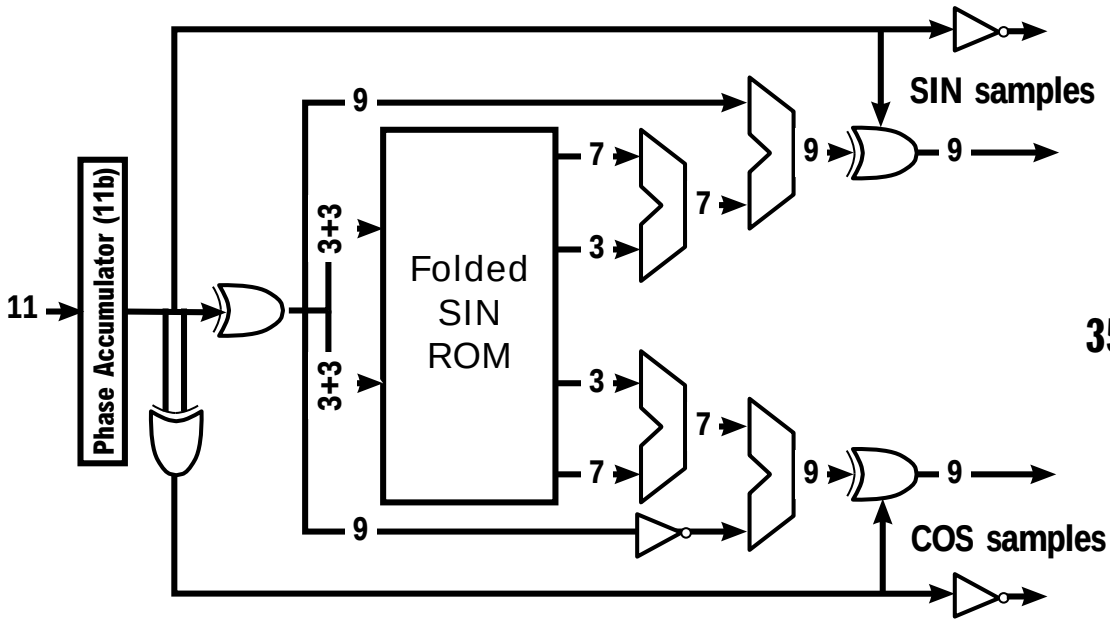
- DAC linearity sets spectral purity
- Requires anti-alias filter

Frequency-Hopping RF Transmitter



- Single-step I-Q upconversion produces single-sideband, suppressed-carrier output in the 902-928 MHz band
- DDFS/DAC need only span 0→13 MHz: sign-select at output produces 902-915 MHz, or 915-928 MHz
- Order of anti-alias filter depends on highest output frequency relative to sample rate
- Acceptable image suppression requires 8b matching in two channels

Direct Digital Frequency Synthesizer



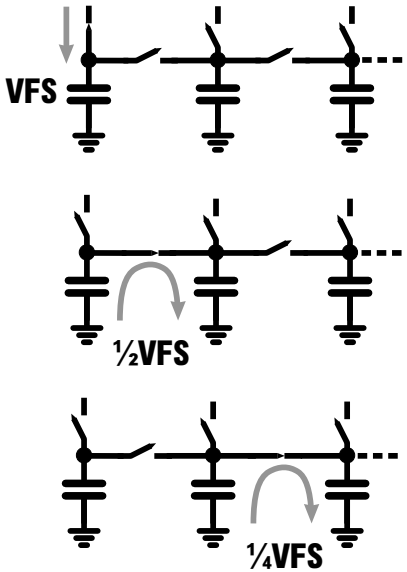
Nicholas & Samueli,
IEEE JSSC, Dec 1991

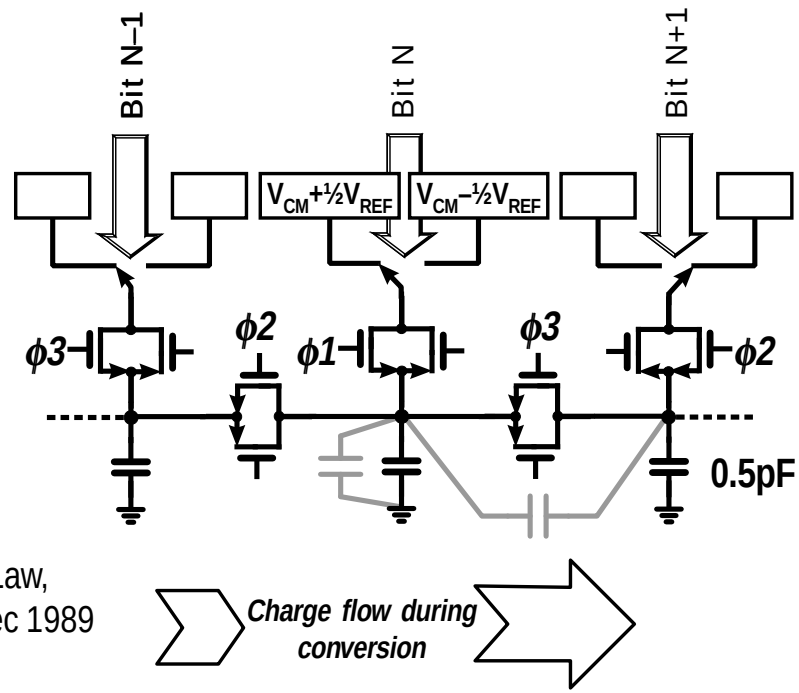
35 mW at 50 MHz, 3 V!

- DDFS guarantees spurious levels < –72 dBc
- Output frequency resolution is (Sample Rate)/2^{11}
  - ✓ ROM contains only quarter-wave data
  - ✓ SIN and COS generated from same ROM by phase-shift of argument
  - ✓ ROM stores difference between amplitude and phase (saves 2 bits)
  - ✓ One large table is replaced by small coarse and fine tables

⇨ ROM is 32× smaller

Principle of Low-Power, High-Speed DAC





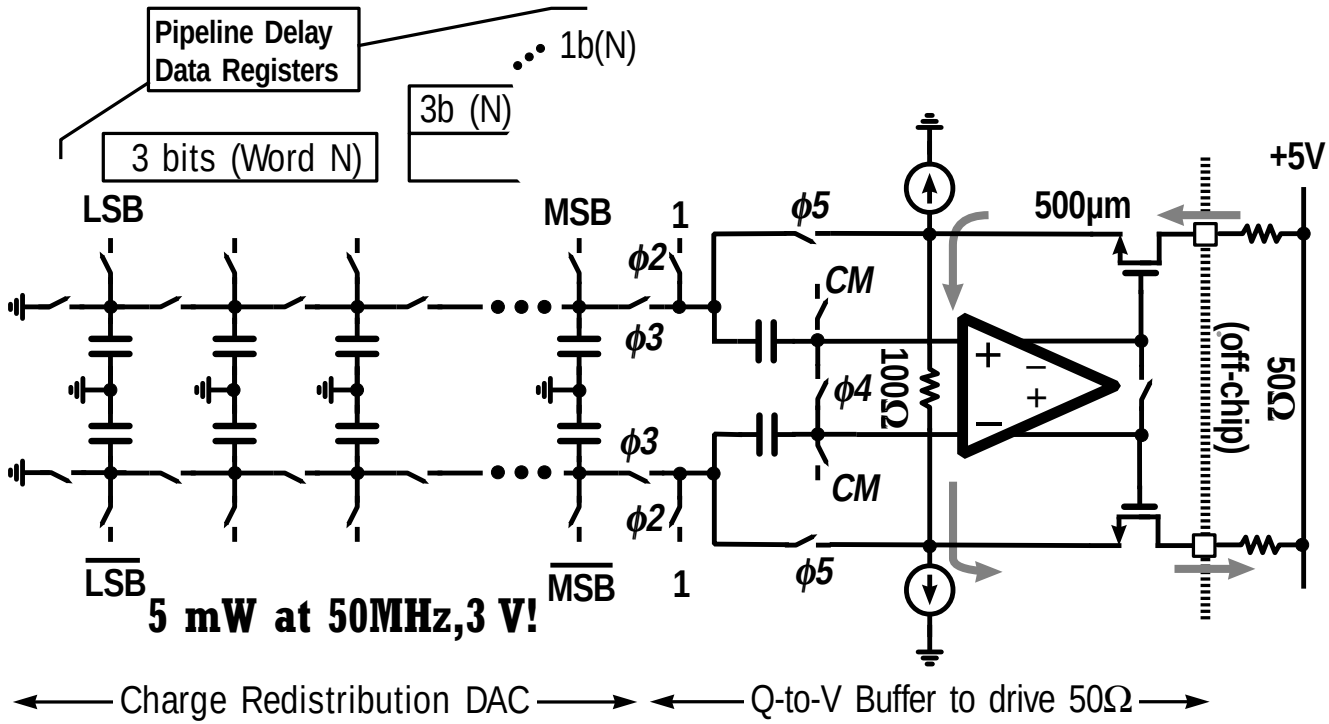
Wang, Temes, Law,
IEEE JSSC, Dec 1989

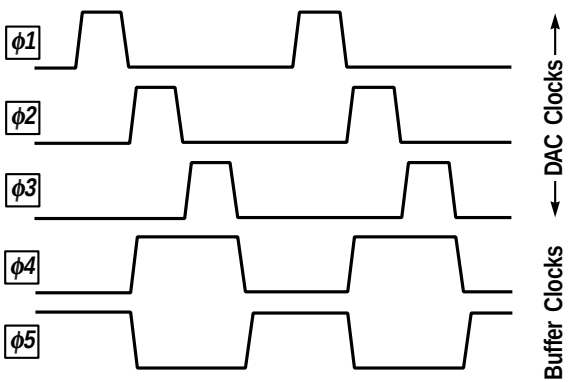
Charge flow during conversion

- Binary division by successive charge redistribution
- Equal-sized capacitors required
- Three-phase clock for proper charge-transfer

- Pipelined operation produces one conversion per clock cycle
- Linearity limited by:
  - ☞ DAC capacitor mismatch
  - ☞ Stray capacitance in DAC cells
  - ☞ Signal-dependent charge injection after redistribution

DAC Implementation





- Differential implementation using two charge-redistribution pipelines
- Output buffer must be at least as linear as DAC — differential buffer degenerated by polysilicon resistor, and driven in closed-loop

What Sets DAC Power Dissipation?

Sources of Power Dissipation

- No static power dissipation in DAC core, but small dynamic CV^2f dissipation
- Clock buffers driving DAC switches dissipate most power

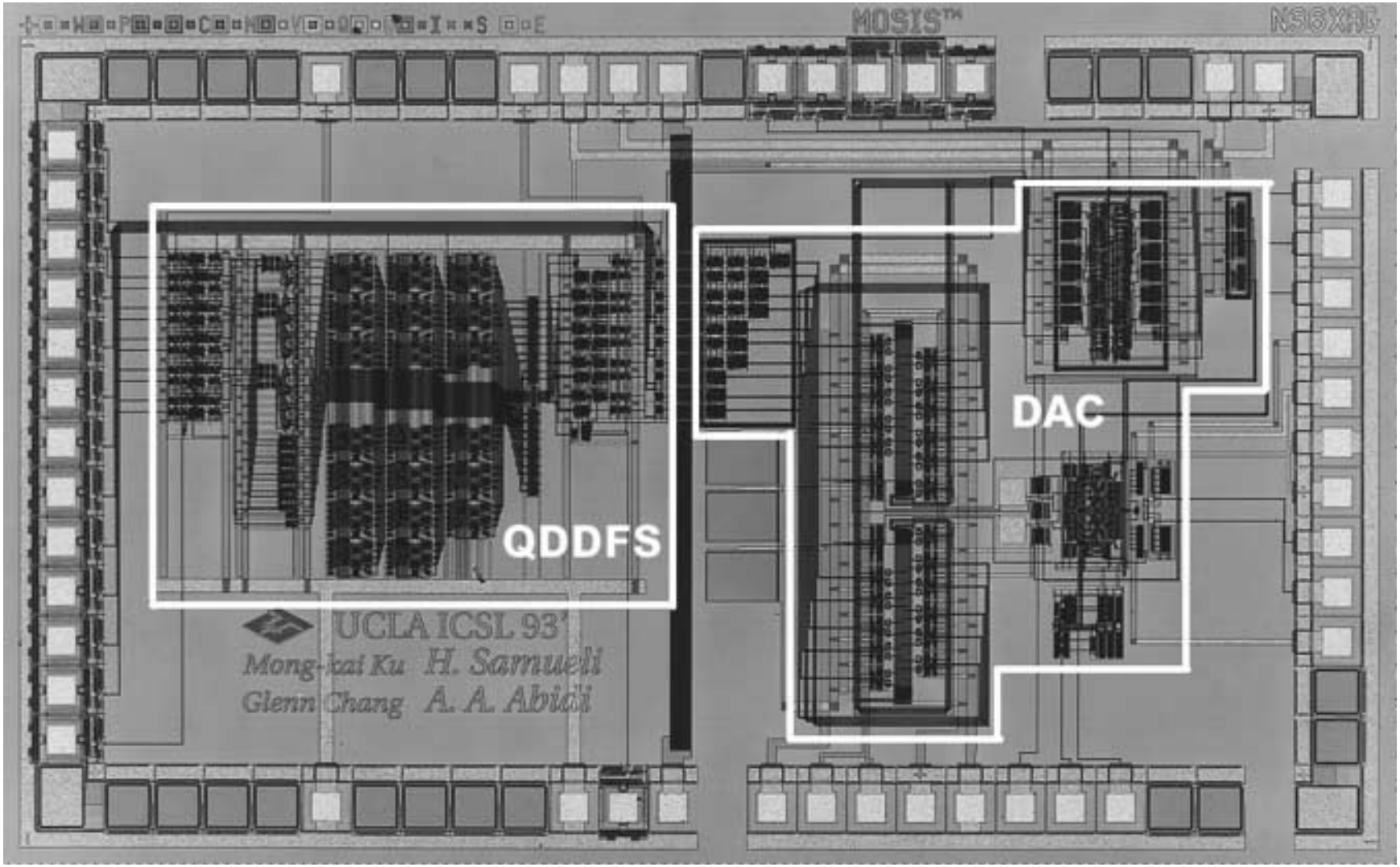
⇨ Power dissipation decreases as DAC cells are scaled down

Lower Limits to Scaling

- 0.5 pF capacitors (400 sq-µm area) *match* to within 0.1% rms

  🗐 Pelgrom, *et al.*, *IEEE JSSC*, Oct 1989

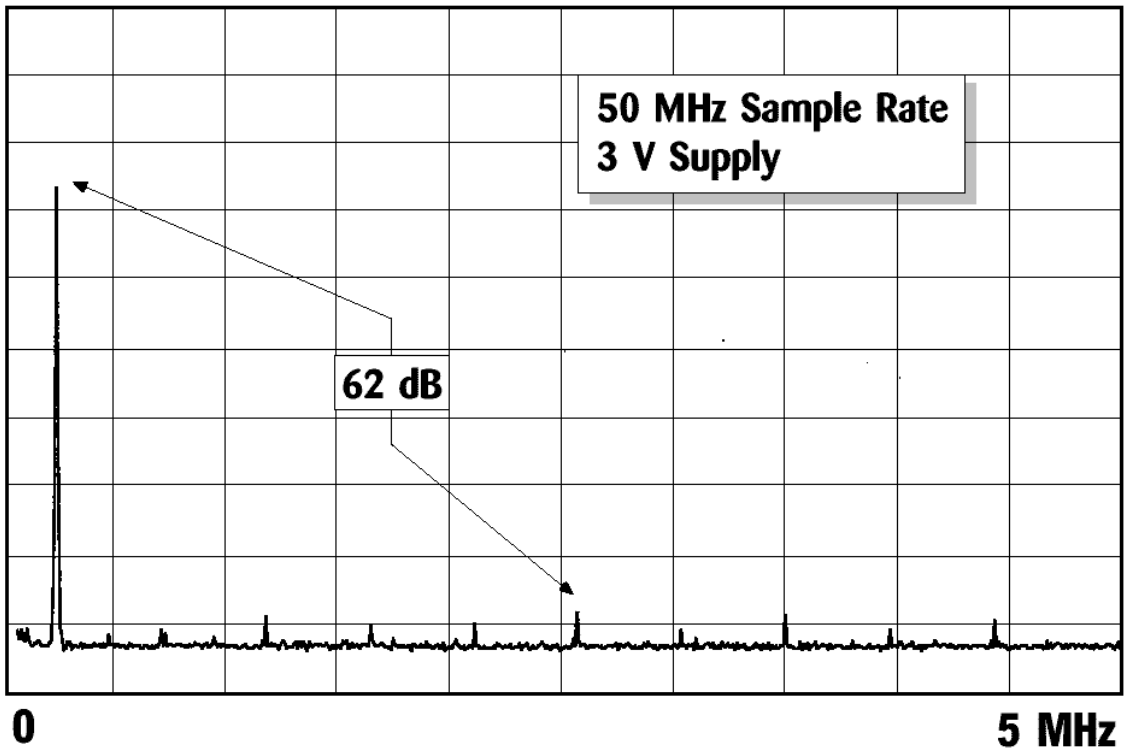
- Switch-induced *noise* with 0.5 pF capacitors accumulating in DAC ≈ 170 µV rms; output buffer *noise* ≈ 110 µV rms ⇨ LSB size > 0.5 mV
- *RC time constant* for settling to 10 b at 50 MHz sets width of switch FET ⇨ lower limit on nonlinear charge injection



1-µm CMOS with double-metal, linear capacitor

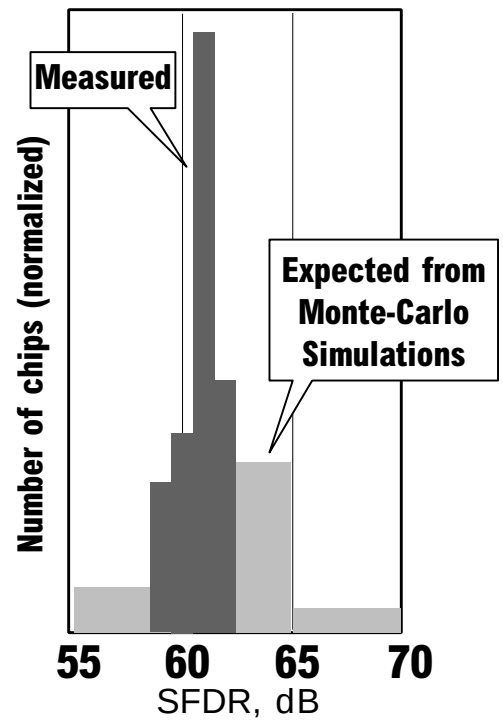
2.9 × 4.9 mm die size

Low-Frequency Synthesis

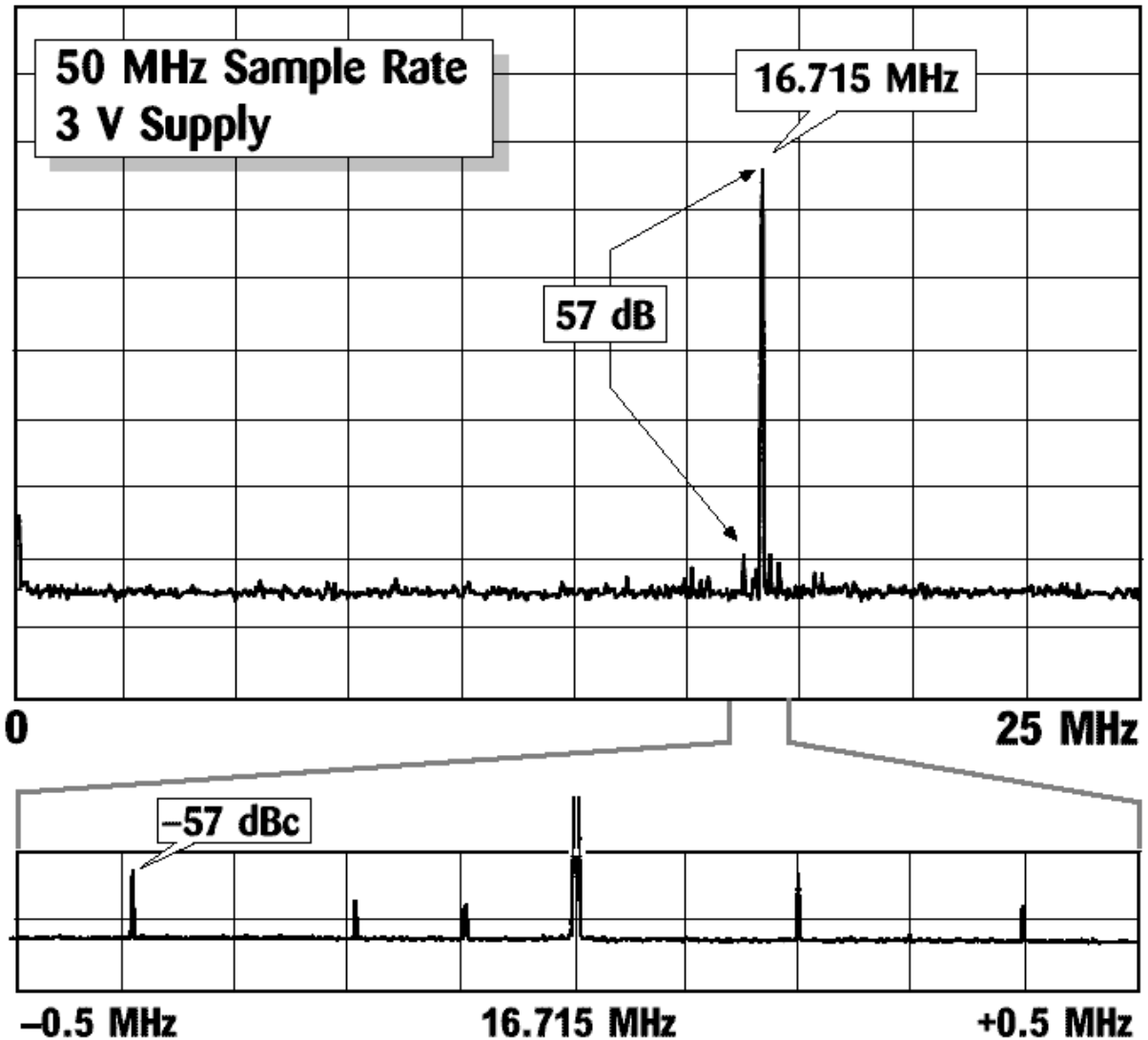


- ✓ Noise floor set by quantization noise
  — measure 2 dB higher than theoretical limit
- ✓ Spurious level as predicted
  — set by capacitor mismatch

Repeatability

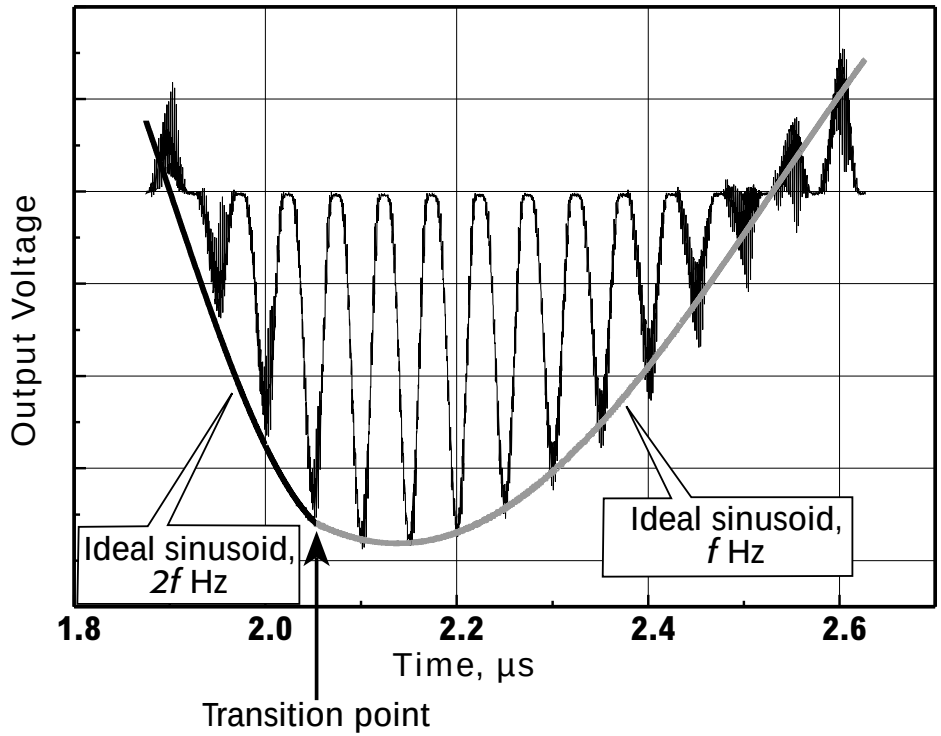


High-Frequency Synthesis



- Spurious levels grow at high frequencies due to 1fF inter-cell stray capacitance
- *No* slew-rate limiting or output glitch at 50 MHz
- On-chip digital circuits do *not* contaminate output spectrum!

Frequency Agility



- Output instantly switches from one frequency to another (after 8 clock cycle latency through DDFS/DAC)
- Anti-alias filter will limit the settling response in system

Conclusions

- ✓ First demonstration of monolithic CMOS 10b DDFS/DAC
- ✓ Low-power design leads to 35 mW DDFS, and 5 mW 10b DAC core, both operating at 50 MHz from 3-V
- ✓ Spectral purity from untrimmed parts is –62 dBc at low frequencies, –57 dBc at 1/3 Sample Rate
- ✓ Low-power circuits ➪ small interaction between analog and digital parts of the chip
- ✓ Direct digital frequency synthesis is a viable solution for an agile sinewave source in battery-powered wireless transceivers